ENGINEERING TRIPOS PART IIA

Thursday 24 April 2008 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

STATIONERY REQUIREMENTS SPECIAL REQUIREMENTS
Single-sided script paper Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

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1 (a) Write brief notes, relating to hazards on the following:

Static-1 hazard, function hazard, dynamic hazard and essential hazard. [10%]

(b) State the theorems that allow a product of sums (POS) logic expression to be free of static and dynamic hazards. Find a hazard-free realisation of the function:

$$T=\Sigma\ (2,3,6,7,8,10),$$

using only

(i) NOR gates,

and then only

(ii) NAND gates. [50%]

(c) Use the tabular method to determine the simplest sum of products (SOP), in terms of ABCD, with A being the most significant, where:

$$T=\Sigma(2,3,5,6,7,8,9,10,11).$$

Also write your result in a minimal product of sums (POS) expression. [40%]

2 (a) A multiplexer, with four data lines D_0, D_1, D_2, D_3, has two control lines P, Q (with Q being more significant) and it is to be wired to yield a logic function:

$$Y=\overline{A}\cdot\overline{B}+A\cdot\overline{B}\cdot\overline{C}+A\cdot B\cdot C\,.$$

Explain how this is done and show a circuit diagram of your solution. [30%]

(b) Explain the differences between *Mealy* and *Moore* sequential circuits. [10%]

(c) A Gray-Code counter is made from four J-K bistables whose outputs are G_3, G_2, G_1, G_0. Fig. 1 shows the path of the desired Gray sequence on a Karnaugh Map. Implement the design synchronously using only 2 and 3 input NAND gates with the four J-K bistables. Show clearly the state table and Karnaugh maps that are needed to give the simplest inputs for the J-K bistables. A full circuit need not be drawn. [60%]

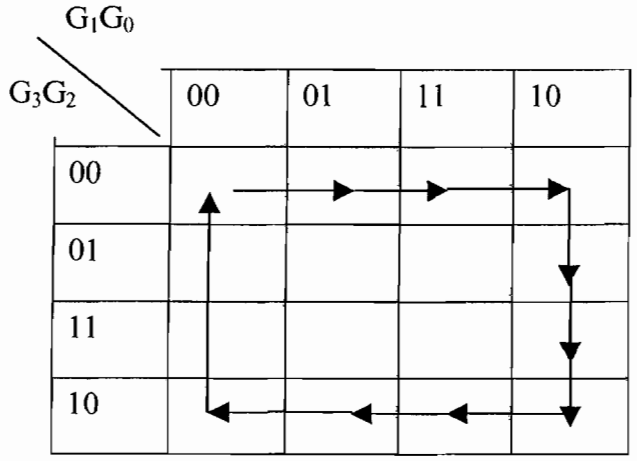

Fig. 1

3 (a) Compare the advantages and disadvantages of the major digital logic families based on MOS and bipolar devices. In your account indicate briefly under what circumstances each family can provide desirable properties. Why has CMOS technology emerged as the most popular choice? [10%]

(b) Two MOS transistors with channel lengths L_1 and L_2 and equal channel widths W are connected in series, and have their gate electrodes connected together as shown in Fig. 2. Show that the two transistors acting together, in non-saturation mode, have a current-voltage characteristic that is the same as that of a single transistor with channel length equal to $L_1 + L_2$. You may neglect the body effect, but state any other assumptions made. [40%]

(c) Fig. 3 shows a two-input NAND gate implemented as a CMOS circuit using MOS transistors with channel dimensions W/L as indicated. Determine the supply current drawn if inputs A and B are linked together and connected to a supply of 1.5 V. The circuit parameters are $V_{DD} = 3$ V, $V_{TN} = 0.5$ V, $V_{TP} = -0.5$ V and $k = k' W / L$, where $k'_N = 10\ \mu A/V^2$ and $k'_P = 5\ \mu A/V^2$. [50%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad V_{DS} \geq (V_{GS} - V_T)$$

where the symbols have their usual significance.

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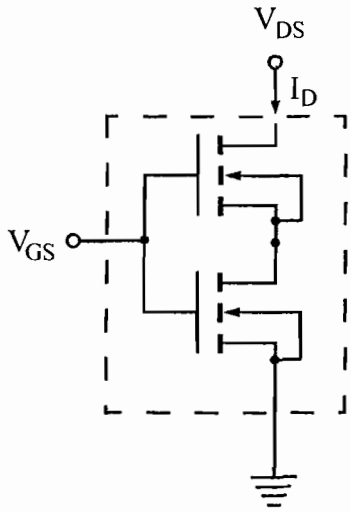

Fig. 2

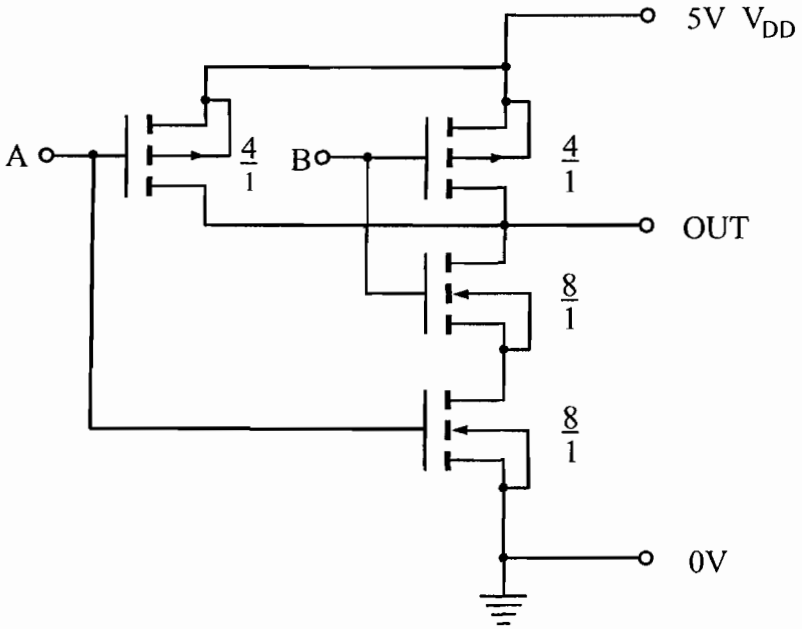

Fig. 3

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4 (a) The circuit shown in Fig. 4 represents an emitter-coupled logic gate. Briefly describe the mode of operation of the device. [10%]

(b) The design is to be operated in an environment in which $V_{CC} = 0$ V, $V_{EE} = -5.2$ V and $V_R = -1.2$ V. $V_{BE(on)}$ may be taken as 0.8 V for all transistors. The output logic voltage levels are to be $V_R + 0.4$ and $V_R - 0.4$. For all transistors the maximum allowable emitter current is 5 mA. Within these constraints, the logic gate is to be designed to achieve maximum switching speed.

(i) Determine the values of resistors R_1 and R_2, and hence the values of the remaining resistors R_E, R_{C1},R_{C2}. For these calculations you may ignore all base currents. [40%]

(ii) Sketch the voltage transfer characteristic for this circuit assuming that the width of the transition region is 200 mV. [50%]

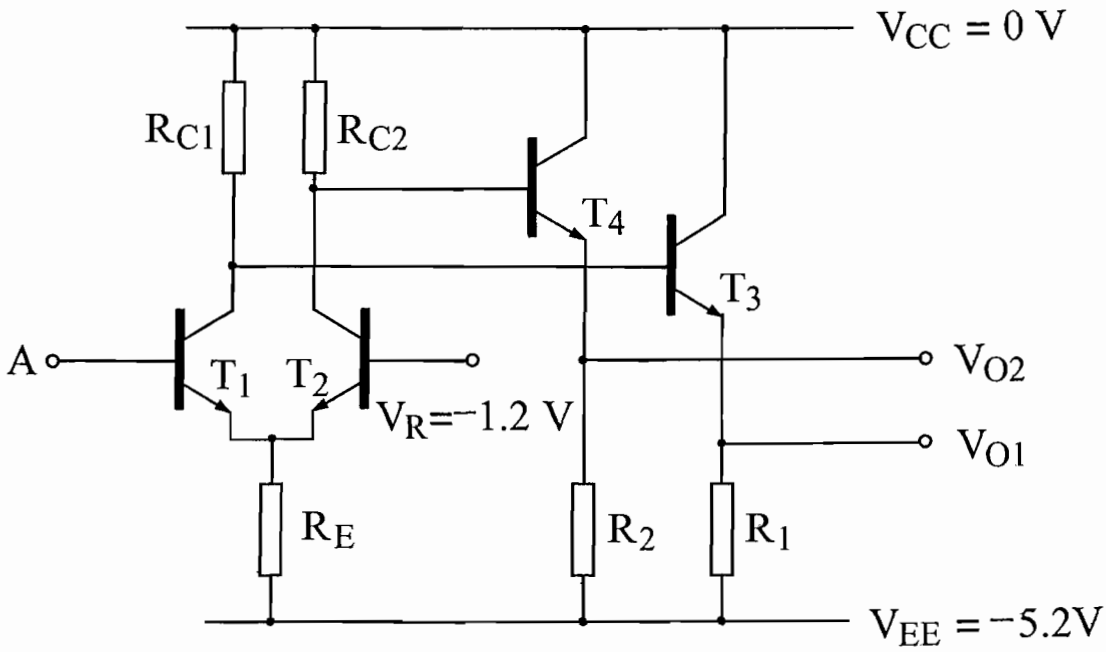

Fig. 4

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