ENGINEERING TRIPOS PART IIA

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Tuesday 6 May 2008 9 to 10.30

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Module 3F5

COMPUTER AND NETWORK SYSTEMS

*Answer not more than **three** questions.*

*All questions carry the same number of marks.*

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*There are no attachments.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

**You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator**

1 (a) Explain what is meant by a *pipelined* datapath. What are pipeline *hazards*? [20%]

(b) Some pipeline hazards can be resolved by *data forwarding*. Explain how this works in the context of the 5-stage MIPS pipeline. Illustrate your answer with a sketch, showing how the forwarding unit is connected to other parts of the datapath. What sort of data hazards cannot be resolved by data forwarding? [40%]

(c) The lecture notes for this course state that "to achieve a good speed-up, we require the pipe stages to be *balanced*." Investigate this statement in the context of the following 5-stage MIPS pipeline:

| **Stage** | **Execution time** |
|---|---|
| IF (instruction fetch) | $kT$ |
| ID (instruction decode and register fetch) | $T$ |
| EX (execution and effective address calculation) | $kT$ |
| MEM (memory access) | $kT$ |
| WB (write back data to registers) | $T$ |

Assuming no stalls, find the time taken to execute $n$ instructions (i) without pipelining and (ii) with pipelining. In the limit as $n \to \infty$, sketch the pipelining speed-up as a function of $k$ in the range $0 \leq k \leq 10$. [40%]

2 (a) Distinguish between *accumulator* and *general purpose register, load-store* instruction set architectures. Illustrate your answer by showing, for each type of architecture, how two numbers in memory can be added and the result stored back into memory. [20%]

(b) What are the distinguishing features of reduced instruction set computer (RISC) architectures? [20%]

(c) Why do hardware designers go to great lengths to reduce the latency of arithmetic logic units (ALUs)? Might this be less important if the ALUs were deployed in a pipelined datapath? [20%]

(d) Describe the operation of a single level, 4-bit carry-lookahead adder. [20%]

(e) Compare the time and space requirements of ripple-carry and carry-lookahead adders. What factors affect the optimal number of levels in a carry-lookahead adder? [20%]

3 (a) Draw a diagram showing the seven-layer open systems interconnection (OSI) reference model for the interconnection of two computers. Clearly label each layer in the model and mark the different working environments. Explain the role of each of these environments within the OSI model. [30%]

(b) Identify which layer in the OSI model would contain the following network operating procedures. Briefly explain your reasons.

(i) Manchester coding [5%]

(ii) Frame check sequence [5%]

(iii) Remote login [5%]

(iv) JPEG to TIFF conversion [5%]

(v) MAC address lookup [5%]

(vi) Address resolution protocol [5%]

(c) Describe how the process of communication through the OSI reference model is performed from both a theoretical and a practical perspective. Use the X.25 model to sketch this process. [20%]

(d) Possibly the most difficult protocol to map onto the OSI model is asynchronous transfer mode (ATM). Briefly explain some of the reasons why this mapping is so difficult. [20%]

4 (a) Give four different examples of physical media which could be used as a transport mechanism in a computer network. Briefly outline the key properties of each medium and indicate how these properties might influence the choice of protocols to use with the medium. [40%]

(b) Describe the differences between single-mode and multiple-mode optical fibre, and their relative performance, when used in a telecommunications network. Why has optical fibre been a very important physical medium within telecommunications networks? [30%]

(c) Explain why single-mode optical fibre has become a mainstay of the synchronous digital hierarchy (SDH). Sketch a simple SDH network at the lowest tier (synchronous transfer module 1, STM-1) and explain the role of each of the components within the network. [30%]

**END OF PAPER**