ENGINEERING TRIPOS PART IIA

Thursday 23 April 2009 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS	SPECIAL REQUIREMENTS
Single-sided script paper	Engineering Data Book
	CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. Fig. 1 shows two digital inverter stages, A and B, based on MOS transistors. Both n-channel transistors shown have a threshold voltage V_{Tn} of 1 V and process transconductance parameter $k'_n = 2 \times 10^{-5}$ AV^{-2}. The p-channel device M_2 has a threshold voltage V_{Tp} of –1 V and process transconductance $k'_p = 1 \times 10^{-5}$ AV^{-2}. In each circuit, the transistor M_1 has an aspect ratio (W/L) of 4. The transistor M_2 has an aspect ratio (W/L) of 8. Each inverter drives a load assumed to be entirely capacitive, represented by C_L. The supply voltage V_{DD} is 3 V for each circuit.

(a) Determine the output voltage V_O for each circuit under the following conditions:

(i) input voltage $V_I = 0$;

(ii) input voltage $V_I = V_{DD}$. [40%]

(b) Explain carefully how the channel dimensions for transistor M_2 should be chosen in order to better balance the delays observed for rising and falling edges applied to the gate input; hence show that the dimensions for gate B already meet this condition. How is this consideration adapted in the design of logic gates with more than one input? [20%]

(c) The inverter B gate receives an input signal V_I which switches abruptly from 0 V to V_{DD}. Assuming the load capacitance C_L is 5 pF, determine the falling edge delay t_{DEL} between the input transition and corresponding output, using the 50% convention for estimation of this delay. State any other assumptions made. [40%]

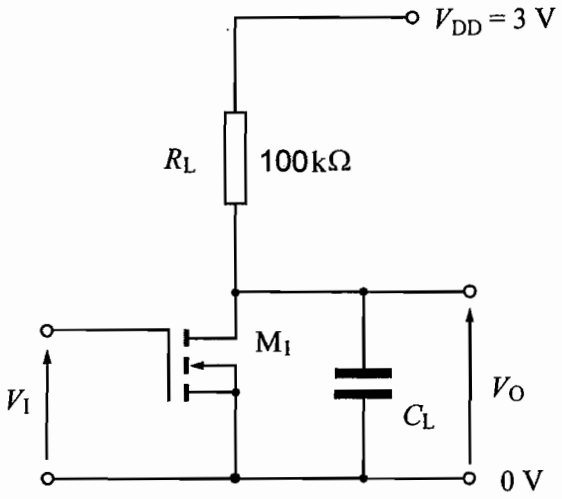
You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{DS} < (V_{GS} - V_T)$$

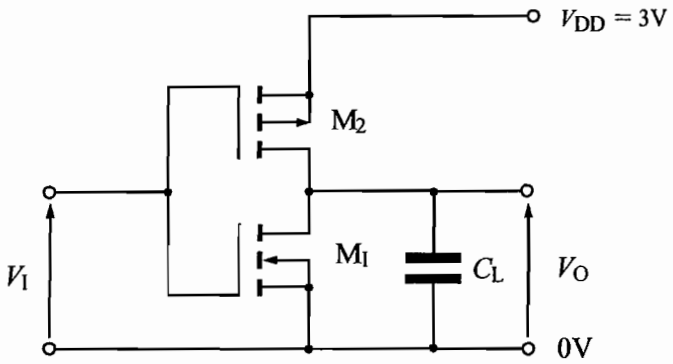
$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad V_{DS} \geq (V_{GS} - V_T)$$

where k is the device transconductance parameter and the other symbols have their usual significance.

(cont.



A



B

Fig. 1

2 (a) The term *saturation* has different meanings according to whether it refers to logic circuits containing MOS transistors or to those based on bipolar transistors. Discuss this statement with reference to the circuits shown in Fig. 2, which depicts primitive logic gates based on MOS and bipolar devices. Explain clearly the circumstances in the operation of logic gates in which saturation may be observed, and how this may affect their performance. [35%]

(b) Consider the operation of the circuits shown in Fig. 2. For circuit A, the device transconductance parameter k is 8×10^{-5} AV^{-2} and V_T is 1 V. For circuit B, the values of V_{CEsat} and V_{BEsat} are 0.2 V and 0.7 V respectively. The bipolar transistor has large-signal current gain $\beta = 100$. [35%]

Determine for each gate the range of input voltages V_I for which the phenomenon of saturation will be observed.

(c) Fig. 3 shows a basic NAND gate described in a research paper published a few years ago. Describe the operation of the circuit and discuss its potential advantages and disadvantages in comparison with other principal families of logic. [30%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad V_{DS} \geq (V_{GS} - V_T)$$

where k is the device transconductance parameter and the other symbols have their usual significance.

(cont.

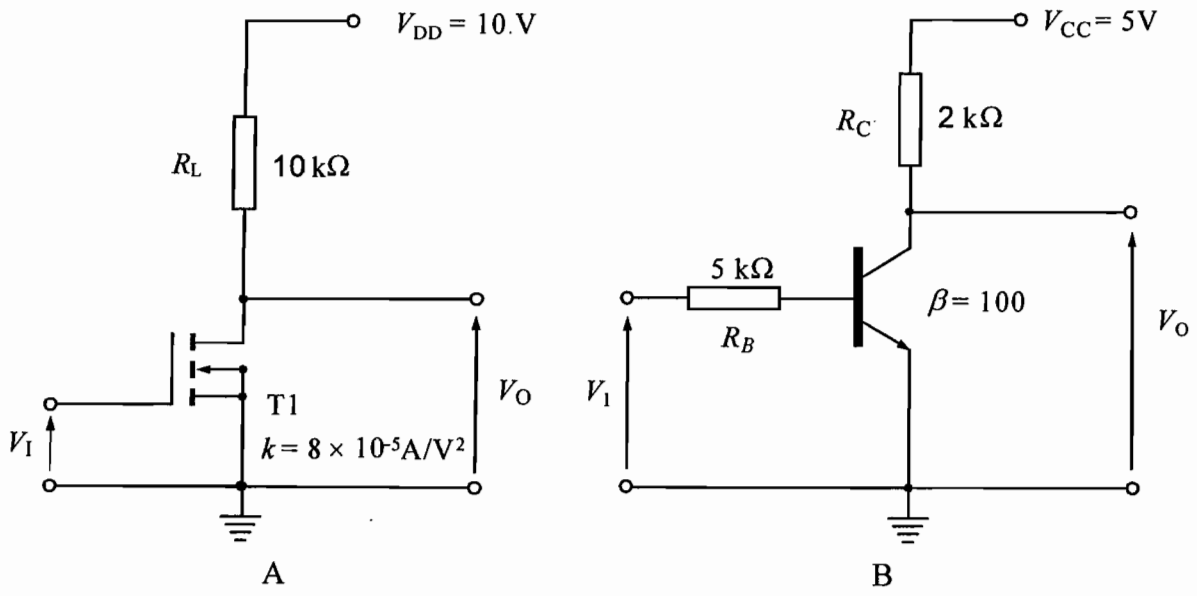

V_{DD} = 10.V
R_L
10 kΩ
V_I
T1
k = 8 × 10^{-5}A/V^2
V_O
A
V_{CC}= 5V
R_C
2 kΩ
5 kΩ
R_B
β= 100
V_I
V_O
B

Fig. 2

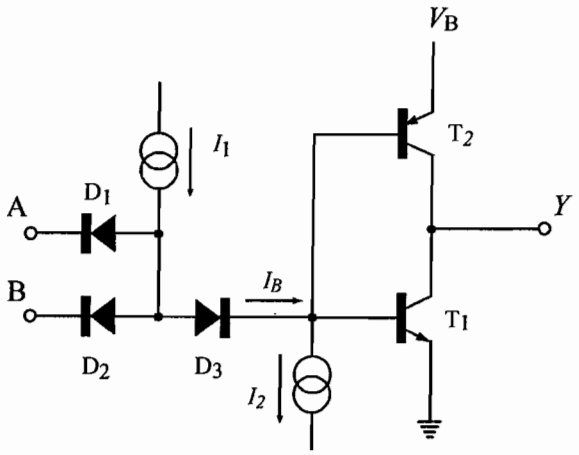

V_B
I_1
T_2
A
D_1
Y
B
I_B
T_1
D_2
D_3
I_2

Fig. 3

3 (a) Find the minimum sum-of-products (SOP) expression for the following function using the Quine McClusky tabular method:

$$T = \Sigma\,(0, 2, 16, 18, 24, 26, 28, 30)$$ [40%]

(b) Fig. 4 shows a combinational logic circuit. Assume that C and $\overline{C}$ change at the same instant, as they are available from a bistable, and that the gates G1, G3 and G5 have each a delay of δ. G2 and G4 have larger delays of 2δ and 4δ respectively.

Draw a clear timing diagram showing C changing from 0 to 1 with A=B=1. Demonstrate that there is a hazard, give its type and find the total delay before the output settles. [30%]

Redesign the circuit to remove the hazard, show its implementation using a selection of gates G1 to G5 and optimise the circuit for minimal total delay when C changes from 0 to 1 with A=B=1. Draw a timing diagram showing no hazard for this situation. Re-optimise the circuit for minimal delay if any of A,B,C variables change, one at a time. What is the maximum delay in this case? [30%]

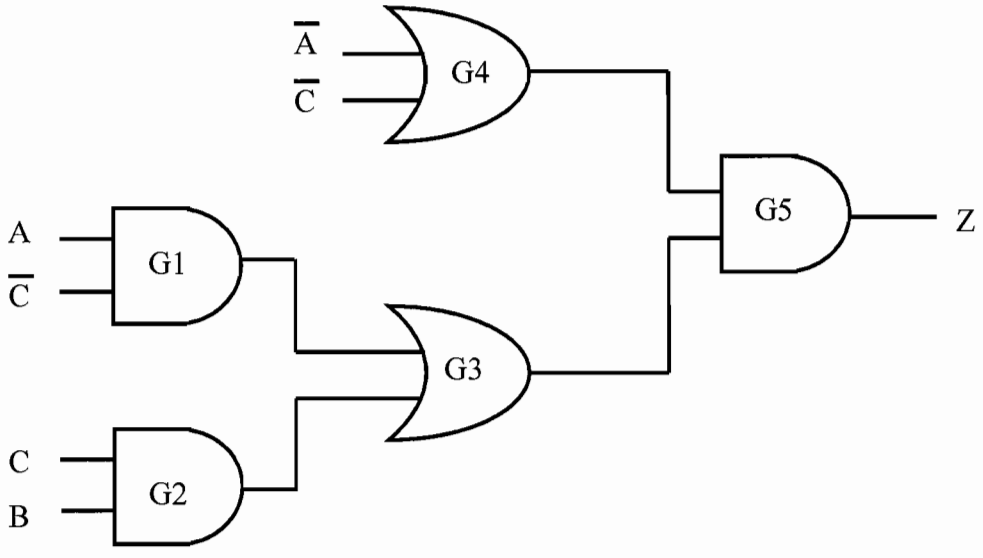


Fig. 4

(cont.

4 A sequential circuit is to be designed having a simple line input X and a single output Z. Starting in a reset state, the circuit receives input sequences consisting of 3-bit words. Each bit is presented for one clock period and there is a gap of one clock period between successive words. The circuit must be in a reset state at the beginning of each word. The output is to be Z=1 upon receipt of the third bit of a word if the total number of level changes (from 0 to 1 or 1 to 0) is odd (101, for example, has two level changes while 001 has only one). Such circuit is called a *change-of-level detector*.

Draw the state diagram and state table for a Mealy implementation showing the allocation of states and the output. [60%]

Draw the circuit implementation of the control using a single ROM and D bistables. What is the size of the memory needed? [40%]

END OF PAPER

Numerical answers 3B2 –2009

1 (a) V_{OL} = 0.185 V for inverter A, V_{OL} = 0 V for inverter B

(c) $I_{D1} = 16\times10^{-5}$ A $\quad t_{sat} = \frac{C_L}{I_{D2}}$ = s = 31 ns $t_{non-sat}$ = 15.9 ns]

The total delay, the sum of t_{sat} and $t_{non-sat}$, or 31 + 15.9 = 46.9 ns

2. (b) V_{DS} = +3.9 V; the range of V_{GS} values for saturation is +1.0 to +4.9 V

V_{IN} = 0.82 V

3. (a) Simplified function $T = \overline{B}\,\overline{C}\,\overline{E} + A\,B\,\overline{E}$

(b) Z = A'BC+ AC'. The minimal delay in the output when C changes from 0 to 1 for A=B=1 can be obtained as 2δ. The total delay = 3δ

4. D1= $y1^{+}$= Σ (1, 2, 3, 6,7,8,9,10,11,14,15)

D2= $y2^{+}$= Σ (1, 5, 9, 13)

D3= $y3^{+}$= Σ (0, 8, 9, 13)

Z= Σ (2, 3, 14, 15)