1(b)

(i) LS-TTL drives CMOS

$N_{MH} = V_{OHls\text{-}ttl} - V_{IHcmos} = 2.5 - 3.5 = -1.0$ V

$N_{ML} = V_{ILcmos} - V_{OLls\text{-}ttl} = 1.0 - 0.4 = 0.6$ V

(ii) CMOS drives LS-TTL

$N_{MH} = V_{OHcmos} - V_{IHls\text{-}ttl} = 4.9 - 2.0 = 2.9$ V

$N_{ML} = V_{ILls\text{-}ttl} - V_{OLcmos} = 0.7 - 0.1 = 0.6$ V

(c) CMOS → BiCMOS would give the following margins:

$N_{MH} = V_{OHcmos} - V_{IHBiCMOS} = 4.9 - 3.5 = 2.9$ V

$N_{ML} = V_{ILBiCMOS} - V_{OLcmos} = 1.0 - 0.1 = 0.6$ V

BiCMOS → CMOS

$NM_H = V_{OHbicmos} - V_{IHcmos} = 4.3 - 3.5 = 0.8$ V

$NM_L = V_{ILcmos} - V_{OLbicmos} = 1.0 - 0.7 = 0.3$ V

3.

If $G_1 = 1$,, $O_1 = \overline{X} + \overline{Y}$

If $G_1 = 0$ and $G_2 = 1$

$$\begin{cases} O_1 = \overline{X} + \overline{Y} \\ O_2 = XY \end{cases}$$

If $G_1 = 0$ and $G_2 = 0$

$$\begin{cases} T = \overline{Q}XY \\ Q^+ = Q\overline{T} + \overline{Q}T = Q(Q + \overline{XY}) + \overline{Q}XY = Q + \overline{Q}XY = Q + XY \end{cases}$$

$O_1 = \overline{X} + \overline{Y}$

$O_2 = Q$

4

J = AB

$K = \overline{A\ B}$

$Q+ = \overline{Q}J + Q\overline{K} = \overline{Q}AB + Q(A + B)$

$Z_i = A \oplus B \oplus Q$