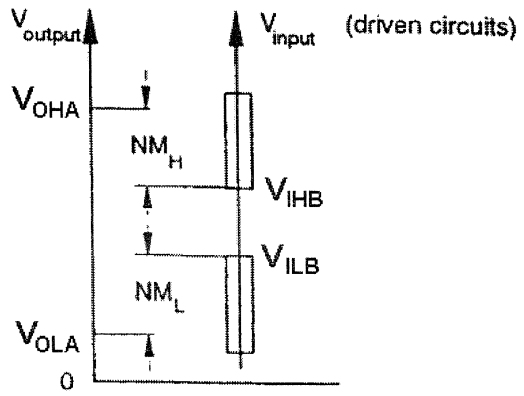
1. (a)



V_{OHA} and V_{OLA} represent respectively:

- the lowest voltage supplied by logic circuit A delivering logic '1', and
- the highest voltage supplied by an output delivering logic '0'

V_{IHB} and V_{ILB} represent respectively:

- the lowest input to B acceptable as logic '1'
- the highest input to B acceptable as logic '0'

If the output of A is connected to the input of B, the noise margins observed in the High and Low states are:

$$NM_H = V_{OHA} - V_{IHB} \qquad \text{and} \qquad NM_L = V_{ILB} - V_{OLA}$$

Both noise margins must be positive if the pair of circuits is to operate consistently. Their magnitude must be δ or greater if superimposed noise of voltage magnitude up to δ is to be rejected.

Note that the voltages V_{OH} and V_{OL} are liable to depend on the magnitude of the current flowing in the corresponding output devices – i.e. they depend on fan-out.

(b) (i) LS-TTL drives CMOS

$N_{MH} = V_{OHls\text{-}ttl} - V_{IHcmos} = 2.5 - 3.5 = -1.0$ V

$N_{ML} = V_{ILcmos} - V_{OLls\text{-}ttl} = 1.0 - 0.4 = 0.6$ V

(ii) CMOS drives LS-TTL

$N_{MH} = V_{OHcmos} - V_{IHls\text{-}ttl} = 4.9 - 2.0 = 2.9$ V

$N_{ML} = V_{ILls\text{-}ttl} - V_{OLcmos} = 0.7 - 0.1 = 0.6$ V

(i) would not work since $N_{MH} < 0$

(ii) will work satisfactorily but note that it will be significantly more susceptible to noise in the low state.

If 20 inputs were driven, the LS-TTL → CMOS margins (for operation assumed to be static or low-frequency) would be unaffected, since the table indicates that CMOS gates draw no input current.

The CMOS → LS-TTL noise margins are liable to be affected.

With the CMOS output high, the CMOS gate must source $20 \times 20 = 400$ μA when delivering '1' to the following 20 gates. This is not a particularly onerous demand.

With the CMOS output low, the CMOS gate must sink a total of $20 \times 0.4 = 8$ mA at its output, from the following inputs. This might be beyond its capacity, or if not, it is liable to raise V_{OLcmos} and erode still further the already poor noise margin in the low state.

In either case, with 20 inputs driven, the additional capacitance will affect the rise/fall time achieved. Full analysis calls for more information about the devices in use and their dimensions, which determine the ability of the output stages to source/sink current to charge/discharge this parasitic load, but drivers implemented in CMOS are often limited cf some bipolar families in terms of available output current.

(c) Considering the BiCMOS design, the input configuration is the same as that of a simple CMOS gate. It is reasonable to deduce that the characteristic input levels will also be the same, and that the input currents would also be 0. Hence CMOS → BiCMOS would give the following margins:

$$N_{MH} = V_{OHcmos} - V_{IHBiCMOS} = 4.9 - 3.5 = 2.9 \text{ V}$$

$$N_{ML} = V_{ILBiCMOS} - V_{OLcmos} = 1.0 - 0.1 = 0.6 \text{ V}$$

In order to estimate the BiCMOS → CMOS combination we need to determine V_{OH} and V_{OL} for the BiCMOS gate, by consideration of the circuit.

With A low, the NMOS transistor MN is **off**. PMOS device MP is **on**, hence current flows into R raising the base potential of Q1 towards V_{CC}. Assuming $V_{BE(on)}$ is 0.7 V, the emitter of Q1 will rise to a maximum of $V_{CC} - 0.7$ V, or 4.3 V in this case.

With A high, MN turns **on**, and MP is **off**. The output discharges initially through the C-E junction of Q2, and via MN and the B-E junction of Q2. Eventually, Q2 turns **off** when its V_{BE} falls to 0.7 V or less, and the rapid discharge of V_{out} through Q2 ceases, and V_{out} can therefore fall no lower than 0.7 V. Hence we can say that V_{out} has characteristic values: $V_{OL} = 0.7$ V and $V_{OH} = 4.3$ V. We can now evaluate the noise margins.

$$NM_H = V_{OHbicmos} - V_{IHcmos} = 4.3 - 3.5 = 0.8 \text{ V}$$

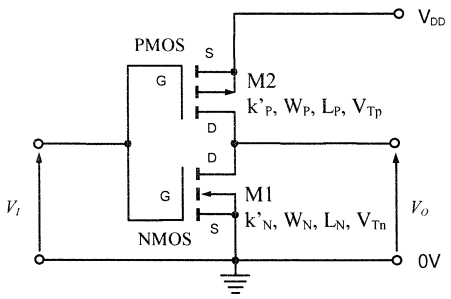
$$NM_L = V_{ILcmos} - V_{OLbicmos} = 1.0 - 0.7 = 0.3 \text{ V}$$

While NM_H is adequate, NM_L is undesirably low. However, the CMOS → BiCMOS combination will work well. Its major advantage is that the enhanced drive capability of the bipolar devices is available, though at the cost of more elaborate foundry processing. This is important in bussed systems like memory arrays where fan-outs may be very large.

The excellent static characteristics of CMOS can be made available in BiCMOS by adding further MOS devices, one in shunt with each of the bipolar devices, and with the common gate connection linked appropriately to the inverter input. The bipolar devices provide fast swings to within 0.7 V of the rails. The parallel MOS devices restore the static levels to very close to V_{CC} and 0 V.

Examiner's note: this question was generally well done, though a surprising number confused the driver gate and the driven gate in their discussion. Quite a few did not attempt part (c). Of those who did, several were not able to reason out what would be the values of V_{OH} and V_{OL} for the BiCMOS gate.

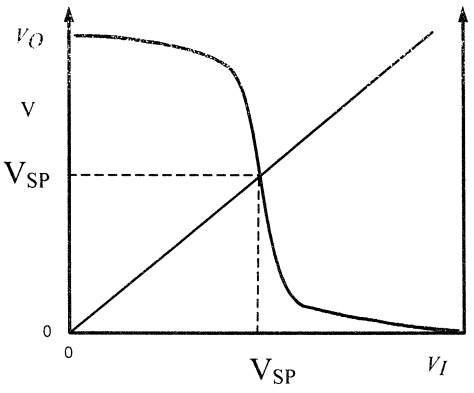
2. (a) (i) As defined V_{SP} is the point at which V_O and V_I are equal, and are expected to lie in the region somewhere between V_{DD} and 0 V.



At this point both MOSFETs are in the *saturation region*, and hence $V_{DS} > V_{GS} - V_T$

Hence the second of the given equations applies. By Kirchhoff, the currents I_{D1} and I_{D2} must be equal, hence:

$$\frac{k'_N}{2}\frac{W'_N}{L_N}(V_{SP}-V_{TN})^2 = \frac{k'_P}{2}\frac{W'_P}{L_P}(V_{DD}-V_{SP}-V_{TP})^2$$



Write $k_N = \frac{k'_N W_N}{L_N}$, and $k_P = \frac{k'_P W_P}{L_P}$; then

$$\frac{k_N}{2}(V_{SP}-V_{TN})^2 = \frac{k_P}{2}(V_{DD}-V_{SP}-V_{TP})^2$$

$$\sqrt{\frac{k_N}{k_P}}(V_{SP}-V_{TN}) = V_{DD}-V_{SP}-V_{TP}$$

Hence, $$V_{SP} = \frac{\sqrt{\frac{k_N}{k_P}}\cdot V_{TN} + (V_{DD}+|V_{TP}|)}{1+\sqrt{\frac{k_N}{k_P}}}$$

noting that V_{TP} is negative.

Let $X = \sqrt{\frac{k_N}{k_P}} = \sqrt{\frac{k'_N W_N L_P}{k'_P L_N W_P}}$, then $V_{SP} = \frac{XV_{TN}+|V_{TP}|+V_{DD}}{1+X}$

It can be seen that with a suitable choice of X (implying ratio of W_P/L_P to W_N/L_N), a range of different values may be obtained for V_{SP}, lying between V_{TN} and $V_{DD} - |V_{TP}|$. However, note that X is proportional to the square root of W/L, so V_{SP} is not a particularly sensitive function of k_N, k_P.

In the inverter, V_{SP} is normally chosen to be at around $V_{DD}/2$:

- to maximise the noise margins N_{MH} and N_{ML}
- this also matches the delay for rising and falling edges at the output, since the pull-up and pull-down conductances are matched.

(ii) The measures that have to be taken to achieve this can be seen by putting $V_{SP} = V_{DD}/2$ in the above equation:

$$\frac{V_{DD}}{2} = \frac{XV_{TN} + V_{TP} + V_{DD}}{1 + X} \quad \text{which we solve for } X$$

$$X = \frac{\frac{1}{2}V_{DD} + V_{TP}}{\frac{1}{2}V_{DD} - V_{TN}}$$

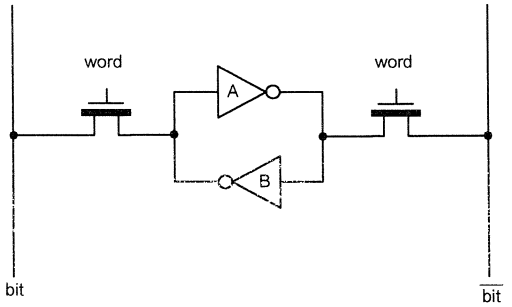
If we can assume, as is often the case, that: $V_{TN} = |V_{TP}|$, then $X = 1$.

Hence, $k'_N \frac{W_N}{L_N} = k'_P \frac{W_P}{L_P}$

i.e. the values of W/L must be chosen to be in the inverse ratio of the devices' k' (or of their mobility μ, assuming constant gate-oxide thickness t_{ox}, since $k' = \mu\varepsilon / t_{ox}$.

Note that the p-channel device is physically larger than the n-channel device, resulting in a loss of symmetry.

(b) The RAM cell consists of a pair of cross-coupled inverters whose inputs may be accessed by means of switching transistors controlled by the **word** signal.



The cell can be in either of two stable states, corresponding to a stored logic '0' or logic '1'.

If inverter B is generating logic '1' that will cause A to output logic '0', which will cause B to output logic '1', so maintaining the original value.

The same argument hold is inverter B is generating logic '0', giving '1' at A's output, so maintaining this continuous set.

Hence the RAM cell may assume only two states and if isolated from external influences it will retain its state while power is applied.

This state may be changed, i.e. data *written*, by driving the vertical **bit** and **bit** lines to new complementary values, and operating the switching transistors by setting the word lines high. The RAM cell inverters must be sufficiently weak (by design) that the bit-line signals can override the signals currently being output by the inverters and switch them into a new state when necessary. It follows also that the driver stages from which the input data is taken must have much greater drive capability, to obtain quick and decisive switching to the new state. Once this has been achieved, the word lines are reset to low, disengaging the switching transistors.

To read out data, both bit-lines are preset to precisely the same voltage, typically the mean of V_{low} and V_{high}. The lines are connected to sensitive comparators, which will initially indicate the equivalence of the signals on the lines. The switching transistors are then enabled. One inverter will drive its corresponding bit-line low, the other high – by a few millivolts. This is because the inverters are designed deliberately with low drive power ('weak'), and the bit-lines represent a substantial capacitive load whose charge is only slightly modified by the influence of the new incremental charges delivered by the two inverters.

The comparator output will then indicate logic '0' or logic '1', according to the sense of the perturbations introduced to the bit-lines by the RAM cell.

To achieve the necessary 'weak' inverters, these are typically implemented using CMOS devices with low values of W/L, leading to low device conductances.

The additional circuit elements required are:

- Address decoder to select a specific horizontal row of cells to be manipulated
- Bank of sensitive comparators (alternatively called sense amplifiers). Design of these is a challenge since they must combine sub-mV sensitivity with high slew rate to read out the data fast.
- Column decoder, to select the output from a specific sense amplifier from the bank, and connect it to the output pin/s; also (for *write* operations) to connect the input data to the chosen set of bit lines.
- *Read/write* control circuitry, which may allow the multiplexed use of a single pin for both input and output

Examiner's note: this two-part question was popular and done quite well. A number failed to notice that at the switching point as defined, V_{GS} for each transistor was equal to V_{DS}; hence each device must be in its saturation mode. Some stumbled on the algebra needed to express V_{SP} in terms of device parameters. The section on the operation of a static memory was done well, though not many could identify more than a couple of the additional circuit elements needed.

3.

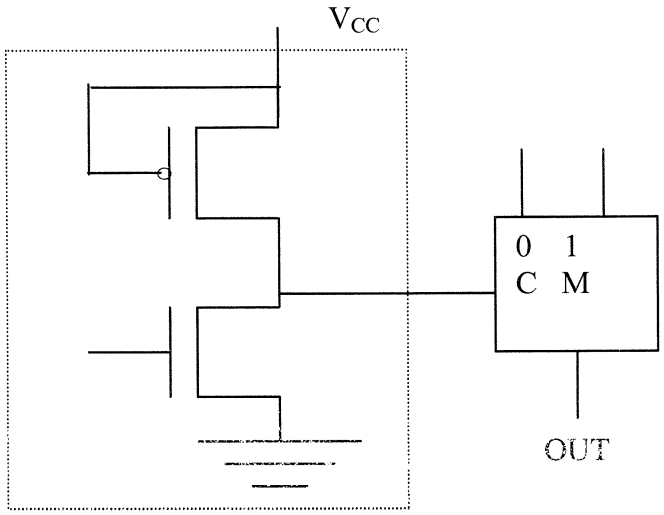
a) **Mask Programmable ROMs - MROMs** -permanently programmed by the manufacturer by simply adding or leaving out diodes or transistors. The customer sends the truth table stating which data should be stored at which address. Expensive, unless a large number is ordered. These memories cannot be reprogrammed. Example : 7488 IC is a 32 words X 8 bits MROM. 5-bit address input will select one of the 32 words.

Programmable ROMs - PROMs - permanently programmed by the customer by burning selectively fuses which act as programmable links in the bipolar or MOS ROMs. Example: 74186 is a 64 words X 8 bits PROM with an access time of 50ns.

Erasable Programmable ROMs - EPROMs the same as PROMS but can be reprogrammed with new data using an ultraviolet light. Data is stored as charge in MOS transistors. Example: 2732 IC can store 4,096 (4k) 8-bit words. - EEPROMs are more advanced EPROMS that can be programmed and reprogrammed using an electrical pulse. Therefore unlike conventional EPROMs, the EEPROMs can be programmed and erased without removing the IC package from the circuit. Example: 2864 IC can store 8,192 (8k) 8-bit words.

b) The control circuits connected to M_1 and M_2 are NMOS inverters.

$G = 0 \Rightarrow C = 1$
$G = 1 \Rightarrow C = 0$



NMOS INVERTER

- If $G_1 = 1 \Rightarrow C_1 = 0 \Rightarrow I/O_2$ is configured as input, $I/O_2 = I$. The input I is selected at the M_1 multiplexer and becomes (or not) an input in the PAL function of G2.

In this case the macro-cell behaves as a single output combinational circuit with 3 inputs X, Y, I. However O1 does not depend on I and therefore is only a function of X and Y. The logic function implemented is:

$$O_1 = \overline{X} + \overline{Y}$$

- If $G_1 = 0$ and $G_2 = 1 \Rightarrow C_1 = 1, C_2 = 0$

B_2 and B_3 are inactive and $I/O_2 = O_2$.

The bistable is bypassed and the macro-cell behaves as a two output combinational network with two inputs.

$$\begin{cases} O_1 = \overline{X} + \overline{Y} \\ O_2 = XY \end{cases}$$

- If $G_1 = 0$ and $G_2 = 0 \Rightarrow C_1 = 1, C_2 = 1$

B_1, B_2 and B_3 are shortcircuits, M_1 and M_2 select the input "1". The cell behaves as a MEALY sequential circuit with two outputs O_1 and O_2. Using reverse method we can work out Q^+ and T.

$$\left.\begin{array}{l} Q^+ = Q \text{ if } T = 0 \\ Q^+ = \overline{Q} \text{ if } T = 1 \end{array}\right\} \Rightarrow Q^+ = Q\overline{T} + \overline{Q}T$$

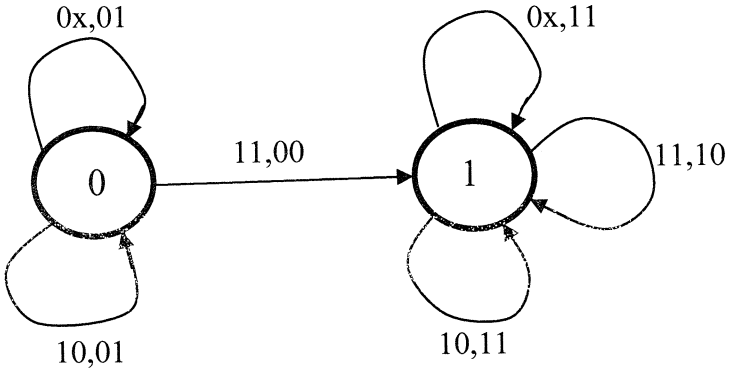
$$\begin{cases} T = \overline{Q}XY \\ Q^+ = Q\overline{T} + \overline{Q}T = Q(Q + \overline{XY}) + \overline{Q}XY = Q + \overline{Q}XY = Q + XY \end{cases}$$

$O_1 = \overline{X} + \overline{Y}$

$O_2 = Q$

State table & state diagram.

Q	Q^+ for Input XY =				O_2O_1 output for XY =			
	00	01	11	10	00	01	11	10
0	0	0	1	0	01	01	00	01
1	1	1	1	1	11	11	10	11



4. a)

A function hazard could be present when more than one input changes at a time -very difficult to analyse. This could be avoided by making sure that only one input (primary or secondary changes at a time).

An essential hazard is caused by a race between an input signal change and an output change. The Essential hazard is only a problem with asynchronous bistable circuits

To remove essential hazards, one can make sure that the primary inputs do not change too fast. For example this is the case in vending machines where between the coins, the time is much greater than the reaction time of the circuit, so that the present states reach the input (secondary input) much faster than the change in the primary inputs.

To remove function hazards one can code intelligently the states so that only one input (primary or secondary) changes at a time, when transiting from one state to the next.

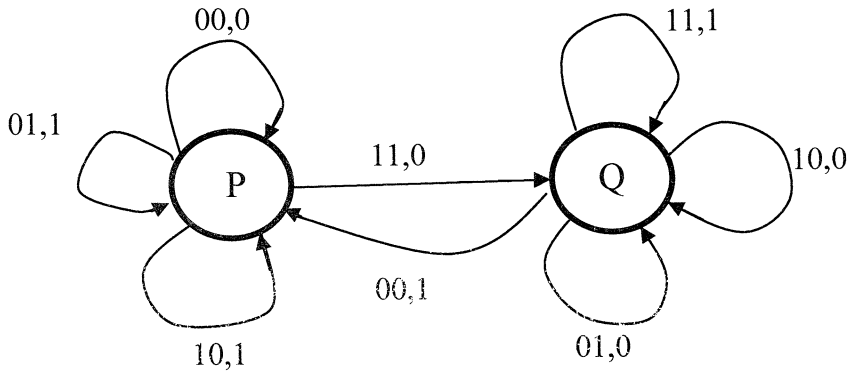
b) The following K-maps can be extracted for Z at the inputs of the bistable:

$J = AB$

$K = \overline{A\ B}$

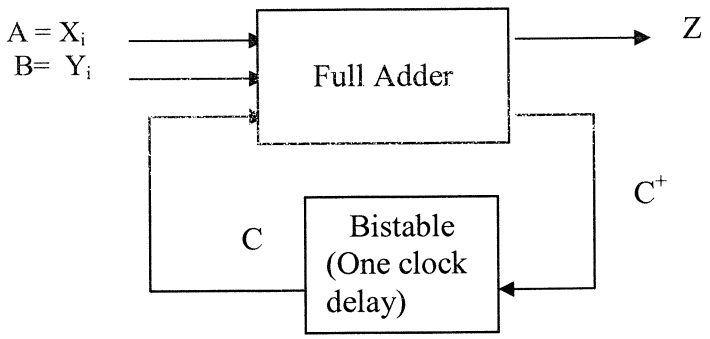
$Q+ = \overline{Q}J + Q\overline{K} = \overline{Q}AB + Q(A+B)$

$Z_i = A \oplus B \oplus Q$



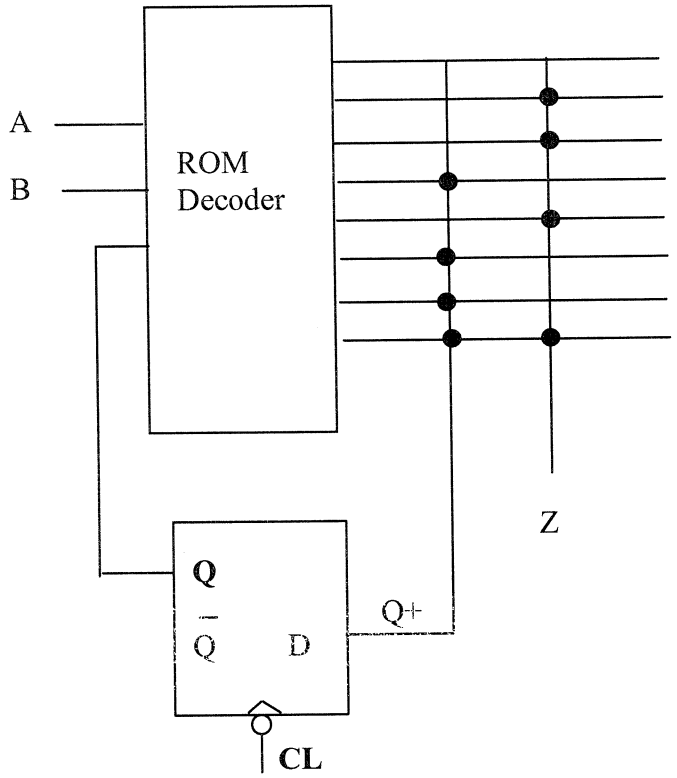
AB	Q	Z	Q^+	JK
00	0	0	0	0x
00	1	1	0	x1
01	0	1	0	0x
01	1	0	1	x0
10	0	1	0	0x
10	1	0	1	x0
11	0	0	1	1x
11	1	1	1	x0

This is an adder. The AB are the inputs Xi Yi (serially entered). Q is the Carry. Q+ is the C+



C = carry bit (present state)
C^+ = next carry bit (next state)

The ROM has 3 addresses – 8 words and 2 bits per word. The total capacity is 8X2 = 16 bits



1(b)

(i) LS-TTL drives CMOS

$N_{MH} = V_{OHls\text{-}ttl} - V_{IHcmos} = 2.5 - 3.5 = -1.0$ V

$N_{ML} = V_{ILcmos} - V_{OLls\text{-}ttl} = 1.0 - 0.4 = 0.6$ V

(ii) CMOS drives LS-TTL

$N_{MH} = V_{OHcmos} - V_{IHls\text{-}ttl} = 4.9 - 2.0 = 2.9$ V

$N_{ML} = V_{ILls\text{-}ttl} - V_{OLcmos} = 0.7 - 0.1 = 0.6$ V

(c) CMOS → BiCMOS would give the following margins:

$N_{MH} = V_{OHcmos} - V_{IHBiCMOS} = 4.9 - 3.5 = 2.9$ V

$N_{ML} = V_{ILBiCMOS} - V_{OLcmos} = 1.0 - 0.1 = 0.6$ V

BiCMOS → CMOS

$NM_H = V_{OHbicmos} - V_{IHcmos} = 4.3 - 3.5 = 0.8$ V

$NM_L = V_{ILcmos} - V_{OLbicmos} = 1.0 - 0.7 = 0.3$ V

3.

If $G_1 = 1$,, $O_1 = \overline{X} + \overline{Y}$

If $G_1 = 0$ and $G_2 = 1$

$$\begin{cases} O_1 = \overline{X} + \overline{Y} \\ O_2 = XY \end{cases}$$

If $G_1 = 0$ and $G_2 = 0$

$$\begin{cases} T = \overline{Q}XY \\ Q^+ = Q\overline{T} + \overline{Q}T = Q(Q + \overline{XY}) + \overline{Q}XY = Q + \overline{Q}XY = Q + XY \end{cases}$$

$O_1 = \overline{X} + \overline{Y}$

$O_2 = Q$

4

J = AB

$K = \overline{A\ B}$

$Q+ = \overline{Q}J + Q\overline{K} = \overline{Q}AB + Q(A + B)$

$Z_i = A \oplus B \oplus Q$