ENGINEERING TRIPOS PART IIA

Thursday 22 April 2010 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1. (a) With the aid of a diagram, show how to determine the noise margins from the characteristic input and output levels V_{IL}, V_{IH}, V_{OL} and V_{OH}. [30%]

(b) Manufacturer's data for 5 volt low-power Schottky TTL (LS-TTL) and CMOS inverters are given in the table below, where I_{IHmax} and I_{ILmax} are the maximum input currents in the high and low logic states respectively.

	V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{IHmax}	I_{ILmax}
CMOS	**1.0 V**	**3.5 V**	**0.1 V**	**4.9 V**	**0**	**0**
LS-TTL	**0.7 V**	**2.0 V**	**0.4 V**	**2.5 V**	**20 μA**	**-400 μA**

Determine the noise margins that will apply when:-

(i) a LS-TTL inverter drives a single CMOS inverter; [10%]

(ii) a CMOS inverter drives a single LS-TTL inverter. [10%]

How would you expect the noise margins to be affected in each case if twenty inputs were driven instead of one? State any assumptions made. [20%]

(c) The LS-TTL inverter of part (b) is replaced with a BiCMOS device from the same manufacturer, for which a simplified circuit is shown in Fig. 1.

Determine the input and output logic levels for the BiCMOS inverter, and the new noise margins in cases (i) and (ii) with the BiCMOS gate substituted for the LS-TTL gate. Comment on the results obtained. [20%]

Suggest how the circuit of Fig. 1 might be adapted to improve its noise performance further. [10%]

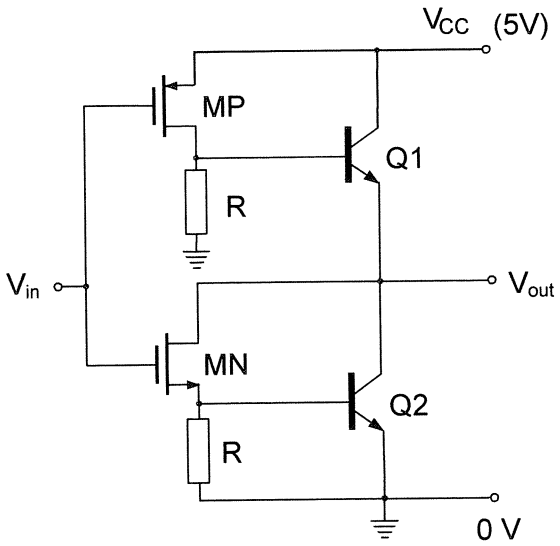

Fig.1

2. (a) In a simple CMOS inverter, the n-channel MOSFET has a threshold voltage V_{TN}, process transconductance k'_N and channel dimensions W_N and L_N. The corresponding parameters for the p-channel MOSFET are V_{TP}, k'_P, W_P and L_P. The power supply voltage is V_{DD}.

(i) Derive an expression for the inverter *switching point voltage* V_{SP}, at which the output voltage and the input voltage are equal. Hence sketch a typical transfer characteristic, clearly showing the switching point V_{SP}. [30%]

(ii) Briefly discuss the measures that must be taken in the design of an inverter to position V_{SP} midway between the supply rails. What are the advantages and disadvantages of doing so? [20%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad V_{DS} \geq (V_{GS} - V_T)$$

where the symbols have their usual significance.

(b) Fig. 2 shows the architecture of a simple static random-access memory cell. Explain briefly the operation of this circuit, and describe the role of the signals *word*, *bit*, and $\overline{bit}$ in allowing data to be written and read. [25%]

(i) What special measures need to be taken in the design of the inverters A and B to allow the circuit to work correctly? [10%]

(ii) Outline the nature of the additional circuit elements necessary to allow the cell to be interfaced to an external circuit. [15%]

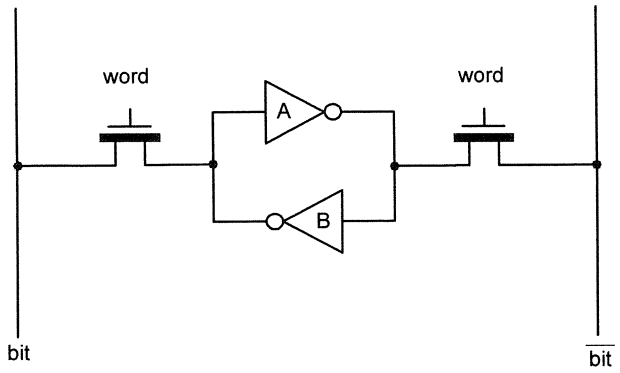

Fig. 2

3. (a) Compare the Mask Programmable Read Only Memories (MROMs), Programmable Read Only Memories (PROMs) and Erasable Programmable Memories (EPROMs) . [20%]

(b) A macro-cell, part of a complex combinational/sequential PAL has been programmed as shown in Fig. 3. The binary gate signals on the n-channel MOSFET switches, G1 and G2, control the 2-1 multiplexers and the non-inverting tri-state buffers B1, B2 and B3. The tri-state buffers act as short-circuits when the control is 'high' and open-circuits when the control is 'low'. There are two main inputs labelled X and Y and one output labelled O1. The I/O2 pin can be configured either as an extra input or the second output of the macro-cell. The bistable is of 'toggle' type (T).

(i) Describe the multiple operation of the macro-cell and find the logic functions for all combinations of the gate signals G1 and G2. [50%]

(ii) Derive the state table and the state diagram if the macro-cell is operated as a state-machine. What type of architecture has the state-machine and why ? [30%]

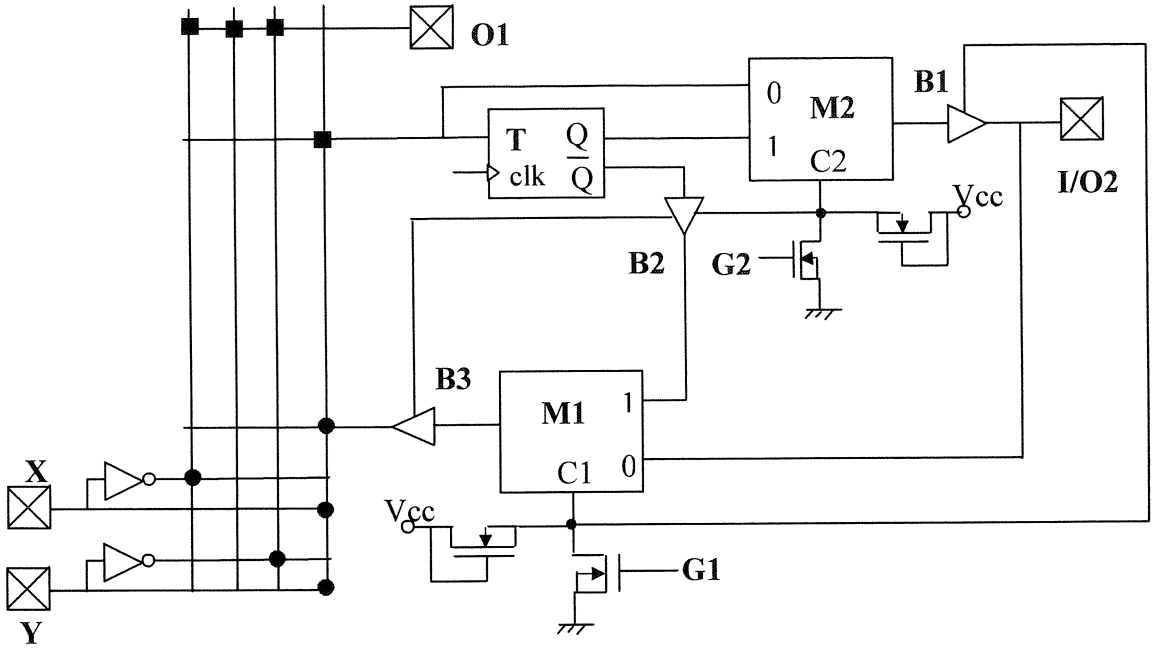

Fig. 3

4 (a) Briefly explain function hazards and essential hazards. Describe a practical example of a design of an asynchronous circuits free of function and essential hazards. [20%]

(b) By using the reverse engineering method analyse the logic circuit shown in Fig. 4. where A, B are the inputs and Z is the output. Derive the state table and the state diagram. [30%]

Draw a meaningful simplified block diagram of the circuit. What specific function does the circuit perform ? [20%]

Implement the same circuit using a read only memory (ROM) and a D bistable, instead of logic gates and the J-K bistable. What is the size of the ROM needed ? [30%]

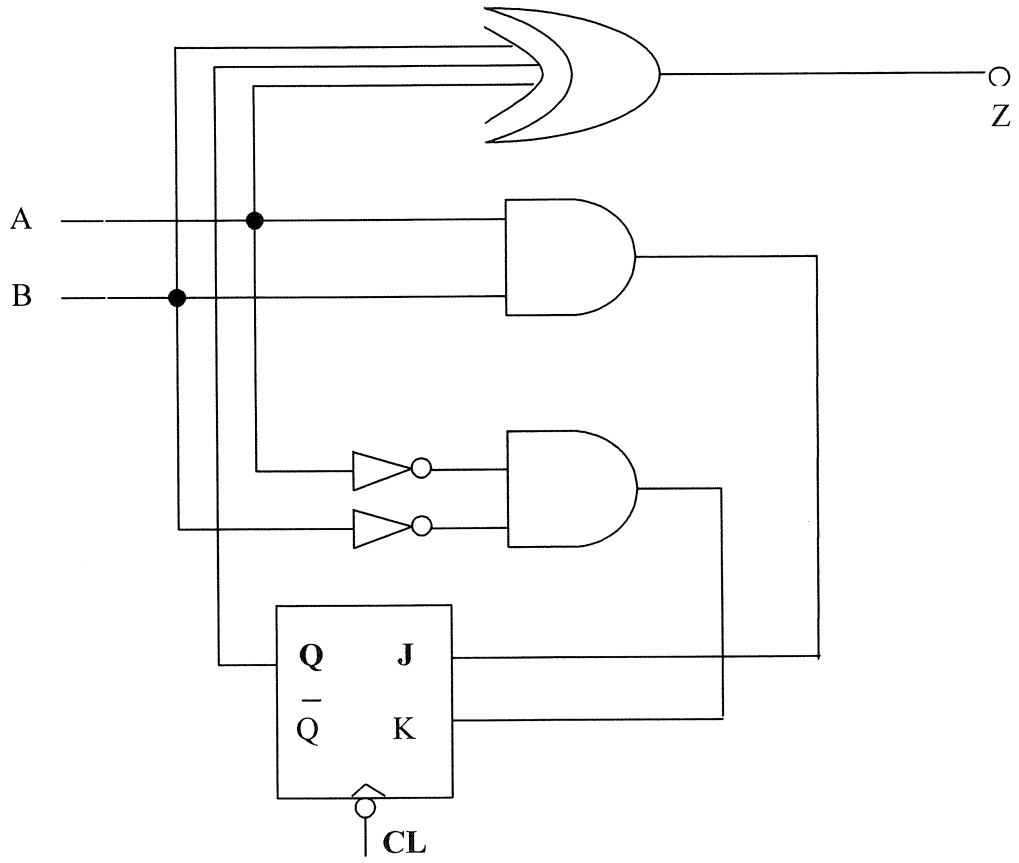

Fig. 4

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1(b)

(i) LS-TTL drives CMOS

$N_{MH} = V_{OHls\text{-}ttl} - V_{IHcmos} = 2.5 - 3.5 = -1.0$ V

$N_{ML} = V_{ILcmos} - V_{OLls\text{-}ttl} = 1.0 - 0.4 = 0.6$ V

(ii) CMOS drives LS-TTL

$N_{MH} = V_{OHcmos} - V_{IHls\text{-}ttl} = 4.9 - 2.0 = 2.9$ V

$N_{ML} = V_{ILls\text{-}ttl} - V_{OLcmos} = 0.7 - 0.1 = 0.6$ V

(c) CMOS → BiCMOS would give the following margins:

$N_{MH} = V_{OHcmos} - V_{IHBiCMOS} = 4.9 - 3.5 = 2.9$ V

$N_{ML} = V_{ILBiCMOS} - V_{OLcmos} = 1.0 - 0.1 = 0.6$ V

BiCMOS → CMOS

$NM_H = V_{OHbicmos} - V_{IHcmos} = 4.3 - 3.5 = 0.8$ V

$NM_L = V_{ILcmos} - V_{OLbicmos} = 1.0 - 0.7 = 0.3$ V

3.

If $G_1 = 1$,, $O_1 = \overline{X} + \overline{Y}$

If $G_1 = 0$ and $G_2 = 1$

$$\begin{cases} O_1 = \overline{X} + \overline{Y} \\ O_2 = XY \end{cases}$$

If $G_1 = 0$ and $G_2 = 0$

$$\begin{cases} T = \overline{Q}XY \\ Q^+ = Q\overline{T} + \overline{Q}T = Q(Q + \overline{XY}) + \overline{Q}XY = Q + \overline{Q}XY = Q + XY \end{cases}$$

$O_1 = \overline{X} + \overline{Y}$

$O_2 = Q$

4

J = AB

$K = \overline{A\ B}$

$Q+ = \overline{Q}J + Q\overline{K} = \overline{Q}AB + Q(A + B)$

$Z_i = A \oplus B \oplus Q$