Numerical answers 3B2 - 2011

1.

$$I_D = 4.5k$$

$$t_{SAT} = 0.13\frac{C_L}{k}$$

$$t_{NON-SAT} = 2.64\frac{C_L}{3k}$$

$$t_{fall} = t_{SAT} + t_{NON-SAT} = \frac{C_L}{3k}(0.39 + 2.64)$$

$$t_{fall} = \frac{15\times10^{-12}}{3\times1.2\times10^{-5}}\times 3.03 = 1.26\ \mu s$$

2

$$\tau = C\times(3 - V_{SW})/I_{LEAK} \quad = \quad 2.1\ \text{ms}$$

The proportion of clock cycles lost to refresh and not available for regular read/write is:

$$\frac{1/2\times10^{-3}}{10^8} \quad = \quad \frac{500}{10^8} \quad = \quad \text{1 cycle in 200,000, a negligible overhead.}$$

The total leakage current for a 1 Mbit memory would be $50 \times 10^{-12} \times 10^6$, or 50 μA. At a supply voltage of 3 V this corresponds to a power loss of 150 μW.