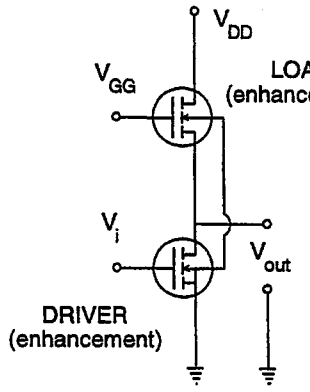
1. (a) **Resistor loads in MOS logic**

Resistive loads are a feature of nMOS logic. Resistors can be manufactured in integrated form using polysilicon (as used for gate electrodes) or doped silicon (as used for source/drain), with the dimensions chosen to achieve the required resistance. Resistors implemented on silicon occupy very considerable area. In order to minimise power dissipation, relatively high values of resistor may be required, and as resistivities of available materials are relatively low, these need to be laid out as long serpentine structures and consume disproportionate amounts of space – the load resistor may require 10-100 times the space of the driver.

While for several years nMOS process technology offered considerable performance advantages over competing bipolar technologies of the day, it suffers from key fundamental disadvantages:

- Continuous dissipation of power in the load in one state (0 output for nMOS)
- Difficulty in obtaining a fully restored logic '0', leading to poor noise margins
- Passive pull-up to Vdd means relatively slow switching for output 0-1.
- Power dissipation, speed, and noise margins are inextricably interdependent

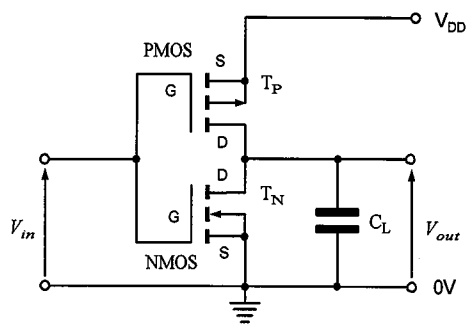


In circuits where resistive loads are unavoidable (for example, pseudo-nMOS logic or linear circuits), an appropriately biased MOSFET may be used as load, with the gate returned to a fixed bias to obtain an appropriate channel conductance, approximating the behaviour of a resistor. Static and dynamic logic gate performance are now a sensitive function of the dimensions of load and driver FET. Use of a depletion-mode FET with grounded gate is also possible.

Although the resistive characteristic is far from ideal (non-linear), such devices are much more compact.

In CMOS, the passive resistor load is replaced by an active complementary device driven by the input signal. Its much superior characteristics of CMOS have led to its ubiquitous use in logic circuits.

(b) The circuit for the CMOS inverter is shown.



Note that since both devices have the sam e k and $|V_T|$, delays and r ise/fall times are the same for both transitions, 0-1 and 1-0.

We shall assume that (i) equations 1 and 2 can be used as given, (ii) that the input changes abruptly, and (iii) there is no load a part from the x pF capacitance; (iv) V_{OH} and V_{OL} for the inverter are V_{DD} and 0 V.

The 10-90% fall time corresponds to the output m aking its transition from 1 to 0. This is caused by the input switching from 0 to 1; the abrupt transition means that T_P switches off instantly, and we need only consider the discharging of C_L thru T_N. We now consider the

changing conditions for this device. At the instant T_N begins to conduct, V_{out} is 4 V, V_{GS}= 4 V and V_{DS} is 4 V. T_N is clearly in its saturation region, in which it will remain until V_{DS} falls to $V_{GS} - V_T$, or until V_{out} rises to 3 V. The remainder of the fall happens with T_N in its non-saturation region.

We are interested in the 10-90% fall time, i.e. the interval between V_{out} passing through 3.6 V and 0.4 V. This interval comprises two periods that have to be found:

t_{SAT} - C_L discharges from 3.6 V to 3.0 V (T_N in saturation region – Eqn 2)
$t_{NON\text{-}SAT}$ - C_L charges from 3.0 V to 0.4 V (T_N in non-sat'n region – Eqn 1).

For t_{SAT}, T_N in its saturation region acts as a constant current source with current:

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 = \frac{k}{2}(4-1)^2 = 4.5k$$

The time t_{SAT} taken to discharge C_L through 0.6 V at constant current is:

$$t_{SAT} = C_L \times 0.6 / I_D = 0.6C_L / 4.5k = 0.13\frac{C_L}{k}$$

As V_{out} reaches 3 V, T_N enters its non-saturation region and the current thereafter depends on its V_{DS} and hence on V_{out}. The expression for I_D (NMOS case) is:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right], \text{ and noting that } V_{DS} = V_{out}, \text{ we can substitute:}$$

$$I_D = \frac{k}{2}\left[2(4-1)V_{out} - V_{out}{}^2\right] = \frac{k}{2}\left(6V_{out} - V_{out}^2\right) = \frac{k}{2}(V_{out})(6 - V_{out})$$

Using $\frac{dV_{out}}{dt} = -\frac{I_D}{C_L}$ we can write: $\int_0^{t_{NON-SAT}} dt = t_{NON-SAT} = -\frac{2C_L}{k}\int_3^{0.4} \frac{dV_{out}}{(V_{out})(6 - V_{out})}$

Note that a positive drain current gives a negative rate-of-change for V_{out}.

This can be simplified using partial fractions to: $-\frac{2C_L}{k}\int_3^{0.4} \frac{1}{6}\left(\frac{1}{V_{out}} + \frac{1}{6 - V_{out}}\right) dV_{out}$

$$\text{Hence } t_{NON-SAT} = \frac{C_L}{3k}\left[\ln\frac{6 - V_{out}}{V_{out}}\right]_3^{0.4} = \frac{C_L}{3k}\left(\ln\left(\frac{5.6}{0.4}\right) - \ln\left(\frac{3}{3}\right)\right) = 2.64\frac{C_L}{3k}$$

The total fall time is the sum of the intervals in the saturation and non-saturation regions.

Hence a suitable expression is: $t_{fall} = t_{SAT} + t_{NON-SAT} = \frac{C_L}{3k}(0.39 + 2.64).$

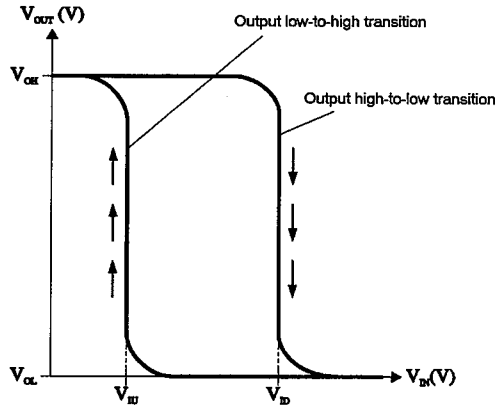
Substituting values, $t_{fall} = \frac{15 \times 10^{-12}}{3 \times 1.2 \times 10^{-5}} \times 3.03 = 1.26\ \mu s$

t_{rise} and t_{fall} may be equalised by designing the parameter W/L for each transistor in the inverse ratio of the mobility μ of the material from which its channel is made. Thus:

$$W_P / L_P = \frac{\mu_N}{\mu_P} \cdot W_N / L_N$$

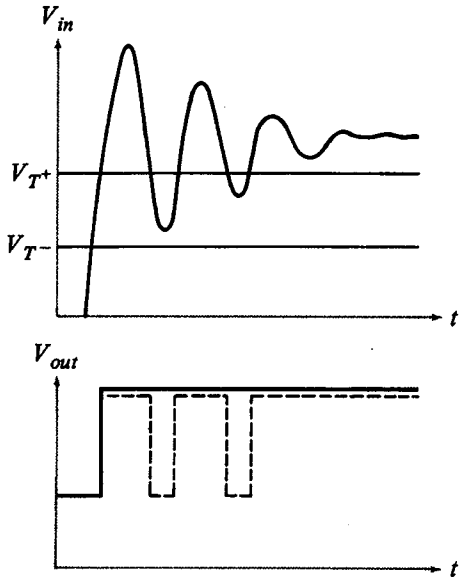
2. (a) In the conventional CMOS logic inverter, the low-to-high and high-to-low transitions occur at the same input voltages. In the Schmitt gate the phenomenon of HYSTERESIS is exhibited, where the L-H and H-L transitions occur at different input voltages.

The voltage transfer characteristic exhibits a hysteresis loop as shown in the Schmitt inverter characteristic.



- V_{OUT} makes its H-L transition when the *rising* input voltage exceeds
  $V_{IN} = V_{ID}$
- V_{OUT} makes its L-H transition when the *falling* input voltage drops below
  $V_{IN} = V_{IU}$
- The condition $V_{ID} > V_{IU}$ must hold.
- V_{ID}–V_{IU} is referred to as the hysteresis of the gate.

If the input V_{IN} exhibits noise, the hysteresis characteristic is helpful in cleaning up and conditioning the signal for digital processing. This may be used to advantage in line receiver applications. Because of the fast transition times in high speed digital systems, and the intrinsic parasitic series inductance and parallel capacitance of a signal wire, the voltage pulse seen at the end of a long line might be as below (characteristic ringing).



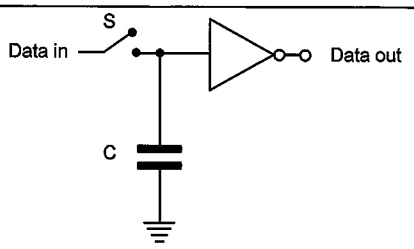
The output of a simple inverter with switch level V_{ID} would exhibit additional spurious pulses.

Setting the switching level to V_{IU} would not necessarily solve the problem as it might cause triggering on other noise events.

The output of a Schmitt inverter with thresholds V_{ID}, V_{IU}, as described would alleviate this effect in a single step, as required.

The Schmitt inverter can also be used for converting non-digital signals (e.g. sine waves) to a digital pulse train.

(b) MOS technologies offer great flexibility , high density, low consumption, high speed, excellent scalability, and ability to integrate complex support functions. Formerly bipolar technologies offered greater speed, but dimensionally scaled MOS memories have now surpassed bipolar technologies in this sense as well.

(c) Let us assume that the inverter switches at VSW = VDD/2, that is, 1.5 V. If C loses half its charge, having been set to logic 1, it will (incorrectly) read out a value interpreted at logic 0. The leakage current is fixed at 50 pA for every cell (a convenient simplification)	

Hence the time τ taken to discharge to 1.5 V is:

$$\tau = C \times (3 - V_{SW}) / I_{LEAK} \quad = \quad \frac{70 \times 10^{-15} \times (3 - 1.5)}{50 \times 10^{-12}} \quad = \quad 2.1 \text{ ms}$$

The capacitor must be refreshed at least this often. In fact, every read or write serves the purpose of refreshing the memory cell being read from/written to, but the routine pattern of reads and writes may not necessarily be sufficiently regular to ensure all cells are properly refreshed. As a result, dedicated hardware is provided to intersperse refresh cycles among the normal read/write transactions.

If the refresh is performed at 2 ms intervals and occupies one clock cycle at 100 MHz, the proportion of clock cycles lost to refresh and not available for regular read/write is:

$$\frac{1/2 \times 10^{-3}}{10^{8}} \quad = \quad \frac{500}{10^{8}} \quad = \quad \text{1 cycle in 200,000, a negligible overhead.}$$

However, additional hardware is needed to achieve this. In most memories this will comprise a clocked counter, coupled with arbitration logic to avoid the risk of refresh and other accesses coinciding in any memory cell.

(d) To determine power dissipation, we assume that all cells are at logic '1', and have identical leakage.

Hence the total leakage current for a 1 Mbit memory would be $50 \times 10^{-12} \times 10^{6}$, or 50 μA. At a supply voltage of 3 V this corresponds to a power loss of 150 μW.

Note that it is more likely that a proportion of cells will be in the 0 state, and we are not told what leakage current flows under these circumstances. However, it is possible that the currents in the two states might be of comparable magnitude.

In practice, this represents the static dissipation of the memory array. To this would have to be added contributions due to changes of state, primarily arising from repeated charge and discharge of the storage and other capacitances. This source of power loss is proportional to frequency of operation, and to V_{DD}^2.

By today's standards, 1Mbit is a moderately small memory!

3. (a) The design rules to implement a combinational circuit free of static or dynamic hazards using only NAND gates are:

(i) All the adjacent 1-terms in the K-map of of the function should be covered by a common 1-term

(ii) There should be no 1-terms that contain both a variable and its complement.

(b) The block diagram is shown below (other schematic variants can also be correct):

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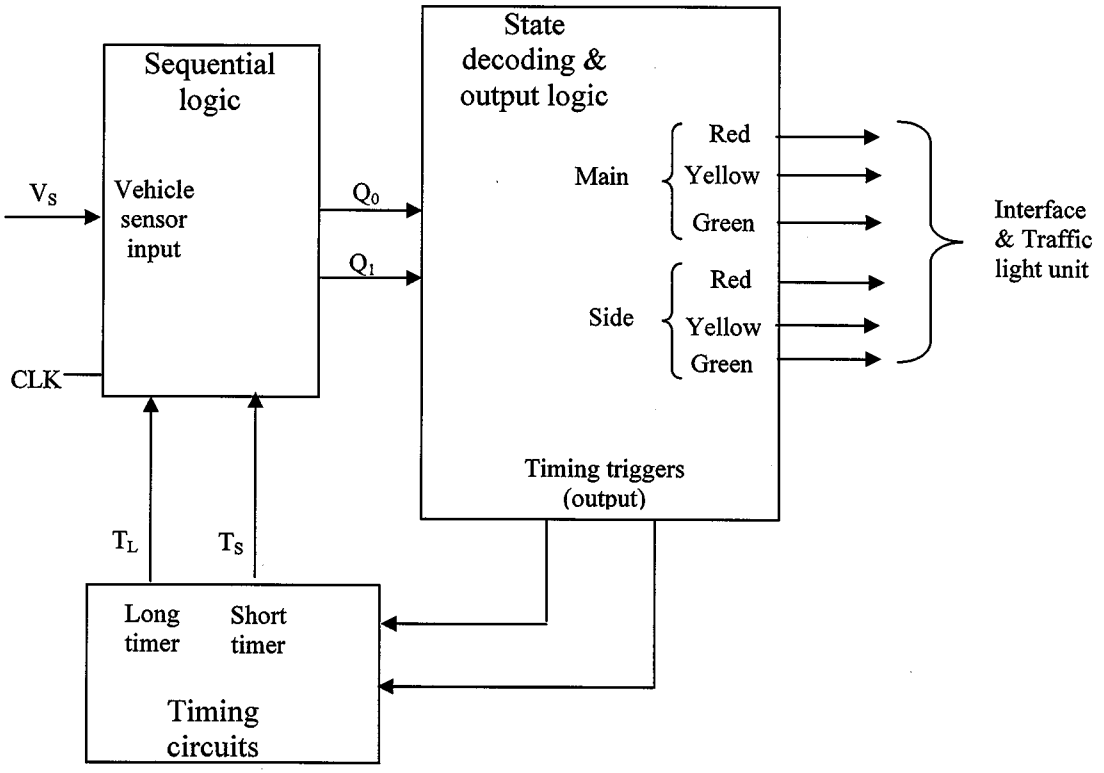


[20%]

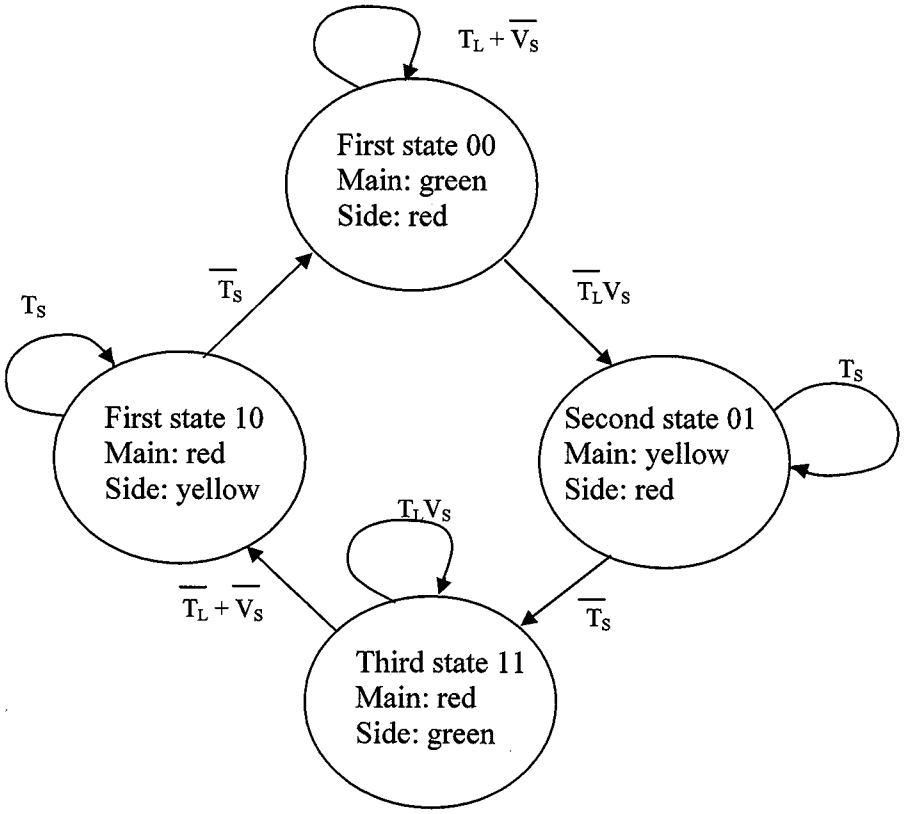
First state. The Gray code for this state is 00. The main street light is green and the side street light is red. The system remains in this state for at least 20 seconds when T_L is 1 or as long as there is no vehicle on the side road, $V_s=0$. The system goes to the next state when the 20 s timer is off (T_L becomes 0) and there is a vehicle on the side street ($V_s=1$).

Second state: Gray code is 01. The main street light is yellow and the side street is red. The system remains in this state for 3 seconds when the short timer is on (T_s is 1) and goes to the next state when T_s becomes 0 (after 3seconds – counted by the timing circuit).

Third state: Gray code is 11. The main street light is red and the side street light is green. The system remains in this state when T_L is 1 and there is a vehicle on the side road,

V_s=1. The system goes to the next state when the 20 s timer is off (T_L becomes 0) or there is no vehicle on the side street (V_s=0), whichever comes first.

Fourth state: Gray code is 10. The main street light is red and the side street is yellow. The system remains in this state for 3 seconds when the short timer is on (T_s is 1) and goes to the first state when T_s becomes 0 (after 3 seconds – counted by the timing circuit).



Present state	Next state for the inputs T_S,T_L,V_S							
	000	001	011	010	100	101	111	110
00	00	01	00	00	00	01	00	00
01	11	11	11	11	01	01	01	01
11	10	10	11	10	10	10	11	10
10	00	00	00	00	10	10	10	10

[30%]

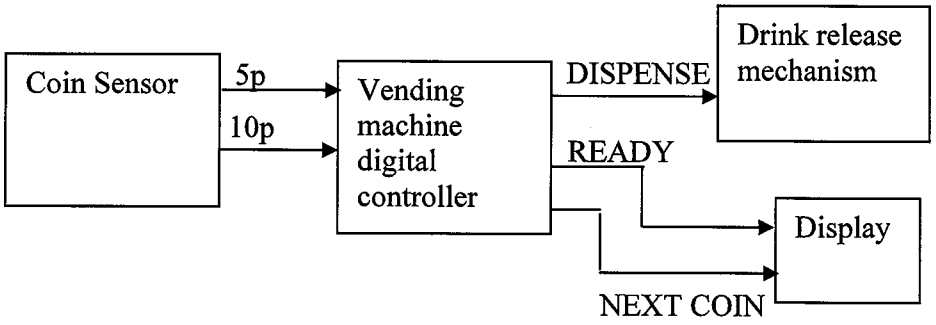
Present state	Light outputs						Trigger outputs	
	MR	MY	MG	SR	SY	SG	Long	Short
00	0	0	1	1	0	0	1	0
01	0	1	0	1	0	0	0	1
11	1	0	0	0	1	0	0	1
10	1	0	0	0	0	1	1	0

[30%]

4. (a) The Quine-McClusky tabular method is based on building lists with adjacent blocks containing the same number of 'High' variables. By comparing, and if appropriate, combining each term from one block with the block below we build subsequent lists. The terms that did not combine in each list (including the last) are termed 'Prime Implicants' (PIs). The 'Prime Implicant table' is formed of the PIs and the original terms of the logic function. The idea is to select the minimal and the simplest PIs which cover all the original terms. This can be done by visual inspection or by a formalised method.

(b) If the logic function is not in a canonical form (or not brought to a canonical form) it is difficult to deal with terms that have fewer variables. Such terms may be introduced in the second or subsequent lists but this results in missing the chance to combine parts of them (canonical components of such terms) with other terms from the first list (or previous lists) and thus the method does not always deliver an optimal solution.The vending machine is shown below:

[20%]



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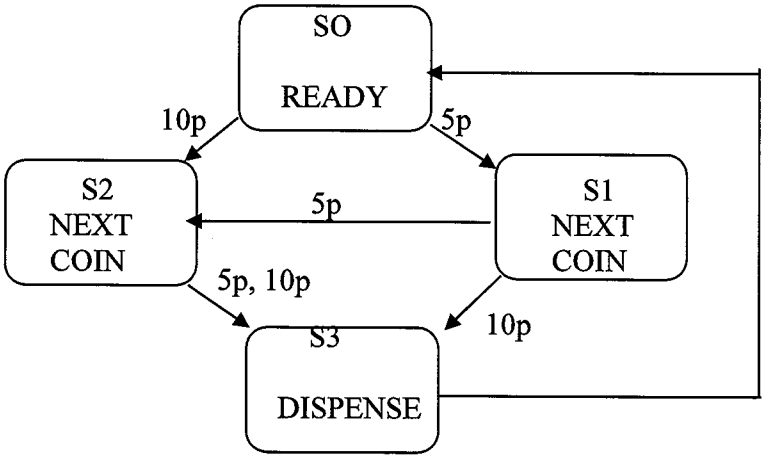
The state diagram is shown below. There are 4 states. Since the outputs are only dependent on the state, this is a Moore state diagram and will lead to a Moore circuit. If no coins are received the machine remains in the same state. Also note that two coins cannot be received at the same time.



The state table is shown below

Present state		Next state for 5p10p= 00	01	11	10	DISPENSE	READY	NEXT COIN
SO	00	00	10	-	01	0	1	0
S1	01	01	11	-	10	0	0	1
S3	11	00	00	-	00	1	0	0
S2	10	10	11	-	11	0	0	1

[30%]

D_1

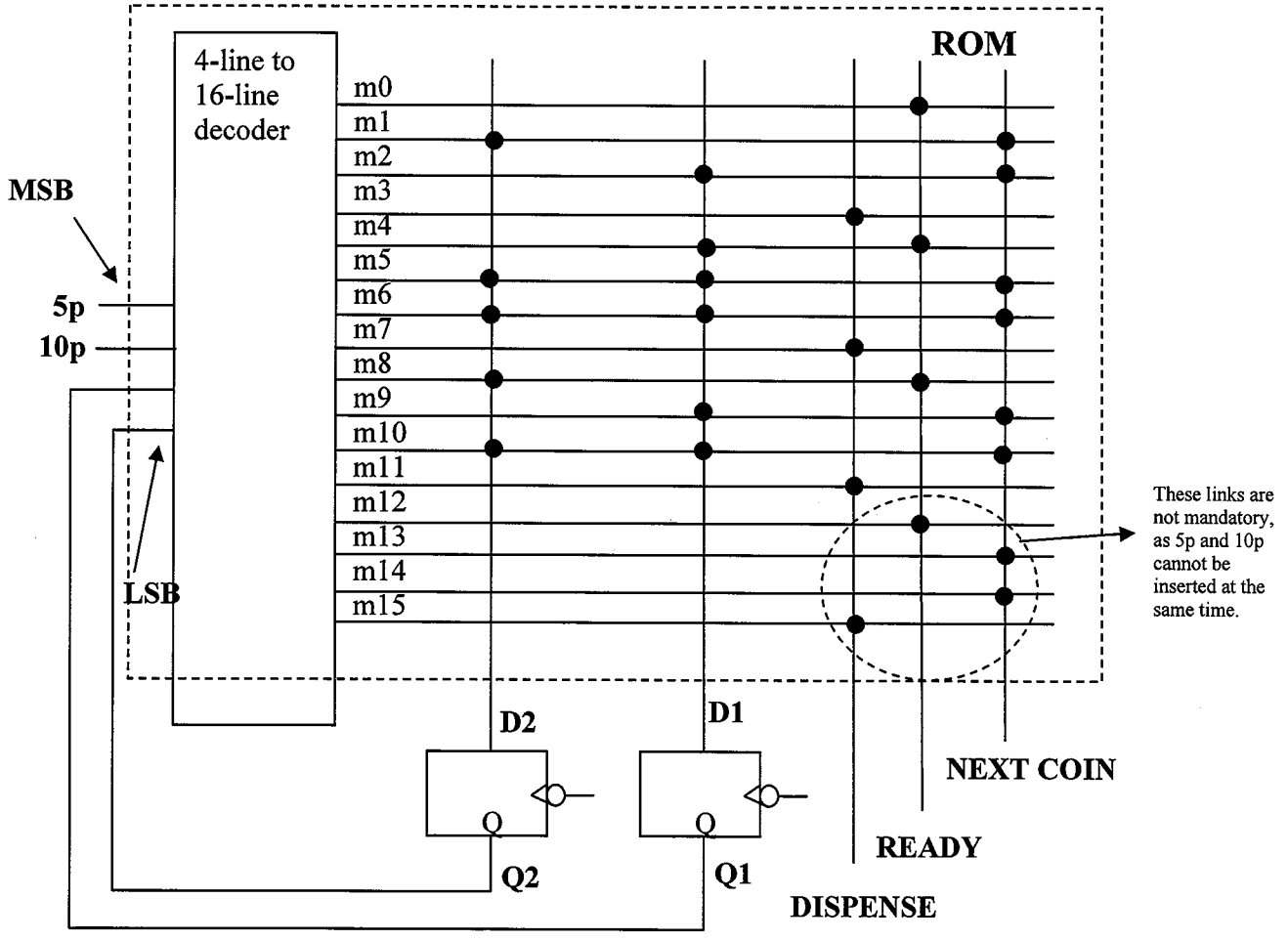
Q_1Q_2 \ 5p 10p	00	01	11	10
00	0	1	x	0
01	0	1	x	1
11	0	0	x	0
10	1	1	x	1

D1= SUM(2,4,5,6,9,10)

D_2

Q_1Q_2 \ 5p 10p	00	01	11	10
00	0	0	x	1
01	1	1	x	0
11	0	0	x	0
10	0	1	x	1

D2= SUM(1,5,6,8,10)



[30%]

Numerical answers 3B2 - 2011

1.

$$I_D = 4.5k$$

$$t_{SAT} = 0.13\frac{C_L}{k}$$

$$t_{NON-SAT} = 2.64\frac{C_L}{3k}$$

$$t_{fall} = t_{SAT} + t_{NON-SAT} = \frac{C_L}{3k}(0.39 + 2.64)$$

$$t_{fall} = \frac{15\times10^{-12}}{3\times1.2\times10^{-5}}\times 3.03 = 1.26\ \mu s$$

2

$$\tau = C\times(3 - V_{SW})/I_{LEAK} \quad = \quad 2.1\ \text{ms}$$

The proportion of clock cycles lost to refresh and not available for regular read/write is:

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