ENGINEERING TRIPOS PART IIA

Thursday 28 April 2011 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

Final version

1. (a) What are the advantages and disadvantages of using MOS transistors rather than resistors as the load element in MOSFET logic gates? Your answer should refer to space occupied, noise margins, speed of operation and power consumption, as well as any other features you consider important. [30%]

(b) A complementary MOS (CMOS) inverter is run from a 4 V supply. It is fabricated from two transistors each with a device transconductance of k. The threshold voltages of the NMOS and PMOS devices are 1 V and –1 V respectively. The output terminal is connected to a capacitive load C_L.

(i) Derive an expression for the 10-90% fall time at the output, assuming that the input voltage changes abruptly. State any other assumptions made. [40%]

(ii) If $k = 1.2 \times 10^{-5}$ A V^{-2} and the external load C_L is 15 pF, determine the 10-90% fall time. [10%]

(iii) What steps must be taken by the designer of the circuit to ensure that the two MOSFETs have identical transconductance values? [20%]

You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad \text{for} \quad V_{DS} < (V_{GS} - V_T)$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad \text{for} \quad V_{DS} \geq (V_{GS} - V_T)$$

where the symbols have their usual significance.

2. (a) Briefly describe the principle of operation of a Schmitt inverter. Sketch a graph depicting a typical voltage transfer characteristic for a Schmitt inverter, and explain the significance of the output high-to-low transition and output low-to-high transition. How might such a gate be used to reconstruct a digital signal from a waveform degraded by interference or by propagation through a long cable? What advantages would this be expected to give? [30%]

(b) Discuss why the vast majority of read-write memory devices available today are based on MOS rather than bipolar technology. [20%]

(c) A dynamic read-write memory cell is modelled as a switch S, a storage capacitor C and an inverter as shown in Fig. 1. The storage capacitor has a capacitance of 60 fF and is charged to 3 V to represent logic 1. Logic 0 is represented by 0 V.

(i) If the leakage current to ground may be regarded as constant at 50 pA, how often must the cell be refreshed? State any assumptions made. [20%]

(ii) If access to the memory is controlled by a 100 MHz clock, estimate the proportion of clock cycles lost through the need to refresh. [10%]

(iii) Estimate the power dissipation due to this effect in a memory circuit of 1 Mbit capacity based on this technology. [20%]

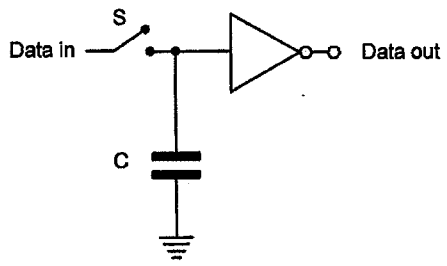


Fig. 1

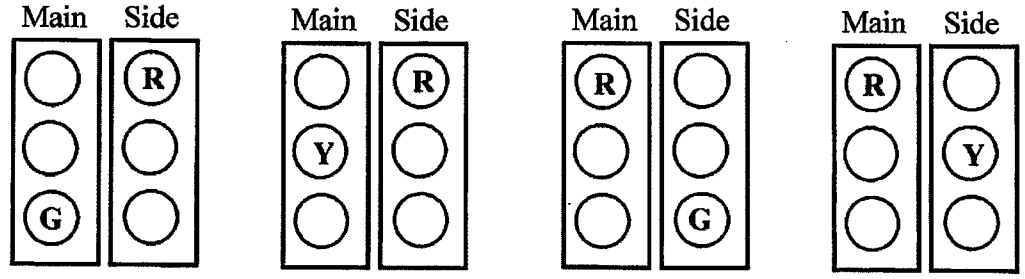
3. (a) State the design rules to implement a combinational circuit free of static or dynamic hazards using only NAND gates. [20%]

(b) A logic controller is required to control a simplified traffic light at the crossroad of a busy main street and an occasionally used side street. The main street is to have a green light for a minimum of 20 seconds or as long as there is no vehicle on the side street. The side street is to have a green light until there is no vehicle on the side street or for a maximum of 20 seconds. There is to be a 3 seconds caution light (yellow) between changes from green to red on both the main street and the side street. These requirements with all the states you need to consider are illustrated in Fig. 2 where R=Red, Y=Yellow and G = Green.

(i) Develop a schematic block diagram of the system indicating the logic blocks, the timing circuit block and the inputs and outputs. [20%]

(ii) Describe the state diagram using Grey coding for a Moore architecture. [30%]

(iii) Derive the output table. There is no need to develop or show the actual circuit implementation. [30%]



First state: 20 s minimum or as long as there is no vehicle on side street

Second state: 3 s

Third state: 20 s maximum or until there is no vehicle on side street

Fourth state: 3 s

Fig. 2

4. (a) In the Quine-McClusky tabular method give the definition of 'prime implicants' and briefly explain the use of the 'prime implicant table'. Explain why, if a logic expression is not in a canonical form or is not brought to a canonical form, the Quine-McClusky tabular method may not always give an optimally simplified solution. [20%]

(b) A simple vending machine dispenses a drink for 15 pence in coins. The machine has a single coin slot and accepts 10p and 5p coins one at a time. Outputs must be generated to operate the drink dispensing mechanism (DISPENSE) and indicator lights signalling that the machine is ready for operation (READY) and in operation waiting for the next coin (NEXT COIN).

(i) Draw schematically the architecture of the vending machine as a block diagram. [20%]

(ii) Derive and draw the state diagram and state table showing the allocation of states. [30%]

(iii) Draw the circuit implementation of the vending machine using D bistables and a ROM. [30%]

END OF PAPER

Numerical answers 3B2 - 2011

1.

$$I_D = 4.5k$$

$$t_{SAT} = 0.13\frac{C_L}{k}$$

$$t_{NON-SAT} = 2.64\frac{C_L}{3k}$$

$$t_{fall} = t_{SAT} + t_{NON-SAT} = \frac{C_L}{3k}(0.39 + 2.64)$$

$$t_{fall} = \frac{15\times10^{-12}}{3\times1.2\times10^{-5}}\times 3.03 = 1.26\ \mu s$$

2

$$\tau = C\times(3 - V_{SW})/I_{LEAK} \quad = \quad 2.1\ \text{ms}$$

The proportion of clock cycles lost to refresh and not available for regular read/write is:

$$\frac{1/2\times10^{-3}}{10^8} \quad = \quad \frac{500}{10^8} \quad = \quad \text{1 cycle in 200,000, a negligible overhead.}$$

The total leakage current for a 1 Mbit memory would be $50 \times 10^{-12} \times 10^6$, or 50 μA. At a supply voltage of 3 V this corresponds to a power loss of 150 μW.