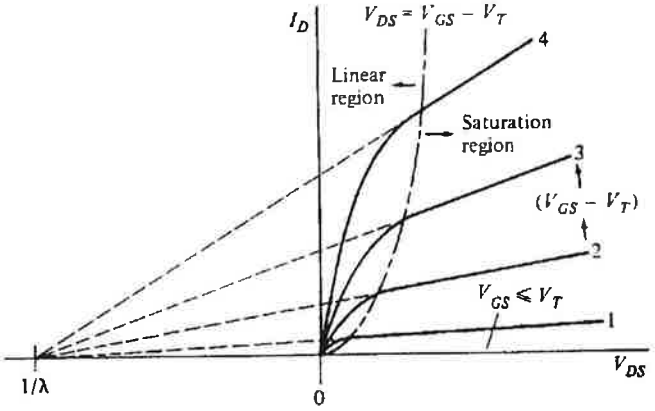
1. For MOS transistors, saturation describes the region of operation where the channel is pinched off near the drain. This typically corresponds to high values of $V_{DS}$. The necessary condition is (for n-channel) :

$V_{DS} > V_{GS} - V_T$

If $V_{DS} = V_{GS} - V_T$, pinch-off happens right at the drain. As $V_{DS}$ increases, the pinch-off region advances progressively towards the source. To a first approximation, $I_D$ remains unchanged as $V_{DS}$ increases, and the device acts as a constant current source/sink. In fact, as $V_{DS}$ increases, the resultant shortening of the channel (channe length modulation) slightly enhances the conductance, and brings about a gradual increase in $I_D$.




The near constant current is a useful characteristic in linear circuits.

Also, a FET connected with D and G shorted together is by definition in saturation, and may be used as a load in place of a resistor – it also occupies much less space.

n-channel enhancement mode MOSFET

Vertical scale greatly exaggerated to emphasise channel-length modulation effect

(ii) For bipolar devices, saturation is observed when the base potential $V_{BE}$ causes a large collector current to flow. Assuming a load is connected between collector and supply, $V_{CE}$ falls to a low limiting value $V_{CEsat}$ (typically ~0.2 V), and is definitely less than the value of $V_{BE}$ (under these conditions about –0.8 V).

In this situation $V_{CB} < 0$ (NPN), and the c-b junction becomes forward biased. The collector injects electronic charge into the base, accounting for some excess base current.

In bipolar, saturation gives a clearly defined low $V_{CE}$ with a typically higher-than-usual $V_{BE}$ and $I_B$, and a large $I_E$. The low $V_{CE}$ can be used to define a logic level (as in saturated-mode bipolar logic). The excess charge stored in the base has to be removed before the device can leave saturation and stop conducting, This takes o(50ns) and limits switching speed available with saturated bipolar logic. A bipolar device in this state can also be used as an effective *low side switch* as its power dissipation is low.

(b) In this circuit, for T2, $V_{DS} \equiv V_{GS}$ since D is shorted to G. Hence by definition $V_{DS} > V_{GS} - V_T$, so T2 is known to be in its saturation mode. We cannot know for certain the state of T1, since Vout is at this point unknown, but we shall assume that, because $V_{GS}$ is high, $V_{DS}$ will likely be low, with that device in its non-saturation state. We must verify this at the end.

Hence we use the first of the given equations for T1, the second for T2

Assuming no current is drawn from the output, we equate $I_{DS}$ for T1 and T2.

$$I_{D1} = \frac{k_1}{2}\left[2\left(V_{GS_1} - V_T\right)V_{OUT} - V_{OUT}^2\right] = I_{D_2} = \frac{k_2}{2}\left(V_{GS_2} - V_T\right)^2$$

For T1, $V_{GS1} = 5$V. for T2, $V_{GS2} = V_{DD} - V_{OUT} = 10 - V_{OUT}$

$$\frac{80}{2}\left(2(5-1)V_{OUT}-V_{OUT}^2\right) = \frac{15}{2}(10-V_{OUT}-1)^2$$

$$128V_{OUT}-16V_{OUT}^2 = 243-54V_{OUT}+3V_{OUT}^2$$

$$19V_{OUT}^2-182V_{OUT}+243 = 0 \qquad \text{Solving,}$$

$V_{OUT} = \dfrac{182\pm\sqrt{182^2-4\times19\times243}}{38}$. Hence $V_{OUT}$ = 4.79 ± 3.18 V

= 1.61 or 7.97 V. The second root is not consistent with T1 in non-saturation. Hence the first root applies, and $V_{OUT}$ = 1.61 V

(c) σ is defined as $I_C/h_{FE}\,I$ . σ describes the degree of saturation of the bipolar circuit. σ = 1 means the circuit is not saturated, σ = 0.1 means it is heavily saturated.

If σ = 0.15, then the base current drive is 1/0.15 × that required to sustain collector current $I_C$, and the circuit is well into saturation, so $V_{CE}$ may be taken as $V_{CEsat}$.

Hence $I_C = \dfrac{V_{CC}-0.1}{R_L} = \dfrac{4.9}{3000} =$ 1.63 mA

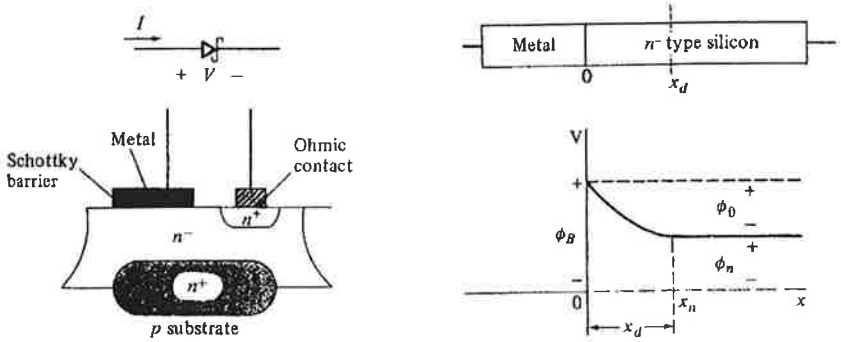
And $I = \dfrac{I_C}{\sigma h_{FE}} = \dfrac{1.63\times10^{-3}}{0.15\times50} =$ 217 μA

If $V_{Esat}$ = 0.7 V, we may apply KVL to get $V_B$, which is given by :

$$V = I\,R + V_{Esat} = 217\times10^{-6}\times 5000 + 0.7 = 1.79\text{ V}$$

*Examiner's note: this question was popular and quite well done. Some lost marks through not distinguishing clearly between saturation in the MOS and bipolar cases. In the quantitative section, a number failed to carry out the all-important test to verify whether the chosen root of the equation satisfied the conditions for non-saturation of the driver device.*

2. A Schottky (or Schottky-barrier) diode is made by creating a microscopically clean contact between a lightly-doped n-type semiconductor and certain metals.

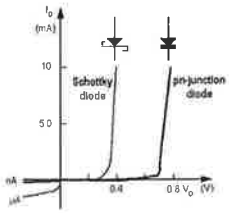



A characteristic **potential barrier** $\phi_B$ at the metal-semiconductor interface impedes the flow of electrons from metal to semiconductor. The height of the barrier depends only on the two materials used, but is typically 0.6 - 0.8 V. A depletion region is set up in the semiconductor close to the interface. However, electrons in the semiconductor far from the interface may acquire energy sufficient to surmount the barrier and escape to the metal, giving rise to a reverse leakage current. The SBD diode is a "majority carrier" semiconductor device. Only n-type carriers (mobile electrons) play a significant role in normal operation of the device. No slow, random recombination of n- and p- type carriers is involved, so the SBD can cease conduction faster than a p-n junction diode. Advantage of this feature is taken in Schottky bipolar logic circuits.
Detailed analysis gives a result similar to that for the p-n junction diode.

$$I = I_0\left(e^{V/V_\theta} - 1\right)$$

**Reverse bias** - adds to the height of the barrier that has to be surmounted
- increases the width of the depletion region

**Forward bias** - reduces the barrier
- electrons flow more easily from semiconductor to metal

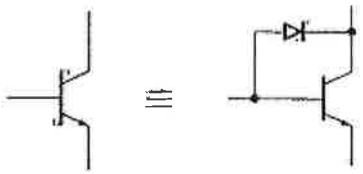



The value of $I_0$ is much larger than that for the p-n junction diode.

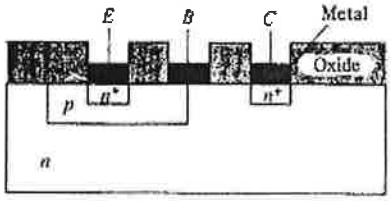
$I_{0(schottky)} \sim 10^{-11}$ A, $I_{0(Si\text{-}Si)} \sim 10^{-15}$ A

Thus a S-B diode of given size typically has a *lower forward voltage* than a comparable p-n junction diode operating at the same forward current.

When a p-n junction is saturated, there is a surplus of minority carriers injected across the junction. In order for the device to stop conducting these minority carriers must be removed. Since the removal depends substantially on diffusion, it has a long time constant, from 10-1000 ns. This leads to slow switching.



The effect can be alleviated if the p-n device can be prevented from entering saturation. The performance of gates in TTL - which depend on saturation - can be much improved by use of *Schottky transistors*.




A SBD is connected across base-collector junction of each bipolar transistor liable to saturate, forming a *clamp* and preventing the junction becoming forward biased by more than approximately 0.5 V, insufficient to allow substantial charge to accumulate in the base region. Schottky transistors switch from saturation about 3-5 times faster than unmodified TTL.

(c) This circuit is similar to the basic diode-transistor logic circuit that evolved to give TTL and its derivatives, enhanced by the use of Schottky barrier diodes at the input. A further key difference is that the output uses a complementary pair, with an active pull-up based on a p-channel transistor.

The circuit is a 2-input NAND, that is, the output will be low if both inputs are high.

The circuit should have the advantage over a more conventional saturating bipolar design of being faster because of the high conductance path provided by T2; also, in the steady-state, the current in the output chain will be lower because one of T1 or T2 will be off while the gate output lies at a regular logic level. However, where good dynamic performance is sought, the relative slowness of switching in pnp bipolar devices will make it difficult to achieve a really fast gate.

*Examiner's note: most candidates were able to describe the SBD satisfactorily, but a number gave rather sketchy accounts of the use of the SBD to speed up saturating bipolar logic. The analysis of the 'novel' circuit in (c), not covered in lectures, was done well by a few, but not all observed that the use of SB diodes should enhance the switching characteristic wrt DTL using p-n diodes.*

3. A multiplexer with two control lines P, Q as described, gives an output

$$D_0\overline{P}\,\overline{Q} + D_1\overline{P}Q + D_2P\overline{Q} + D_3PQ$$

We may connect two of the input variables ABCD to P and Q, and must then choose appropriate functions of the other variables to the data inputs D0, D1, D2 and D3. The clearest way to do this is to plot a K-map. The choice of which variables to connect as control inputs will affect the form of the map and may determine the simplicity or otherwise of the result. Let us assume A maps to P and B maps to Q.

| PQ=AB / CD | 00 D0 | 01 D1 | 11 D3 | 10 D2 |
|---|---|---|---|---|
| 00 | 1 | 0 | 0 | 0 |
| 01 | 1 | 1 | 0 | 1 |
| 11 | 0 | 1 | 1 | 0 |
| 10 | 0 | 1 | 1 | 1 |

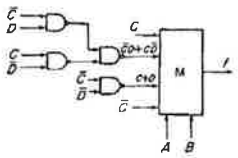
The four-variable K-map can now be divided into four four-cell, two-variable maps, and simplification now takes place within the confines of these two-variable maps (in shaded regionss)

The data line inputs obtained are:

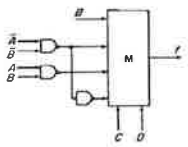
$$D_0 = \overline{C} \qquad D_1 = C + D$$

$$D_2 = \overline{C}D + C\overline{D} \qquad D_3 = C$$

and the corresponding circuit is shown in (a) below.



(a) Circuit diagram with AB as controls



(b) Simpler result with CD as controls

This approach does not guarantee the simplest possible approach, even if the maps are minimised. Other choices of control variables need to be examined to see if there might be a simpler solution (AC, AD, BC, BD, CD are all alternatives). If the variables CD are used to control the MUX, a simpler result is obtained – see (b).

(b) In the Moore sequential network, the Primary Outputs, Z, are a function of the present states Q only, i.e. Z = f(Q). In the Mealy sequential network, the POs are a function of both the present states Q and the Primary Inputs X, hence: Z = f(X,Q).

The choice of the network is one of convenience and personal preference, but the Mealy model is more general. The most significant operational difference between the two is that when a set of inputs is applied to the Moore network, the resulting outputs do not appear until after the clock pulse causes the bistables to change state.

(c) First construct the State Table.

| Current State | Next State | | | | |
|---|---|---|---|---|---|
| $G_3G_2G_1G_0$ | $G_3'G_2'G_1'G_0'$ | *J3 K3* | *J2 K2* | *J1 K1* | *J0 K0* |
| 0 0 0 0 | 0 1 0 0 | 0 X | 1 X | 0 X | 0 X |
| 0 1 0 0 | 0 1 0 1 | 0 X | X 0 | 0 X | 1 X |
| 0 1 0 1 | 0 1 1 1 | 0 X | X 0 | 1 X | X 0 |
| 0 1 1 1 | 0 1 1 0 | 0 X | X 0 | X 0 | X 1 |
| 0 1 1 0 | 1 1 1 0 | 1 X | X 0 | X 0 | 0 X |
| 1 1 1 0 | 1 1 1 1 | X 0 | X 0 | X 0 | 1 X |
| 1 1 1 1 | 1 1 0 1 | X 0 | X 0 | X 1 | X 0 |
| 1 1 0 1 | 1 1 0 0 | X 0 | X 0 | 0 X | X 1 |
| 1 1 0 0 | 1 0 0 0 | X 0 | X 1 | 0 X | 0 X |
| 1 0 0 0 | 0 0 0 0 | X 1 | 0 X | 0 X | 0 X |

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | X | X |
| 01 | **X** | 0 | X | **X** |
| 11 | **X** | 0 | X | **X** |
| 10 | **X** | 1 | X | **X** |

*J3*

| G3G2 / G1G0 | 0 0 | 0 1 | 1 1 | 1 0 |
|---|---|---|---|---|
| 00 | 1 | X | X | 0 |
| 01 | **X** | X | X | **X** |
| 11 | **X** | X | X | **X** |
| 10 | **X** | X | X | **X** |

*J2*

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | **X** | 1 | 0 | **X** |
| 11 | **X** | X | X | **X** |
| 10 | **X** | X | X | **X** |

*J1*

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 0 | 0 |
| 01 | X | X | X | **X** |
| 11 | X | X | X | **X** |
| 10 | X | 0 | 1 | **X** |

*J0*

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | 0 | 1 |
| 01 | **X** | X | 0 | **X** |
| 11 | **X** | X | 0 | **X** |
| 10 | **X** | X | 0 | **X** |

*K3*

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | 0 | 1 | X |
| 01 | **X** | 0 | 0 | **X** |
| 11 | **X** | 0 | 0 | **X** |
| 10 | **X** | 0 | 0 | **X** |

*K2*

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | X |
| 01 | **X** | X | X | **X** |
| 11 | **X** | 0 | 1 | **X** |
| 10 | **X** | 0 | 0 | **X** |

*K1*

| G3G2 / G1G0 | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | X |
| 01 | **X** | 0 | 1 | **X** |
| 11 | **X** | 1 | 0 | **X** |
| 10 | **X** | X | X | **X** |

*K0*

$$J_3 = G_1.\overline{G_0} \qquad K_3 = \overline{G_2}$$

$$J_2 = \overline{G_3} \qquad K_2 = G_3.\overline{G_1}.\overline{G_0}$$

$$J_1 = \overline{G_3}.G_0 \qquad K_1 = G_3.G_0$$

$$J_0 = G_1.G_3 + \overline{G_3}.\overline{G_1}.G_2 \qquad K_0 = G_3.\overline{G_1} + \overline{G_3}.G_1$$

*Examiner's note: this question produced some good answers, but a minority could not cope with a 4:1 multiplexer, and tried to convert it into an 8:1 design. Those who drew out the K-map rapidly found a convenient solution, and a couple hit on the simpler result shown above. In section (c) most were able to derive the state & state transition tables, though some missed out a transition and produced incorrect K-maps.*

4. (a) Procedure for Quine-McCluskey:

(i) Systematically examine each term of the given logic expression and express it in canonical form.

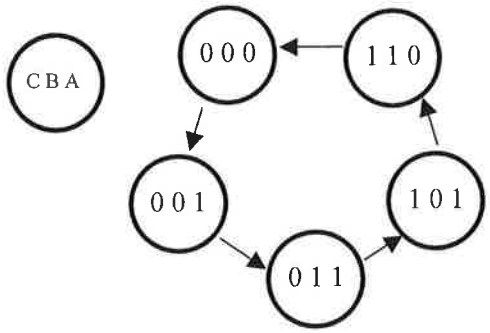
(ii) Construct a list of all the on-set minterms (including any 'don't care' terms) in the form of binary numbers. Group terms with the same number of 'high' variables in blocks and assemble the list for convenience in order of increasing count of 'high' variables.

(iii) Build a set of derived lists based on the result of (i), by combining terms from adjacent blocks that differ by one variable only, and transfer such pairs to the next list. Formally, the terms satisfy the expression: PQ + PQ' = PQ, where P represents a product of a set of literals, and Q is a single variable. Q is transformed into a dash '-' in the new list. All possible pairs of minterms should be compared and combined. Once the second list is complete, the process is repeated to construct a third, fourth, .. until no further terms will combine. Any remaining terms which did not combine in any of the lists are Prime Implicants.

(iv) Construct a Prime Implicant Table, in which the Prime implicants are tabulated against the original on-set ('don't cares' are not included at this stage)

(v) The final solution is based on the minimal and simplest set terms that will 'cover' the original expression.

(b)




**Toggle type bistable excitation table**

| Q | Q' | T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |

| Current State | Next State | T inputs | | |
|---|---|---|---|---|
| *C B A* | *C' B' A'* | $T_C$ | $T_B$ | $T_A$ |
| 0 0 0 | 0 0 1 | 0 | 0 | 1 |
| 0 0 1 | 0 1 1 | 0 | 1 | 0 |
| 0 1 1 | 1 0 1 | 1 | 1 | 0 |
| 1 0 1 | 1 1 0 | 0 | 1 | 1 |
| 1 1 0 | 0 0 0 | 1 | 1 | 0 |

From the state table:

| A \ CB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | X | 1 | X |
| 1 | 0 | 1 | X | 0 |

$T_C = B$

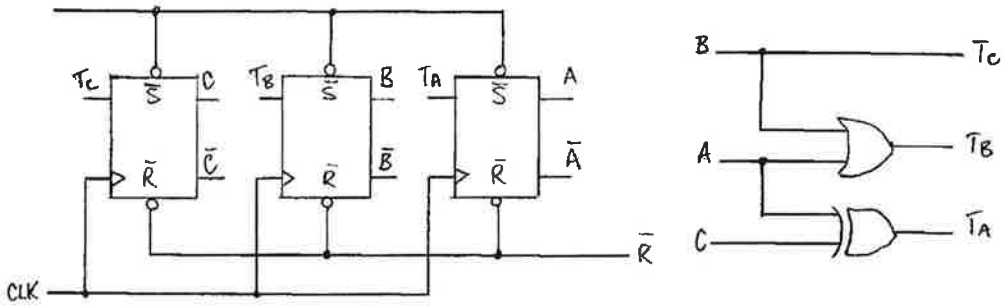
| A \ CB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | X | 1 | X |
| 1 | 1 | 1 | X | 1 |

$T_B = A + B \text{ or } A + C$

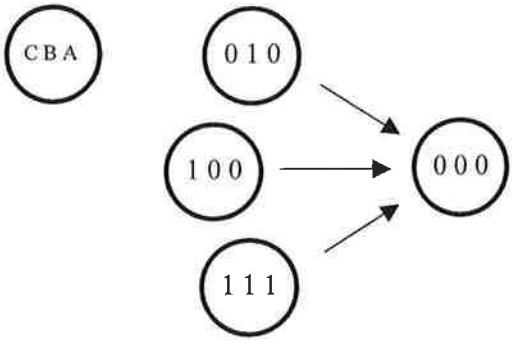
| A \ CB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | X | 0 | X |
| 1 | 0 | 0 | X | 1 |

$T_A = A'C' + AC = A \oplus C$

Diagram




(c) The unused states can be made to advance to zero by use of the asynchronous reset signal provided on each T-type.

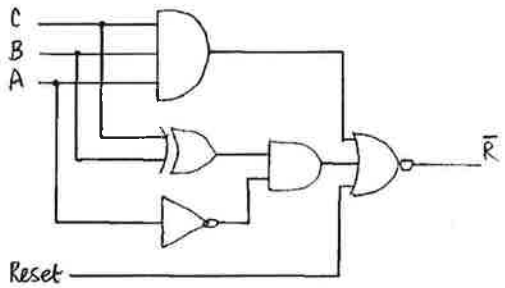



| A \ CB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |

$R = ABC + \overline{A}\,\overline{B}C + \overline{A}B\overline{C}$

$R = \overline{A}(B \oplus C) + ABC$

Diagram




*Examiner's note: Accounts of the Quine-McCluskey procedure varied widely, although it is well covered in lecture notes and several books. A small number of candidates appeared to have misunderstood the operation of a T-type bistable and came up with asynchronous designs.*

**Answers**

1. (b) 1.61 V (c) 1.79 V

2.

3. If AB controls the MUX: $D_0 = \overline{C}$, $D_1 = C + D$, $D_2 = \overline{C}D + C\overline{D}$, $D_3 = C$

$J_3 = G_1.\overline{G_0}$ $\quad K_3 = \overline{G_2}$

$J_2 = \overline{G_3}$ $\quad K_2 = G_3.\overline{G_1}.\overline{G_0}$

$J_1 = \overline{G_3}.G_0$ $\quad K_1 = G_3.G_0$

$J_0 = G_1.G_3 + \overline{G_3}.\overline{G_1}.G_2$ $\quad K_0 = G_3.\overline{G_1} + \overline{G_3}.G_1$

4. $T_C = B$, $T_B = A + B$, $T_A = \overline{A}.\overline{C} + A.C = A \oplus C$