ENGINEERING TRIPOS PART IIA

Tuesday 8 May 2012 2.30 to 4

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Describe what is meant by the term *saturation* when it refers to:

(i) MOS transistors,

(ii) bipolar transistors

in the context of logic gates made from these devices. Your answer should clearly indicate instances where saturation can be used to advantage in the design of logic gates, and where it is disadvantageous. [30%]

(b) Fig. 1(a) shows a logic gate based on MOS transistors M1 and M2 whose device transconductances k_1 and k_2 are shown.

Calculate the logic 'low' output voltage V_{OL} for this gate assuming the threshold voltage for both transistors V_T = 1 V, and V_I = 5 V when $V_{OUT} = V_{OL}$. You may assume the following equations for the drain current I_D flowing in a MOSFET:

$$I_D = \frac{k}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad \text{for} \qquad V_{DS} < (V_{GS} - V_T);$$

$$I_D = \frac{k}{2}(V_{GS} - V_T)^2 \qquad \text{for} \qquad V_{DS} \geq (V_{GS} - V_T),$$

where k is the device transconductance parameter, and other symbols have their usual meanings. Indicate clearly which device, if any, is in its saturation mode. [40%]

(c) For the bipolar transistor inverter circuit shown in Fig. 1(b), the value of σ is 0.15. Explain the significance of this value. If the values of $V_{CE\,sat}$ and $V_{BE\,sat}$ for the device are 0.1 V and 0.7 V respectively, calculate for this circuit the input voltage V_B that would produce this value of σ. [30%]

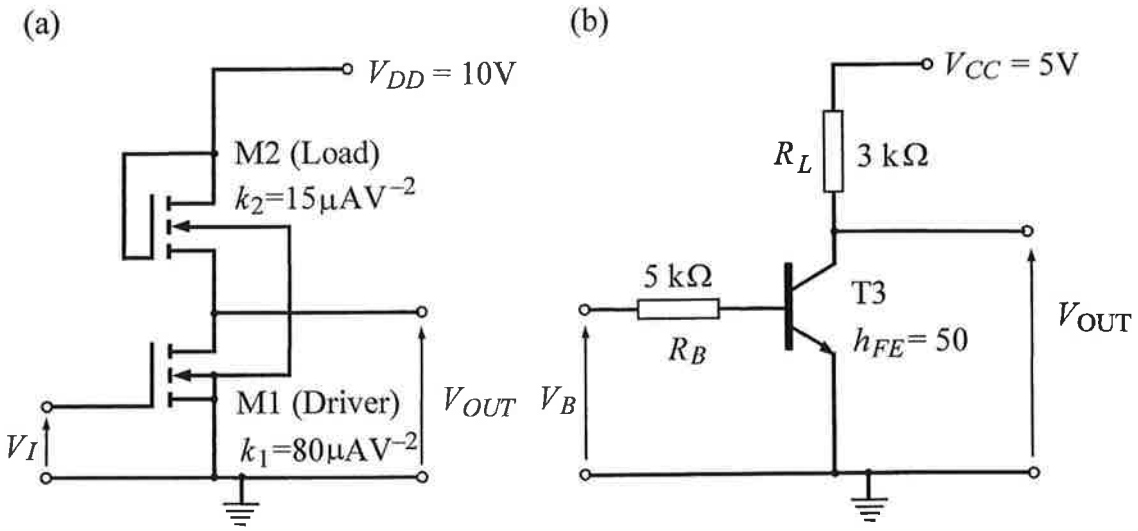
(a)
V_{DD} = 10V
M2 (Load)
k_2=15μAV^{-2}
M1 (Driver)
k_1=80μAV^{-2}
V_I
V_{OUT}
(b)
V_{CC} = 5V
R_L
3 kΩ
5 kΩ
R_B
T3
h_{FE}= 50
V_B
V_{OUT}

Fig. 1

2 (a) With the aid of appropriate diagrams describe the construction and electrical characteristics of the *Schottky barrier diode*, emphasising how they differ from those of the silicon p-n junction diode. [30%]

(b) Describe how advantage has been taken of the Schottky barrier diode in the development of faster forms of integrated bipolar logic, and explain how the speed improvement was achieved. [30%]

(c) Fig. 2 shows a basic 2-input NAND gate proposed in a research paper published a few years ago. D_1, D_2 and D_3 are Schottky barrier diodes, and T1 and T2 are silicon bipolar transistors. Describe the operation of the circuit and discuss its expected advantages and disadvantages in comparison with other principal families of logic. [40%]

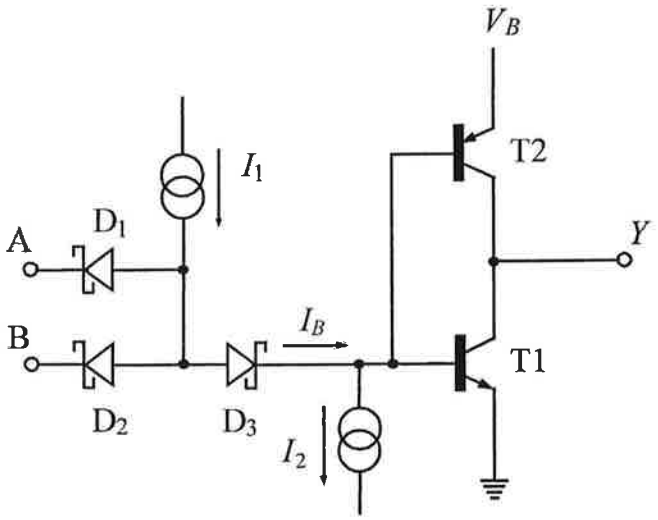

Fig. 2

3 (a) A multiplexer with four data lines, D_0, D_1, D_2, D_3, has two control lines P, Q. It is to be wired to generate a logic function of 4 variables, ABCD, defined by the following expression:

$$f = \sum 0, 1, 5, 6, 7, 9, 10, 14, 15$$

In this notation P and A represent the higher significance variables in their respective groups. Explain how this may be done, and show a circuit diagram of your solution. [30%]

(b) Explain the differences between *Mealy* and *Moore* sequential circuits. [10%]

(c) A modulo-10 counter is to be made from four J-K bistables whose outputs are G_3, G_2, G_1, G_0, where G_3 is the most significant bit. Fig. 3 shows the path of the desired counting sequence as a Karnaugh map. Implement the design synchronously using only 2 and 3 input NAND gates with the four bistables. Show clearly the state table and the Karnaugh maps that are needed to give the simplest inputs for the J-K bistables. A full circuit need not be drawn. [60%]

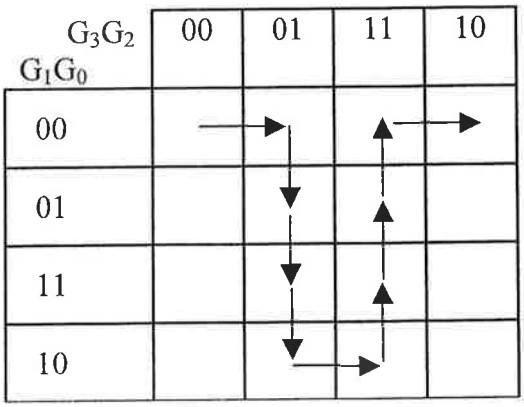

Fig. 3

4 (a) Describe briefly the main steps employed in the Quine-McCluskey tabular method for minimising logic functions. [20%]

(b) Design and show the circuit implementation of a 3-bit synchronous counter whose outputs CBA advance through the sequence: 000, 001, 011, 101, 110, 000; the sequence then repeats. The unused states 010, 100 and 111 are to be regarded as 'don't care' conditions in order to simplify the logic. The implementation is to use T (toggle) bistables with asynchronous Preset and Reset inputs. [50%]

(c) During power-up of the counter designed in (b) it is found that it does not always operate correctly because it can start randomly in an unused state. Develop a simple solution to fix this problem by adding a small number of additional gates to the circuit already implemented, without redesigning the counter. [30%]

END OF PAPER

Answers

1. (b) 1.61 V (c) 1.79 V

2.

3. If AB controls the MUX: $D_0 = \overline{C}$, $D_1 = C + D$, $D_2 = \overline{C}D + C\overline{D}$, $D_3 = C$

$J_3 = G_1.\overline{G_0}$ $\quad K_3 = \overline{G_2}$

$J_2 = \overline{G_3}$ $\quad K_2 = G_3.\overline{G_1}.\overline{G_0}$

$J_1 = \overline{G_3}.G_0$ $\quad K_1 = G_3.G_0$

$J_0 = G_1.G_3 + \overline{G_3}.\overline{G_1}.G_2$ $\quad K_0 = G_3.\overline{G_1} + \overline{G_3}.G_1$

4. $T_C = B$, $T_B = A + B$, $T_A = \overline{A}.\overline{C} + A.C = A \oplus C$