ENGINEERING TRIPOS PART IIA

Wednesday 9 May 2012 9 to 10.30

Module 3F5

COMPUTER AND NETWORK SYSTEMS

Answer not more than ***three*** *questions.*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachments:

Supplementary page with a partially complete diagram for Question 1.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

FINAL version

1 (a) Explain why the latency of the arithmetic logic unit (ALU) is of paramount important in computer hardware design. [10%]

(b) Describe the operation of a single level, 4-bit carry-lookahead adder. [20%]

(c) Figure 1 shows a *carry save adder*, an arrangement of full adders designed to add together five 4-bit numbers d, e, f, g and h. d3 is the most significant bit of d, d0 is the least significant bit, and likewise for the other numbers. In this worst case arrangement, it is assumed that an extra bit is required to store the sum after each number is added in, hence the 8-bit result (sum0 ... sum6 and carry).

(i) Verify the operation of the carry save adder by working through the addition $11 + 3 + 10 + 6 + 8 = 38$. A copy of Fig. 1 with the correct bits inserted for d, e, f, g and h can be found at the back of this question paper. Complete the diagram by labelling each of the remaining signals (i.e. the unlabelled arrowheads) with a 0 or a 1. [20%]

(ii) The carry save adder can be extended to add together more numbers by inserting extra rows before the final ripple-carry stage. If the latency of a full adder is T, what would be the latency of a carry save adder summing N m-bit numbers? Compare this with the more obvious approach of summing the first two numbers using a ripple-carry adder, then adding in the third using a second ripple-carry adder, and so on. [25%]

(iii) Comment briefly on how the design in Fig. 1 might be further improved in terms of both latency and hardware complexity. [15%]

(iv) Suggest one common computing procedure that would benefit from the fast addition of many numbers at once. [10%]

(cont.

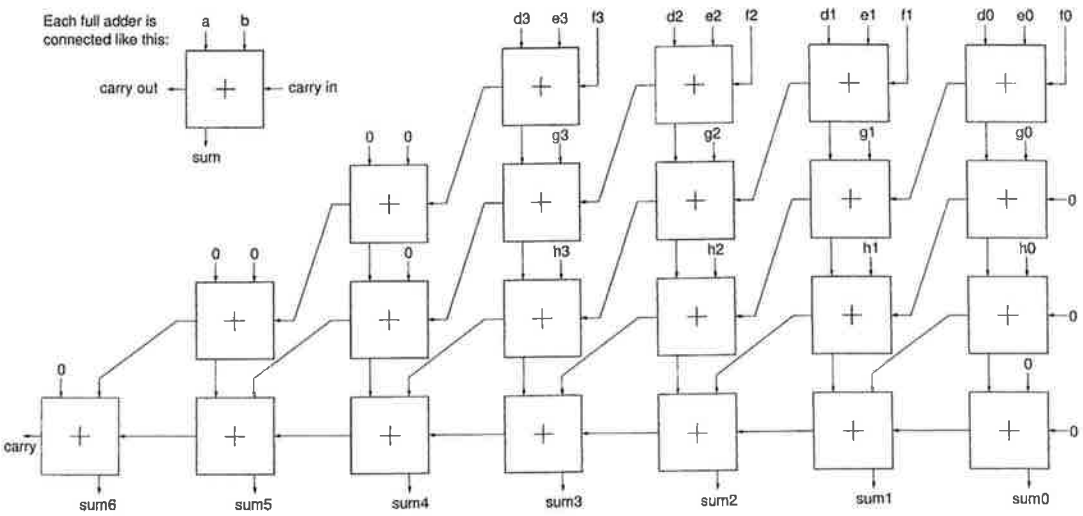


Fig. 1

(TURN OVER

2 (a) Explain what is meant by a pipeline *hazard*. Distinguish between data and branch hazards. [20%]

(b) Consider the following four pairs of MIPS instructions.

```
pair 1   add $9,$8,$10        # writes $9
         add $7,$9,$8         # reads $9

pair 2   sw $9,200($3)        # writes memory location 200($3)
         lw $7,200($3)        # reads memory location 200($3)

pair 3   lw $9,200($3)        # writes $9
         add $7,$9,$8         # reads $9

pair 4   lw $9,200($3)        # writes $9
         sw $9,100($3)        # reads $9
```

Each pair represents a potential "read after write" data hazard. For the MIPS datapath in Fig. 2, and assuming for now no data forwarding, state whether each pair represents an actual hazard. Discuss how any hazards you identify might be resolved through hardware or software means. [40%]

(c) What extra hardware would be required in Fig. 2 to support (i) superscalar operation and (ii) simultaneous multithreading? How would you expect each of these enhancements to affect instruction throughput? [40%]

(cont.

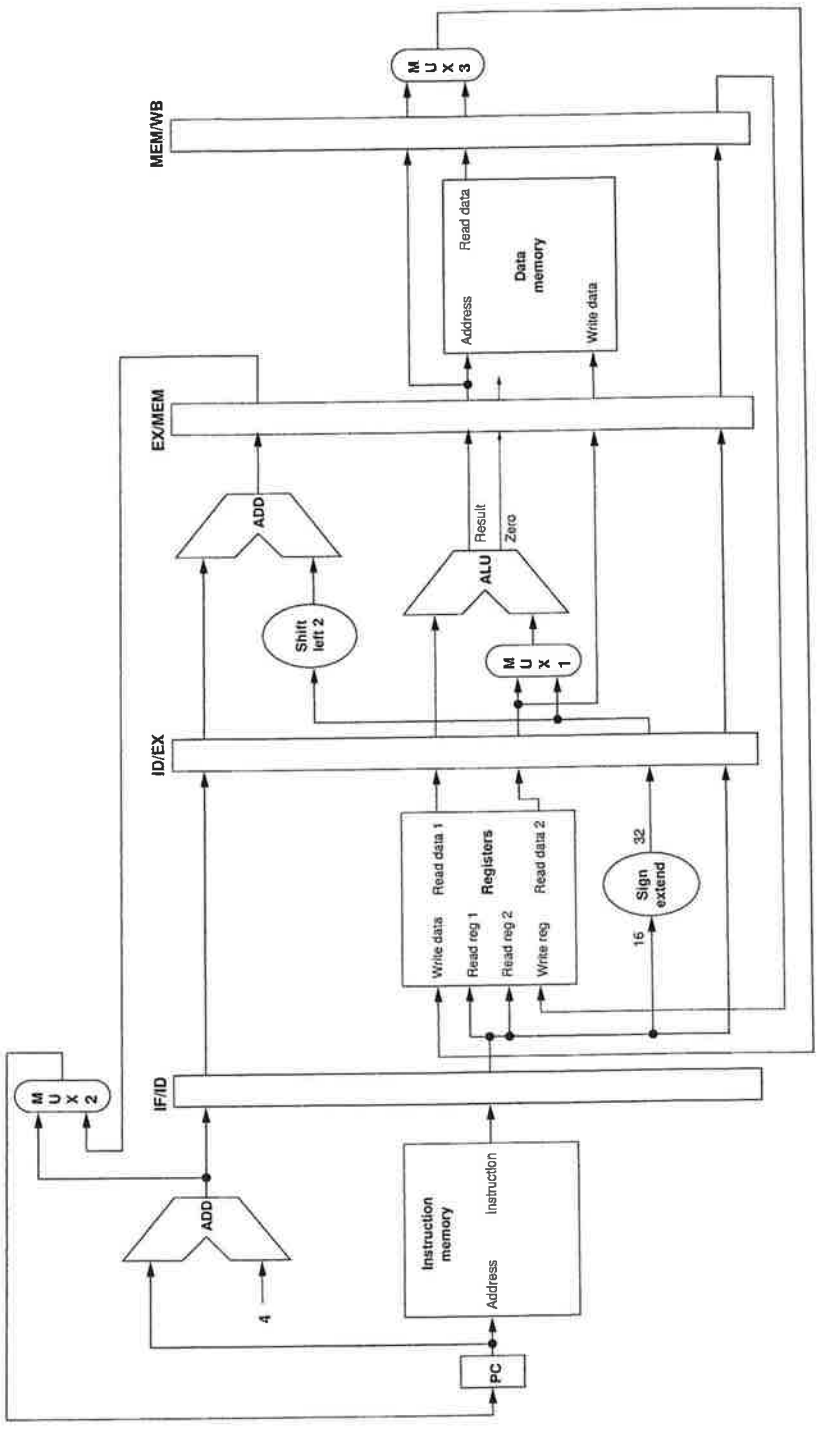


Fig. 2

(TURN OVER

3 (a) Describe the basic function of the *physical layer* as defined by the open system interconnect (OSI) seven layer reference model. Explain why the physical layer is such a critical element in the evolution of computer networks. Give five different examples of purely physical layer entities or protocols that are used in computer networks today. [25%]

(b) Give two examples of physical layer media that have had a direct impact on the evolution of modern network structures and higher layer protocols. Highlight any residual effects seen in these higher layer protocols that are echoes of the previous physical layer entity. [25%]

(c) One of the key features of the OSI reference model is the data terminal equipment (DTE) to data circuit equipment (DCE) interface. Show with a diagram where this interface exists in the OSI model and explain why it is an important part of modern computer networks. [25%]

(d) A modern evolution of several different protocols is the mutli-protocol label system (MPLS) used extensively in today's long haul transmission network. Explain carefully why MPLS is really just an example of the DTE/DCE interface defined in (c). [25%]

4 (a) Give a brief description of the carrier sense multiple access with collision detection (CSMA/CD) medium access control (MAC) protocol when used in an ethernet local area network (LAN). Explain how logical link control (LLC) was originally used to control frames in an ethernet LAN. [30%]

(b) Explain why CSMA/CD was not a suitable protocol for use in wireless LANs. Give two clear examples of where CSMA/CD malfunctions. [20%]

(c) How did the next generation of wireless LAN protocols resolve the two problems demonstrated in (b)? [30%]

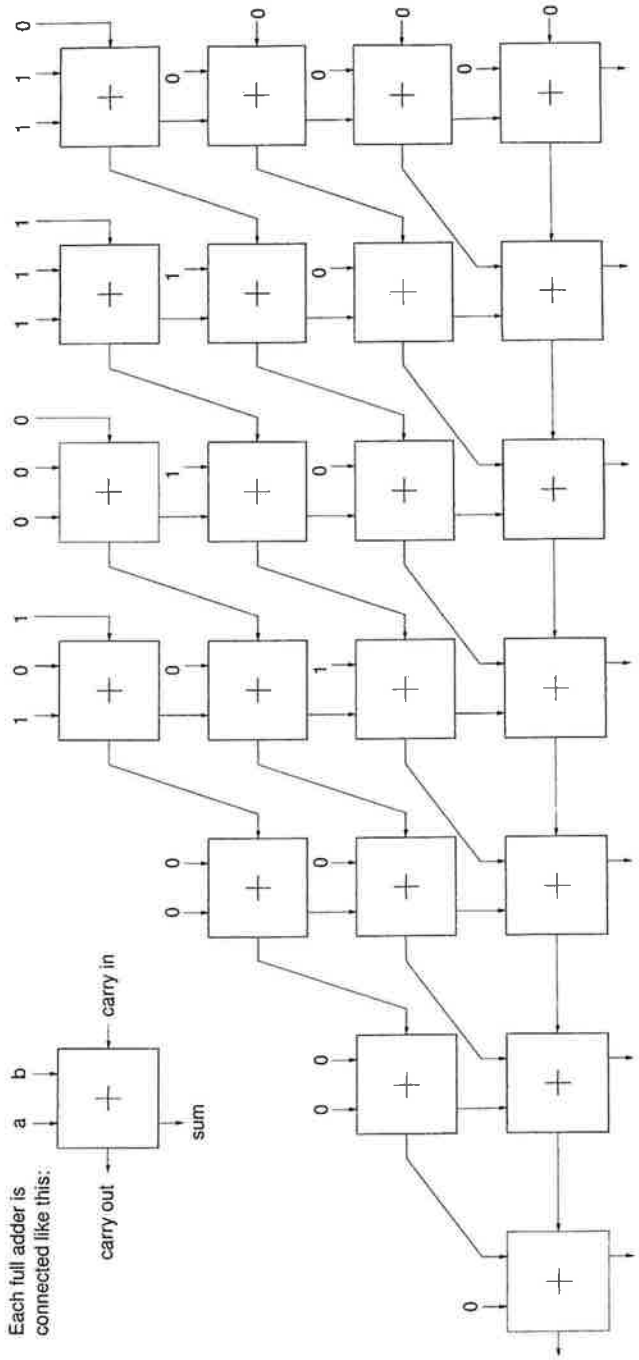
(d) Identify three further techniques that have evolved along with wireless LAN protocols (802.11) to improve their performance over a wireless channel. [20%]

END OF PAPER

Engineering Tripos Part IIA Candidate Number:

Wednesday 9 May 2012 9 to 10.30 Module 3F5

To be detached and handed in with your solution to Question 1



Part IIA 2012

Module 3F5: Computer and Network Systems

Numerical Answers

1. (c) (ii) Carry save $(m + 2N - 4)T$, sequential ripple carry $\frac{N-1}{2}(2m + N - 2)T$.