Module 3B3 2013 Crib

1. (a) (i) For a step-down converter the output voltage V_{OUT} is given by

$$V_{OUT} = \rho V_{IN}$$

Where V_{IN} is the DC input voltage and ρ is the duty cycle.

Two cases: $39V\ to\ 12V$

$$\rho = {}^{12}/_{39} = 0.31$$

$53V\ to\ 12V$

$$\rho = {}^{12}/_{53} = 0.23$$

[10%]

(ii) The inductor current is a triangle waveform with minimum value zero and maximum value ΔI.

During current build-up, $(lasts\ \rho T)$

$$L\,{}^{di}/_{dt} = V_{IN} - V_{OUT}$$

During current decay $(lasts\ (I-\rho)T)$

$$L\,{}^{di}/_{dt} = (O - V_{OUT})$$

Using build-up

$$\int di = \frac{I}{L}\int_0^{\rho T} (V_{IN} - V_{OUT})dt$$

$$V_{OUT} = \rho V_{IN}$$

$$\Delta I = \frac{I}{L} V_{IN}(I-\rho)\rho T$$

As required. [20%]

(iii) At the boundary, $\Delta I = 2I_{OUT}$

So $L_{MIN} = \frac{V_{IN}(I-\rho)\rho T}{2I_{OUT}}$

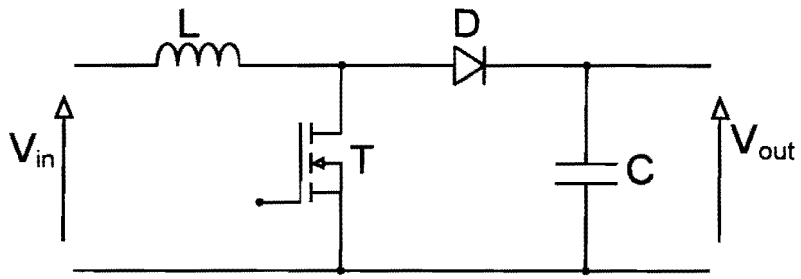
The worst case, i.e. largest L is when I_{OUT} has its lowest value (1 A) and V_{IN} its highest value (53 V).

At 53 V, ρ=0.23

$$L_{MIN} = \frac{53(1-0.23)0.23\,10^{-5}}{2\times 1} H = 47\mu H$$

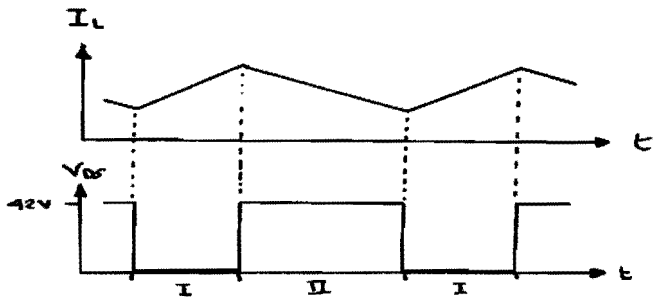
[20%]

b (i)



[10%]

(ii) Diagram showing inductor current and the voltage across the transistor.



[20%]

(iii) When the transistor is off, the voltage across it rises to V_{OUT}, assuming the diode is ideal. So the minimum rating is 42 V- in practice a margin needs to be applied and in automotive applications this is quite large. A 100 V rated transistor would be a good choice. [10%]

(iv) The discontinuous mode is practical, and may be desirable but a closed loop controller is needed. Switching is likely to be based on inductor current rather than using a fixed frequency. Period I transistor is on inductor current grows. Period II transistor is off, inductor current falls. [10%]

2. (a) (i) IGBTs are used for newer voltage source converters for HVDC systems. Reasons include:

(i) IGBT can be turned off whereas thyristors rely on line commutation.
(ii) The switching frequency can be greater as IGBTs switch faster than thyristors.
(iii) Snubber requirements are reduced.

Fast switching reduces the switching loss in one switching event but keeping the switching frequency modest limits overall switching losses.

If at an instant current is flowing out of terminal A, when the upper IGBT is on the current flows through that IGBT. When the upper IGBT turns off, and the lower turns of, the current will continue to flow out of terminal A as the load will be inductive-resistive. The current path will therefore be though the diode in inverse parallel with the lower IGBT. The same reasoning applies to the other IGBTs and diodes depending on the direction of the current. [25%]

(ii) Considering half bridge A, the lower IGBT and the upper diode form a boost converter and the upper IGBT and lower diode form a step-down converter, presupposing an inductance in series with terminal A. [25%]

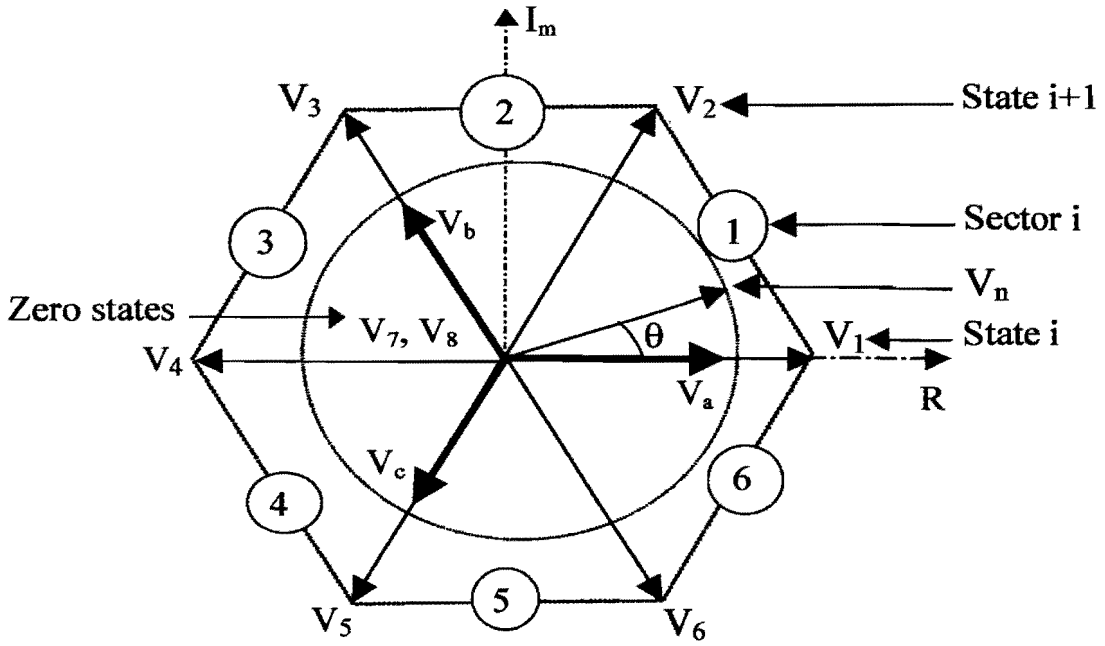
(b) (i) Advantages are (i) the fundamental obtainable from a given DC link voltage is greater (ii) the switching signals are easily generated digitally. [10%]

(ii) The eight states are

State	'ON' switches	$\frac{V_a}{V_{dc}}$	$\frac{V_b}{V_{dc}}$	$\frac{V_c}{V_{dc}}$
V_1	S_1 , S_6 , S_2	1	0	0
V_2	S_1 , S_3 , S_2	1	1	0
V_3	S_4 , S_3 , S_2	0	1	0
V_4	S_4 , S_3 , S_5	0	1	1
V_5	S_4 , S_6 , S_5	0	0	1
V_6	S_1 , S_6 , S_5	1	0	1

[10%]

(iii) The phase and line voltages are represented on the complex plane as follows.



The objective of SVM technique is to obtain V_n with the eight SVs so that it will have an amplitude proportional to the modulation index m and rotating in the complex plane with an angular velocity ω_1 proportional to the frequency of the fundamental output f_1.

Obviously one should obtain V_n using the nearest two non-zero SVs, (State I and i+1), and either of the zero states. By switching between these three (or four) states, duty ratio modulation then controls the magnitude of the two nearest non-zero SVs. [10%]

(iv) Using the diagram of part (iii), the maximum phase voltage achievable by sine wave pwm is the radius of the inner circle. With the space vector approach, the maximum output voltage is given by the circle enclosing the hexagon, Geometry shows these to be in the ratio $2/\sqrt{3}$ or 1.15. [10%]

(v) At each time the microcontroller can work the appropriate states between which to switch according to modulation index. The sequence of states will change along with modulating signal. From the states, suitable signals will be generated for driving the gates of the power devices via suitable gate drive circuitry. Normally the microcontroller will generate values for on and off times and dead-times as desired. [10%]

3. (a) (i) The peak voltage is $230\sqrt{2} = 325\ V$. Allowance can be made for two diode voltage drops of I V, so peak is 323 V. The minimum allowable voltage is 275 V. So ripple voltage is 323-275=48 V.

Using $\Delta V = \frac{I}{2f_c}$ and assuming a 50 Hz supply, gives

$$C = \frac{10}{2.50}\frac{1}{48} = 2mF$$

This formula assumes discharge over half a cycle so gives an over-estimate for C but even so 2mF is large. [25%]

(ii) The point at which charging starts is given by $V_c = 323 \sin\theta$

Where θ is measured from a zero-crossing V_c (the capacitor voltage) is given by

$$V_c = 323 - \frac{10}{2.10^{-3}} \times 7.10^{-3} = 288\ V$$

This corresponds to $\theta = 63°$ or 3.5ms before the peak. Iteration leads to a discharge time of 8.35ms, hitting the rising sine wave 29.5° before its peak, the conduction angle is about 30°. The current wave form is highly distorted so the supply current has a high harmonic content. Harmonic content is subject to regulations and even if not, it is undesirable. [15%]

(b) (i) No turn-on loss in the MOSFET.
No diode recovery loss.

Drawbacks include:

High peak current in the MOSFET.

High I^2R losses in the inductor. [20%]

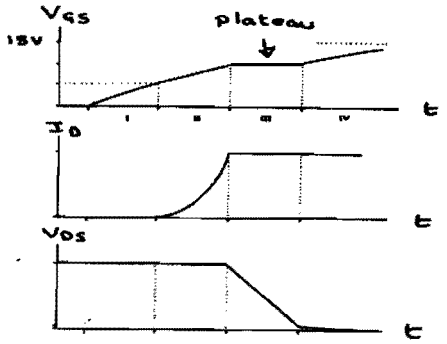
(ii) D_3 to D_6 can be ordinary pn junction power diodes for rectifier service.

D_1 and D_2 need to be fast recovery diodes. [10%]

(iii) The circuit can be though of as being in two parts – step-up converter at the input and a step-down converter at the output. The input converter is operated to draw current as a series of half sine waves, to give an essentially sinusoidal current on the mains side. The voltage step up ratio will need to vary to keep the mains current sinusoidal requiring corresponding variation of the transistor's duty cycle. There is an issue of duty cycle resolution in terms of avoiding distortion near the zero crossing. The voltage across C_1 is then reduced by the following step-down converter to give a fixed output. Transistor T2's duty cycle will be varied to maintain a fixed output voltage against some variation in the voltage across C1. Obviously suitable control chips are needed. There are also more sophisticated ways of operating the circuit. [20%]

(iv) At light load, it would not be possible to maintain continuous conduction in L1. This is not necessarily a problem if the controller can cope. If there is an overload, the boost converter may not be able to maintain the voltage on C1. Also, if the voltage on C1 falls below the required output voltage the operation of the step-down converter is compromised. [10%]

4. (i)



[30%]

(ii) On-state: assume the MOSFET conducts for 50 % of the period. So Pcond is given by

$Pcond = I^2 R_{DSon} 0.5$

$25^2 \times 0.5 \times 0.02 = 6.25W$

Switching: assume linear rise in drawn current over the plateau period. The plateau period is found as follows $\frac{V_{GG}-V_{TH}}{R_G} = C_{VSS}\frac{dV_{DS}}{dt}$

$$\frac{15-5}{5} = 100.10^{-12} - \frac{200}{\Delta t}$$

Hence $\Delta T = 10\ ns$

Switching loss is $½.200.25.10^{-8} J = 25\ \mu J$

Total per period is $50\ \mu J$

Total power loss is $50.10^{-6} \times 450.10^3 = 22.5\ W$ [30%]

(b) (i) At 450 kHz, $X_L = 2\pi 450.10^3.50.10^{-6} = 141\ \Omega$

$Z = 5 + j141$

$|Z| = 141.5\Omega$

$V_1 = \frac{4}{\pi}\frac{1}{\sqrt{2}}V_{DC}$

$= 180\ V_{rms}$

$V_1 = {}^{180}/_{141.5} = 1.27A$

For 3rd harmonic (lowest harmonic)

$V_3 = \frac{4}{\pi}\frac{1}{\sqrt{2}}\frac{1}{3}V_{DC}$

$= 60\ V_{rmr}$

$Z = 5 + j423$

$|Z| = 423$

$I_3 = {}^{60}/_{423} = 0.14\ A$ [10%]

(ii) Resonance occurs at

$\omega^2 LC = 1$

$$C = \frac{1}{50.10^{-6}(450.2\pi 10^3)^2} = 2.5nF$$

[10%]

(iii) At resonance, $|Z| = 5\Omega$

So $\underline{T_1} = {}^{180}/_{5} = 36A$

(iv) The switching can be modified so the voltage across the load is zero for a fraction of the period, either by turning the two upper transistors on together or the two lower together. [10%]