ENGINEERING TRIPOS PART IIA

---

Wednesday 1 May 2013 9.30 to 11

---

Module 3B2

INTEGRATED DIGITAL ELECTRONICS

*Answer not more than **three** questions*

*All questions carry the same number of marks.*

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

*There are no attachments.*

**You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator**

1. The circuit shown in Fig.1 represents a form of an emitter-coupled logic gate in which $V_{CC} = 0$ V, $V_{EE} = -6$ V and $V_R = -1.5$ V. The logic output swing is required to be 1.2V symmetrical around the reference voltage, $V_R$. For all transistors, $V_{BE(on)} = 0.8$ V, and the emitter current of any device may not exceed 5 mA.

(a) Calculate suitable values of $R_{C1}$, $R_{C2}$ and $R_E$ such that the logic levels for the circuit are consistent for input and output, choosing conditions to achieve maximum switching speed. You may assume that all base currents are negligibly low for the purposes of this calculation. [20%]

(b) Sketch a suitable circuit to generate the reference voltage $V_R$ (component values are not required), and explain briefly how it works. [30%]

(c) Determine the noise margins $NM_H$ and $NM_L$. To estimate $V_{IH}$ and $V_{IL}$ you may assume that the width of the transition region of the voltage transfer characteristic is 150 mV, symmetrically placed around $V_R$. [10%]

(d) Estimate the change in the output voltage at the terminal $V_{O2}$ due to the base current drawn by T4 if the current gain, $h_{FE}$, of T4 is 50? [10%]

(e) Determine the maximum fan-out of the circuit assuming that it is limited by the reduction in the high level noise margin, $NM_H$, because of loading by the driven gates. You may assume that a 10% reduction in $NM_H$ can be tolerated. State all assumptions made. Explain why the calculated fan-out is unlikely to be realised in practice. [30%]

(cont.

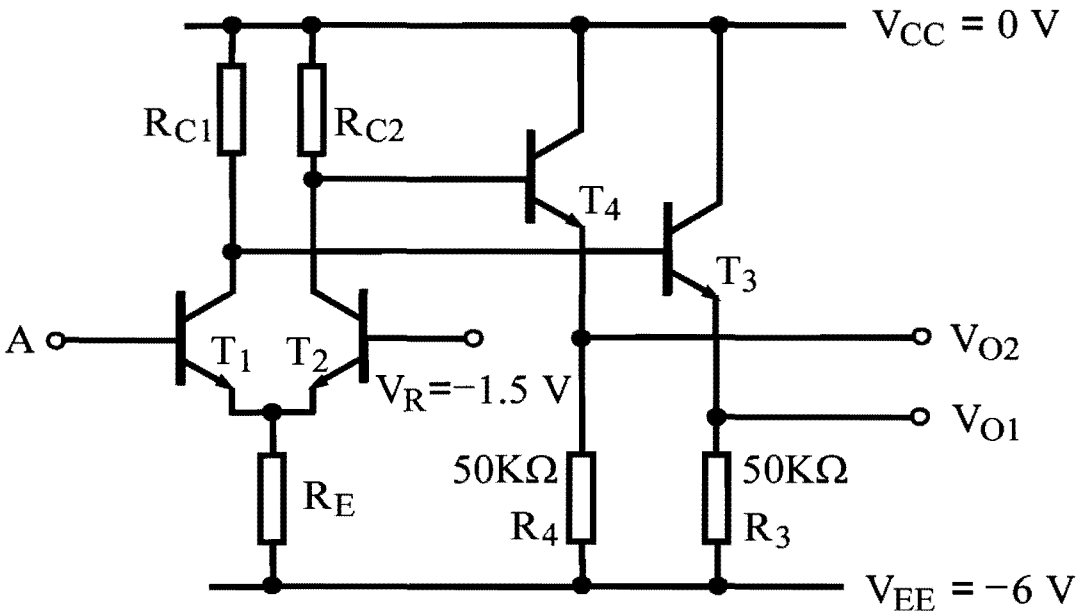


Fig. 1

(TURN OVER

2. (a) Give the reasons for the popularity of CMOS technology in the design of digital logic systems. What are the disadvantages of CMOS? Your answer may include references to: implementation, compactness, input and output levels, and drive capability, as well as any other factors you consider important. [30%]

(b) With the aid of a diagram, show how to determine the noise margins from the input and output logic levels $V_{IL}$, $V_{IH}$, $V_{OL}$ and $V_{OH}$. [30%]

(c) Fig. 2 shows a simple CMOS static random access memory cell. Explain the mode of operation of this circuit, and explain the role of the signals *word*, *bit*, and $\overline{bit}$ in allowing data to be written and read. Describe briefly the special design criteria that apply to the MOSFETs M1 - M6. [40%]

(cont.

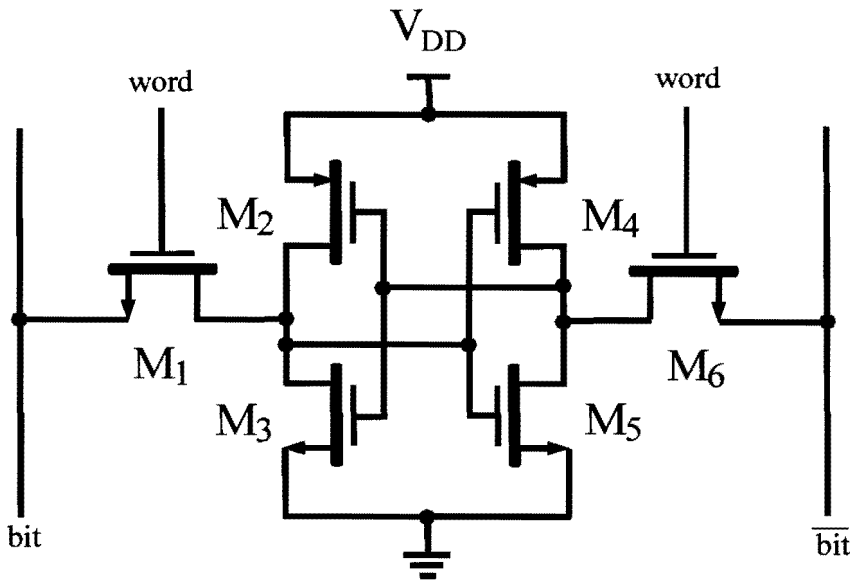


Fig. 2

(TURN OVER

3. (a) Draw the equivalent circuit of a Master-Slave J-K bistable using S-R bistables and logic gates. Write down the logic function of the J-K bistable which defines the next state as a function of the present state and the inputs. [30%]

(b) By using the reverse engineering method analyse the logic circuit shown in Fig.3. Derive the state table and the state diagram. [50%]

What specific function does the circuit in Fig. 3 perform? [20%]

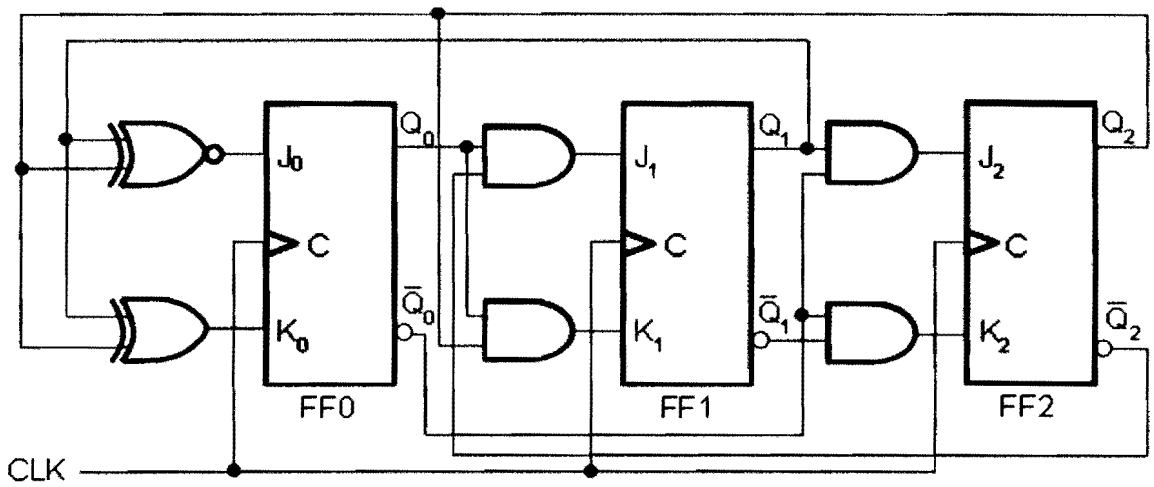


Fig. 3

4. Fig.4 shows the block diagram of a circuit that adds two binary numbers. The numbers are fed to the adder serially starting with the least significant bit, at the input $X_i$ and $Y_i$. The sum $Z_i$ appears in a serial form at the output while the carry bit is fed back through a bistable to the input.

(a) Implement the circuit using a J-K bistable and a Programmable Logic Array. State any assumptions made. [30%]

(b) The circuit in Fig.4 is to be modified to perform either addition or subtraction of two binary numbers depending on an external control signal. Show how this circuit could be implemented using a J-K bistable and a Programmable Logic Array. [30%]

(c) Compare the operation and performance of the sequential adder shown in Fig. 4 with those of a combinational ('parallel') adder that would perform a similar function. [20%]

(d) Draw the block diagram of a 4 bit parallel adder-subtractor and show specifically the part of the circuit that decides whether addition or subtraction is to be performed. [20%]

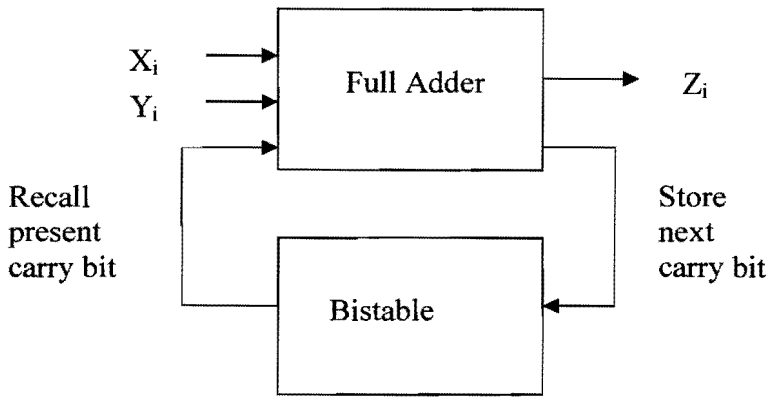


Fig. 4

**END OF PAPER**