4B2 CRIB 2003

1. a) Conductivity modulation

In a semiconductor with a low-doped region carriers may be injected of the opposite type. Injecting a large number creates a field attracting carriers of the same type as the original doping. Hence it appears more highly doped and its conductivity is significantly reduced.

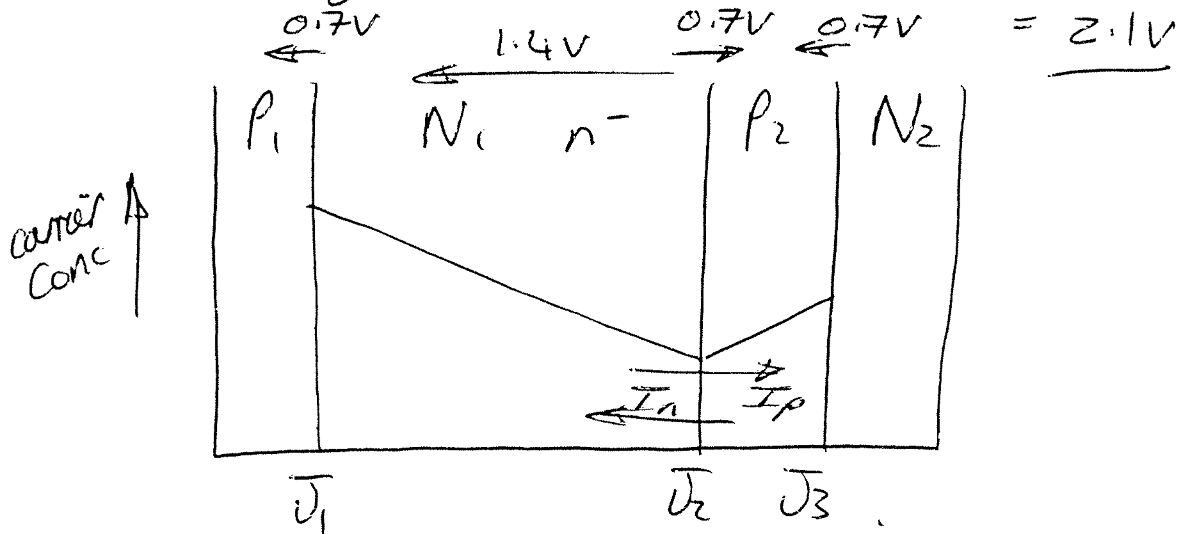
Injection efficiency.

In a pn^- junction, a forward bias results in a current flow consisting mostly of holes into the n^-, by virtue of their ratios. However the number of electrons in the n^- increases (see above) so the ratio of the carrier flows changes. Injection efficiency refers to this ratio.

4

1, a) <u>cont</u>.

Converter grade thyristor.

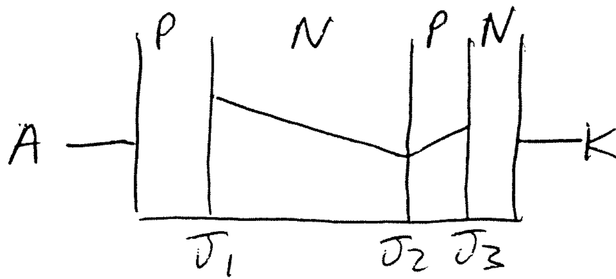


N_1 is n^- and heavily conductivity modulated.

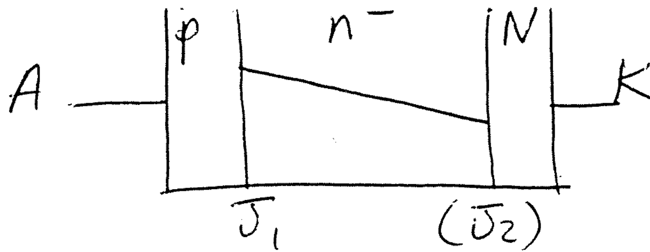
The injection efficiency of J_1 and J_3 starts very low when the device is off. It then rises as carriers are injected in large numbers — increased current. It then settles back down as the N_1 and P_2 regions get swamped with carriers. ~~and~~ Conductivity modulation in N_1 means that a lot of electrons come through ~~back from~~ J_1, giving an injection efficiency of about 0.3

J2 also participates as the conductivity modulation causes it to become forward biased. However it can't really be considered to be injecting current — more that it's field changes the carrier concentration.

1/b) The carrier distributions are similar.



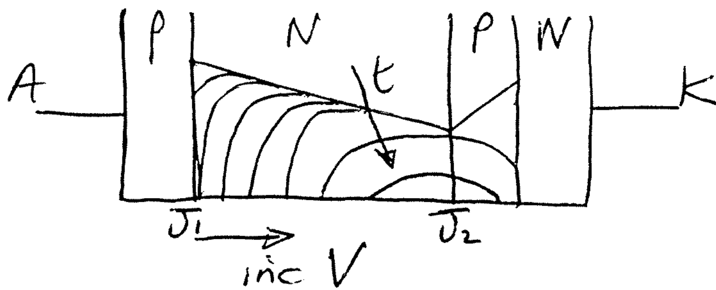
Thyristor



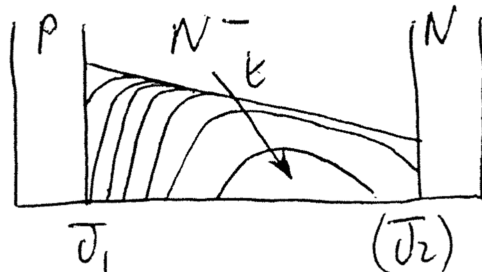
high voltage
p-n⁻-n diode

2

Turn off is accomplished by taking the current down to zero and then the voltage may then appear in reverse.



The charge around J_2 recombines. Some is removed by reverse current



2 The charge around J_2 is initially removed by reverse current & then recombination after the depletion layer at (J_2) appears.

In essence the turn of is quite similar However diodes are optimised for soft turn-off 2

Electron irradiation, γ ray irradiation, Gold doping.
3

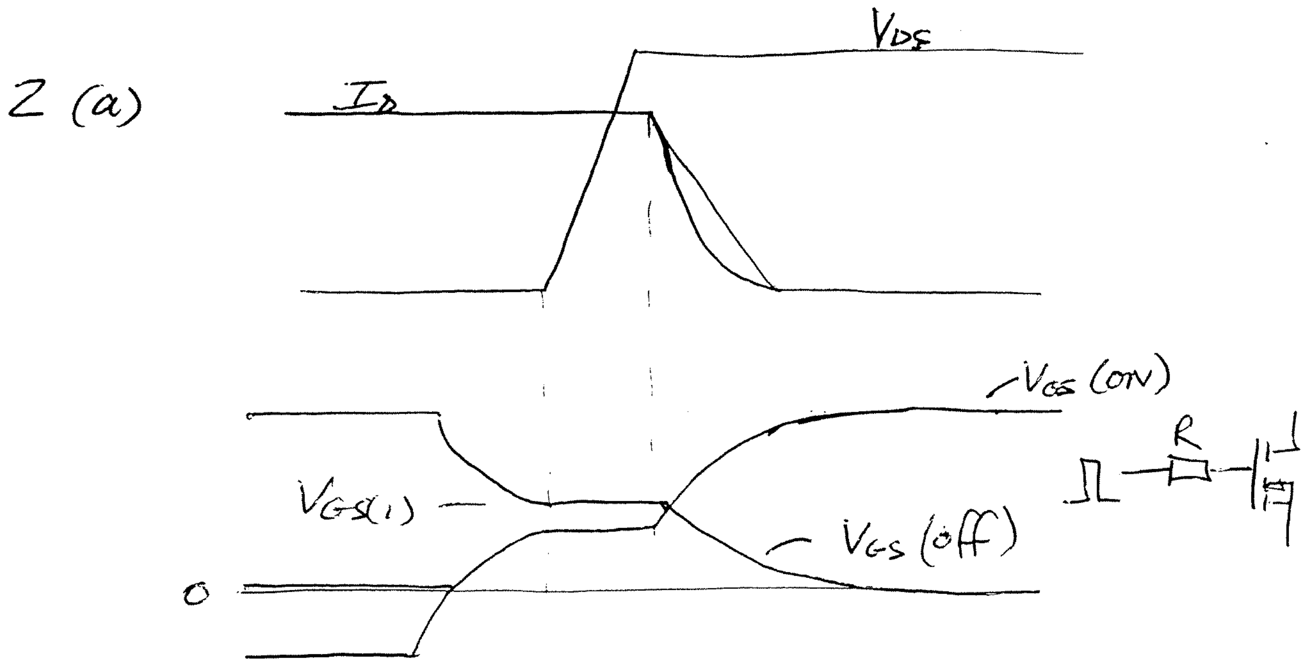
1/ c) In a diode the idea is to keep charge around the n^-N junction (J_2) to allow the charge to be removed while the volts are rising. Also the volts must be allowed to rise so the charge must go from around J_1 first. Since the current is common, the

charge around J_1 must be lower to start with and removed easily. The only way to do this is via irradiation (or gold doping). The region around J_1 is affected. Also, to keep the reverse current small, the overall lifetime is reduced to a very low value. Electron irradiation covers the whole device.

In a converter grade thyristor, the main issue is a low on-state voltage, so long lifetimes are needed. However to give a good $\frac{dV}{dt}$

rating at turn-off and a short turn-off time t_q some electron irradiation is used.
3

2 (a)



There are three phases in the gate voltage waveform. The first is dis-charging C_{iss} to the voltage $V_{GS(1)}$ required to support the drain current. 2

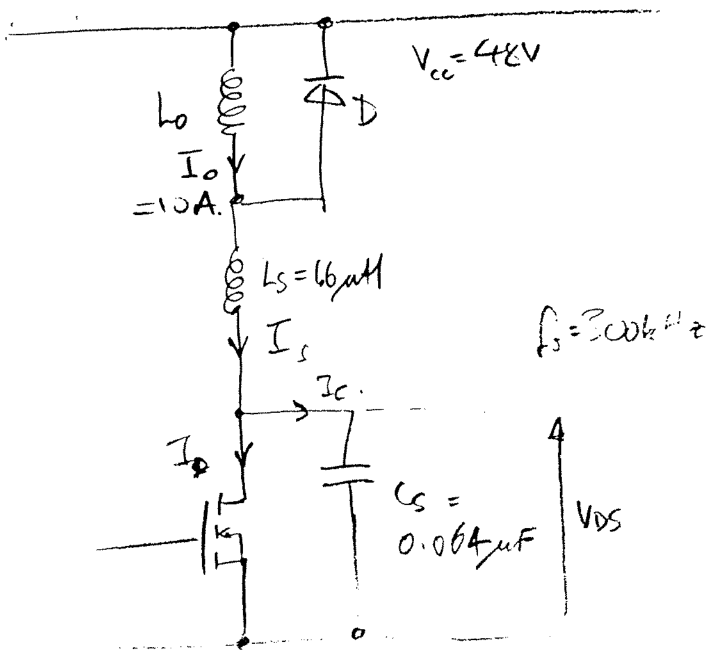
As it tries to go lower, the drain voltage will rise. The discharge gate current is then matched by the current $C_{GD}\frac{dV_{DS}}{dt}$, so C_{GS} stops disharging and the plateau appears. 2

Once the voltage V_{DS} has risen to the supply voltage, the current redirects to the freewheel diode (not shown) and the current can fall. C_{iss} dicharges and the drain current follows it down according to

$$I_D = \frac{K}{2}(V_{GS}-V_{TH})^2$$

2

2 (b) Square corner on the Safe Operating area — so can use max V & I directly. 2
Control of switching via the gate, can control diode recovery 2
(Cost!)



(a) Calculate energy at turn-off and resulting switching power loss

Assume I_D falls linearly in 100ns. $\Rightarrow$ $\frac{dI_D}{dt} = \frac{-10}{100e-9} = -100e6\ As^{-1} = -100A/\mu s$

$$\Rightarrow I_D = 10 - t \times 100e6$$

Then $I_C = 10 - I_D = t \times 100e6$

$$\Rightarrow V_{DS} = \frac{1}{C_s}\int_0^{t_0} I_C\,dt = \frac{1}{C_s}\,100e6 \times \frac{t_0^2}{2} = \frac{100e6 \times (100e-9)^2}{2 \times 0.064e-6}$$

$$= 7.8125V$$

Also $E = \int_0^{t_0} V_{DS} I_D\,dt$

$$= \int_0^{t_0} \left(\frac{1}{C_s}\left|\frac{dI_D}{dt}\right| \times \frac{t^2}{2}\right) \times \left(10 - \left|\frac{dI_D}{dt}\right| t\right) dt$$

$$= \frac{1}{2C_s}\left|\frac{dI_D}{dt}\right| \int_0^{t_0} 10t^2 - t^3\left|\frac{dI_D}{dt}\right| dt$$

$$= \frac{1}{2C_s}\left|\frac{dI_D}{dt}\right| \left[\frac{10t^3}{3} - \frac{t^4}{4}\left|\frac{dI_D}{dt}\right|\right]_0^{t_0}$$

$$= \frac{1}{2 \times 0.064e-6} \times 100e6 \times \left(\frac{10 \times (100e-9)^3}{3} - \frac{(100e-9)^4}{4} \times 100e6\right)$$

$$= 651nJ \Rightarrow P = Ef = 651e-9 \times 300e3 = 0.195W$$

2/c) cont.

$$Z_0 = \sqrt{\frac{L}{C}} = \sqrt{\frac{1.6}{0.064}} = 5$$

Once the diode comes on, the L-C circuit rings with the 10A remaing in L. The ringing voltage peak is $I_0 Z_0 = 50V$.

So max $V_{DS} = 48 + 1 + 50 = \underline{\underline{99V}}$

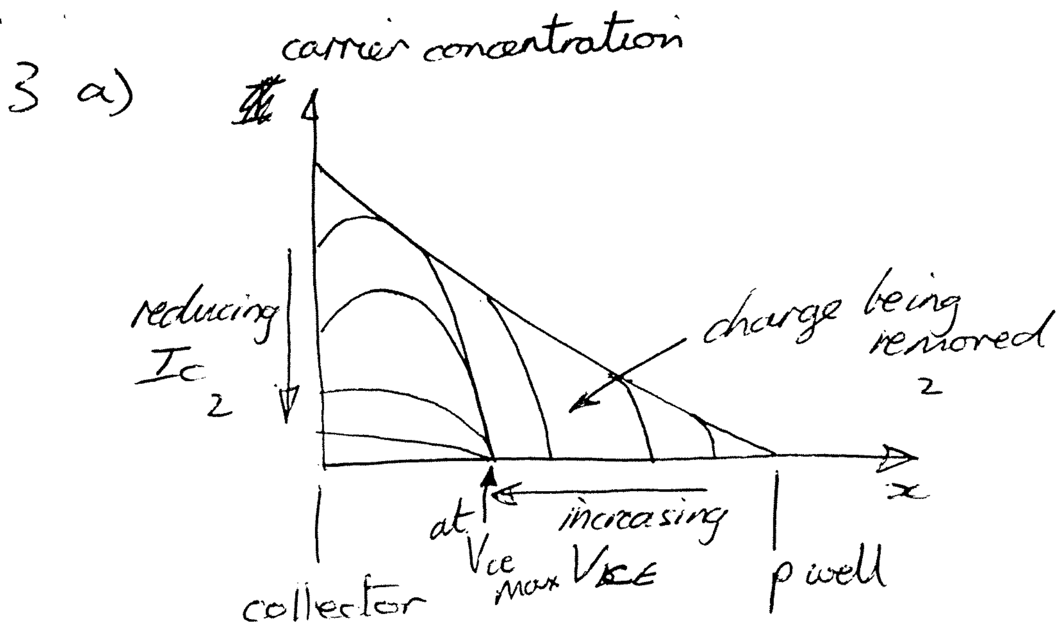
(1 = diode drop.)

4

The advantage of this circuit is low - even very low switching losses. But, the voltage capabilities of the MOSFET must be about 2x those needed for hard-switching. This probably means a higher on-state voltage and <u>more</u> on-state losses!

2

3 a)



With an inductive load, the volts must rise first before the current may fall. 2

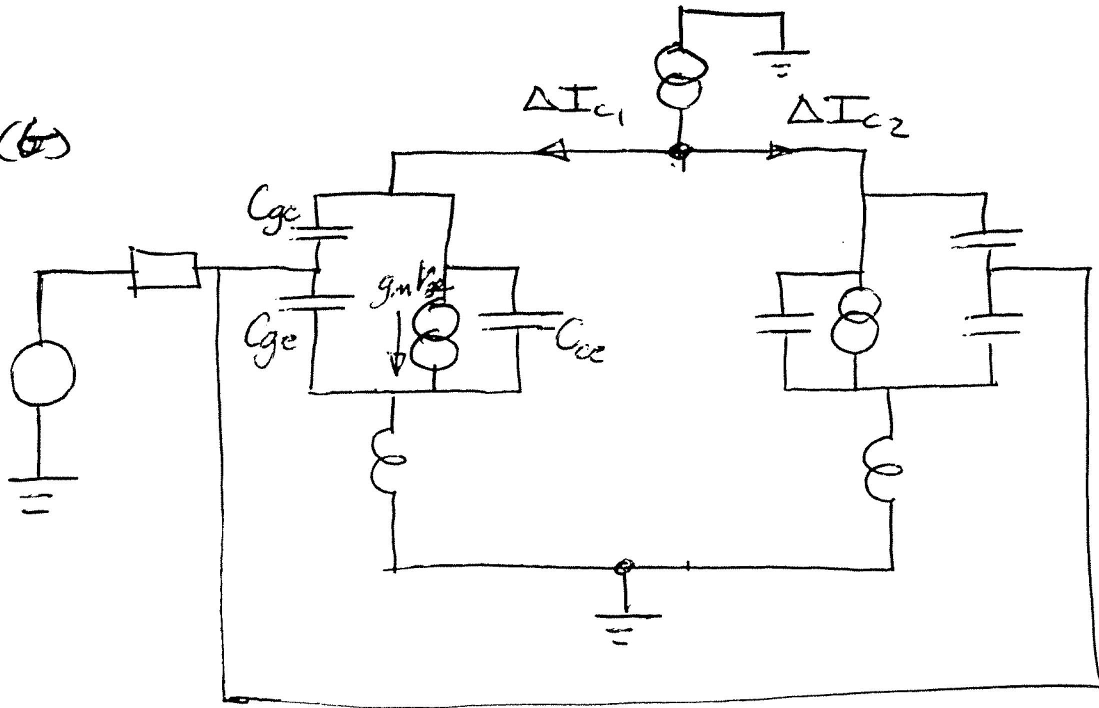
So at turn-off the voltage rises, with a depletion layer forming around the p-wells. Nothing changes at the collector and, as it knows no changes in its current.

Once the voltage has risen, the collector current may fall. This is indicated by the reduced gradient at $x=0$. As the current may fall quickly, charge appears "trapped". This is removed by the tail current, which remains for a long time, typically. Thus the "bump" of charge turns into a slope and drops away.

The depletion layer cannot form until charge is removed by I_c. As this is a large quantity of charge the process is slow. It obeys the

$$I_c = C_0 \frac{dV_{CE}}{dt}$$ capacitor equation. 2

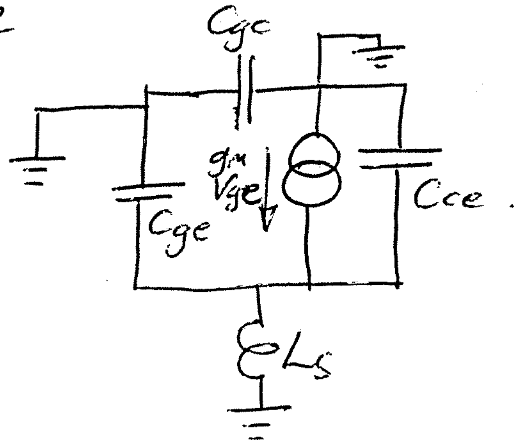
3(b)



A little careful thought is required:

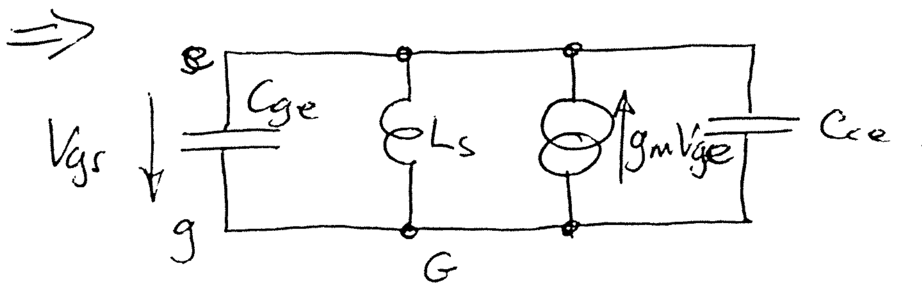
$\Delta I_{c_1} = -\Delta I_{c_2}$ so the collector looks like it is at ground.

So $\frac{1}{2}$ circuit.



2

$\Rightarrow$



3(b) cont.

Σi at G.

$$(C_{ge} + C_{ce}) s V_{ge} + \frac{1}{sL_s} V_{ge} + g_m V_{ge} = 0$$ 2

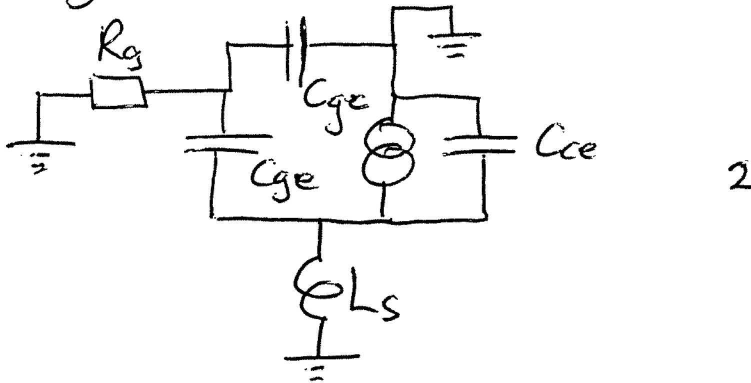
the resonant frequency, for low damping

is $\frac{1}{\sqrt{L_s(C_{ge}+C_{ce})}} \simeq 16\,MHz$ 2

equation.

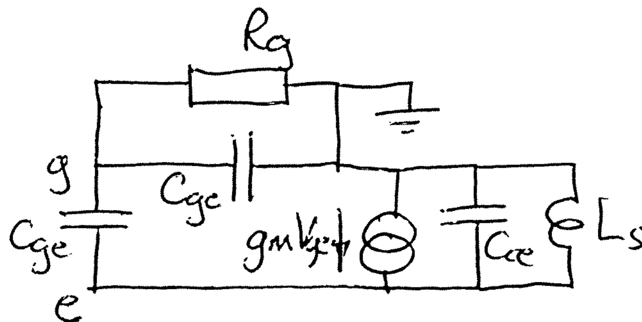
$$(s^2 L_s (C_{ge}+C_{ce}) + sL_s g_m + 1) V_{ge} = 0.$$

With a gate resistor in series with each gate.



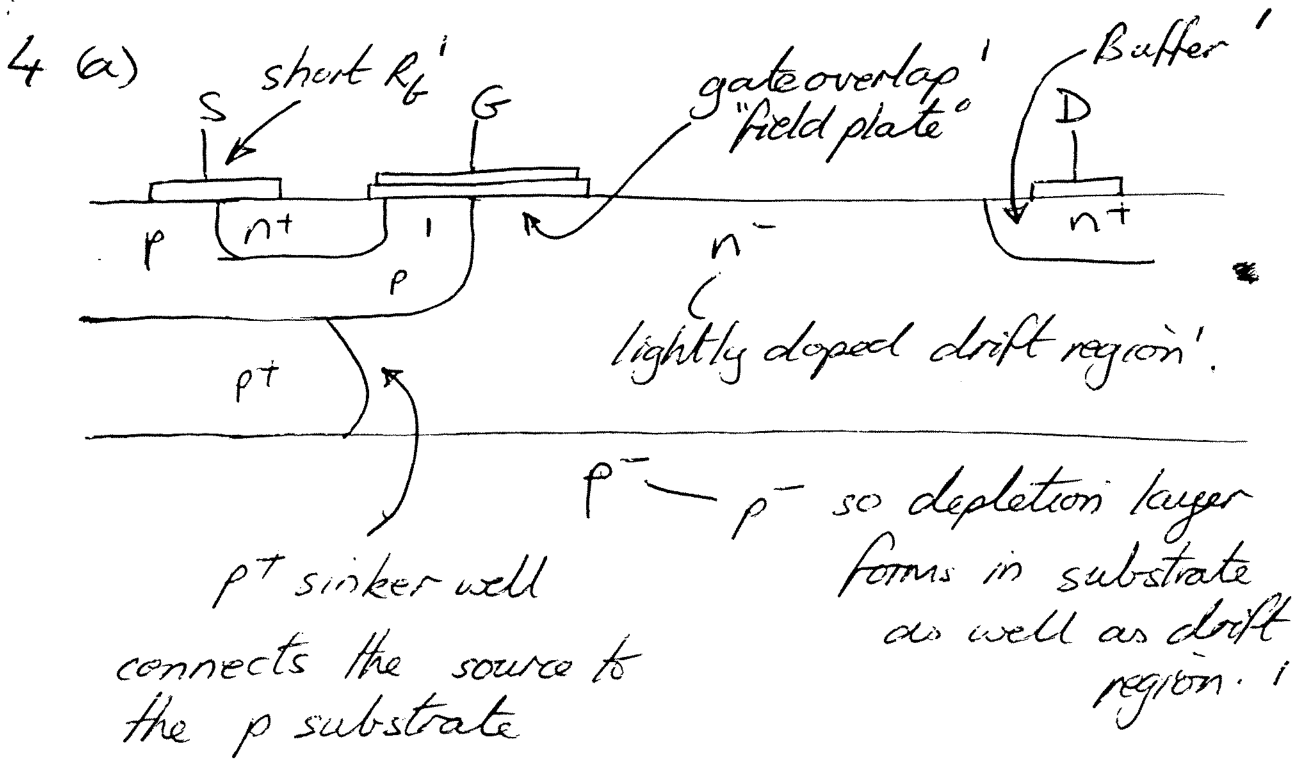
2

$\Rightarrow$



Whilst R_g removes some resonances, if an appropriate value is chosen, it still leaves an oscillatory response to step changes. <u>But</u> it also <u>slows the switching</u> 2

4 (a)



The short R_f eliminates the npn bipolar action so the $\frac{dV}{dt}$ rating is high.

4 (b) i) forward MOSFET Cathode = Source
Anode = Drain.
Anode gate connected to Anode. 2

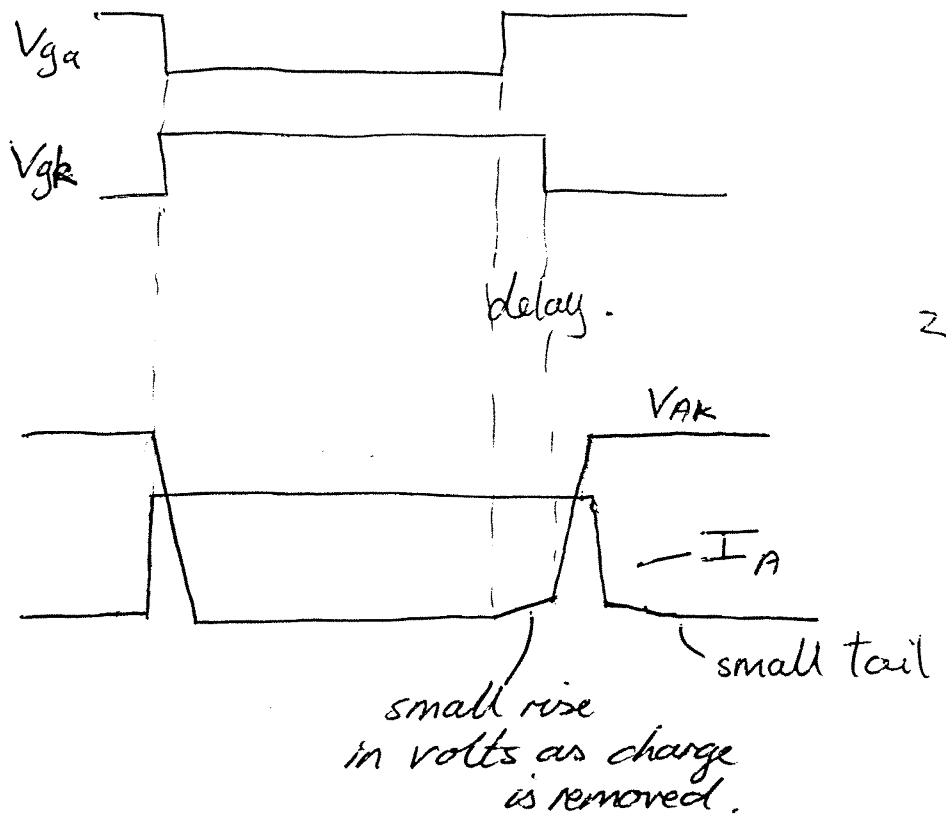
ii) Reverse diode – as above, note the cathode short. 2

iii) forward LIGBT Cathode = Emitter
Anode = Collector. 2
Anode gate voltage 10V below Anode V.

iv) Weak forward IGBT at high current
Anode gate connected to anode
The current overcomes the Anode short. 2

b(cont)

Turn-on needs no special precautions. So switch both gates simultaneously. At turn-off it is attractive to remove charge early rather than in an exponential (lossey) tail after turn-off. So turn off the anode gate early.



A good RESURF design allows the n-drift to be as short as possible.

Good Kathode and anode shorts so that the parasitic behaviour does not come into play at turn-off. 2

Short MOS channels ~ light p & n doping under the ~~channe~~ gates. This conflicts with the shorting performance unless small geometries are used at the shorts. 2

1 Mark each sensible new point

5/. In each case the choice is far from easy! Usually the main choice is between two of the three.

a) Low V so not IGBTs due to onstate voltage

	Cost	efficiency.	circuit.
MOS	high	OK (see cost)	easy.
Bipolar	low	OK / poor (hard to drive.)	tricky

b) High V, but very low current. Not IGBT's

	Cost	efficiency	circuit.
MOS	low*	low (see cost)	drivers too expensive
Bipolar.	low	high.	easy (consistent load)

* May use p-channel.

c) ~600V dc so about 5-10A switching.
1000V MOSFETs at 10A are very expensive.

	Cost	efficiency	circuit.
IGBT	OK	OK.	use simple driver ICs
Bipolar	OK	high	hard - varying I_c. high base current.

d) 300V 30kW ⇒ dc volts so 100A.
Unattractive bipolar gate drives needing ≈10A I_B

	Cost	efficiency	circuit
IGBT	OK.	lower on-state	easy.
MOS	OK.	more devices in parallel.	easy.

Might let efficiency dominate costs.