4B8 – ELECTRONIC SYSTEM DESIGN

SOLUTIONS FOR EXAM - 23 APRIL 2003

V1.0

SOLUTIONS

1. Solution for question 1

(a)

(i) V_{in} connects to the GND.
The source of the noise voltage, connects to the inverting node of the amplifier therefore:

$$(V_0 - V_e) / R_2 = V_e / R_1$$

$$V_0 - V_e = V_e R_2 / R_1$$

$$V_0 = V_e + V_e R_2 / R_1$$

$$V_0 = V_e (1 + R_2 / R_1)$$

(ii) The noise voltage source connects to the non-inverting node of the amplifier. As the inverting input of the amplifier will be at the same potential as the non-inverting node of the amplifier then the same equation will be derived as in case (i).

(b) Assume that the bias current i_{b2} flows through the resistor R and the bias current i_{b1} flows through the resistor R_1. The output voltage V_0 is defined as:

$V_0 = V_+ - V_-$
$V_+ = R\, i_{b2}$
$V_- = R_1 R_2 / (R_1 + R_2)\, i_{b1}$ (parallel resistors in feedback)
$V_0 = R\, i_{b2} - R_1 R_2 / (R_1 + R_2)\, i_{b1}$

The output V_0 will be zero if:

$$R\, i_{b2} = R_1 R_2 / (R_1 + R_2)\, i_{b1}$$

The bias current for a non-inverting and an inverting nodes are equal then:

$$i_{b2} = i_{b1}$$

$$R = R_1 R_2 / (R_1 + R_2)$$

(c)

(i) Open loop gain for a two-stage amplifier is defined as:

$$A(\omega) = A_0 / [(1 + j\,\omega/\,\omega_1)(1 + j\,\omega/\omega_2)]$$

If $j\omega = s$ then

$$A(s) = A_0 / [(1 + s/\omega_1)(1 + s\omega_2)]$$
$$A(s) = A_0\,\omega_1\,\omega_2 / [(\omega_1 + s)(\omega_2 + s)]$$

As

$$A(f) = A(s)/(1 + \beta A(s))$$

Then

$$A(f) = A_0\,\omega_1\omega_2/\,[(\omega_1 + s)(\omega_2 + s)] / \{(1 + \beta A_0\,\omega_1\omega_2/\,[(\omega_1 + s)(\omega_2 + s)]\}$$
$$A(f) = A_0\,\omega_1\omega_2/\,[(\omega_1 + s)(\omega_2 + s)] / \{[[(\omega_1 + s)(\omega_2 + s)] + \beta A_0\,\omega_1\omega_2]/\,[(\omega_1 + s)(\omega_2 + s)]\}$$
$$A(f) = A_0\,\omega_1\omega_2/\,[(\omega_1 + s)(\omega_2 + s) + \beta\,A_0\,\omega_1\omega_2]$$
$$A(f) = A_0\,\omega_1\omega_2/\,[\,s^2 + s(\omega_1+\omega_2) + \omega_1\omega_2 + \beta A_0\,\omega_1\omega_2]$$
$$A(f) = A_0\,\omega_1\omega_2/\,\{\,\omega_1\omega_2\,[s^2/\,\omega_1\omega_2 + s(\omega_1+\omega_2)\,/\,\omega_1\omega_2 + 1 + \beta A_0]\}$$
$$A(f) = A_0 / [s^2/\,\omega_1\omega_2 + s(\omega_1+\omega_2)\,/\,\omega_1\omega_2 + 1 + \beta A_0]$$
$$A(f) = A_0 / \{\,(1+\beta A_0)[\,s^2/[\,\omega_1\omega_2\,(1+\beta A_0)] + s(\omega_1+\omega_2)\,/[\,\omega_1\omega_2\,(1+\beta A_0)] + 1\,]\}$$
$$A(f) = A_0 / [\,s^2/[\,\omega_1\omega_2\,(1+\beta A_0)] + s\,(w_1+w_2)\,/[\,\omega_1\omega_2(1+\beta A_0)] + 1\,]$$

If

$$\omega_n = [\omega_1\omega_2\,(1+\beta A_0)]^{1/2}$$

$$A(f) = A_0 / [\,s^2/\,\omega_n{}^2 + s\,(\omega_1+\omega_2)/\,\omega_n{}^2 + 1]$$

If

$$K = (\omega_1+\omega_2)\,/\,2\,\omega_n$$

$$A(f) = A_0 / [\,s^2/\,\omega_n{}^2 + s\,2K\,/\,\omega_n + 1] \qquad (\text{eq. } 1)$$

(ii) From eq 1. using $s = j\omega$

$$A(f) = A_0 / [\,-\omega^2/\,\omega_n{}^2 + j2K\,\omega/\,\omega_n + 1]$$

$A(f) = A_0 / [\ 1 - \omega^2 / \omega_n^{\ 2} + j2K\ \omega / \omega_n]$

Then

$| A(f) | = | A_0 | / |[\ 1 - \omega^2 / \omega_n^{\ 2} + j2K\ \omega / \omega_n] |$

$| A(f) | = | A_0 | / [\ (1 - \omega^2 / \omega_n^{\ 2})^2 + 4K^2\ (\omega / \omega_n)^2\ ]^{1/2}$

The peak frequency is defined by the minimum of the denominator D

$D(\omega) = (1 - \omega^2 / \omega_n^{\ 2})^2 + 4K^2\ (\omega / \omega_n)^2$
$D(\omega) = 1 - 2\omega^2 / \omega_n^{\ 2} + \omega^4 / \omega_n^{\ 4} + 4K^2\ \omega^2 / \omega_n^{\ 2}$
$D(\omega) = \omega^4 / \omega_n^{\ 4} - 2\ \omega^2 / \omega_n^{\ 2}\ (\ 1 - 2K^2) + 1$

The minimum will be when

$D'(\omega) = 0$

Let $\omega^2 / \omega_n^{\ 2} = m$

$D(m) = m^2 - 2m(\ 1 - 2K^2) + 1$

$D'(m) = 2m - 2(1 - 2K^2)$

then

$2m = 2(1 - 2K^2)$

$m = 1 - 2K^2$

and

$\omega = \omega_n\ (1 - 2K^2)^{1/2}$

$| A(f) | = | A_0 | / [\ (1 - \omega^2 / \omega_n^{\ 2})^2 + 4K^2\ (\omega / \omega_n)^2\ ]^{1/2}$

$| A(f) | = | A_0 | / [\ (1 - 1 + 2K^2)^2 + 4K^2(\ 1 - 2K^2)]^{1/2}$

$| A(f) | = | A_0 | / (\ 4K^4 + 4K^2 - 8K^4)^{1/2}$

$| A(f) | = | A_0 | / [4K^2\ (\ 1 - K^2\ )]^{1/2}$

$$| A(f) | = | A_0 | / 2K (1 - K^2)^{½}$$

$$A = 1 / 2K (1 - K^2)^{½}$$

$\omega_1 = 2\pi 10^3$
$\omega_2 = 2\pi\ 10\ 10^3$
$A_0 = 120\ dB = 10^6$
$\beta = 0.5$

$$\omega_n = [\omega_1 \omega_2 (1+ \beta A_0)]^{1/2}$$

$$\omega_n = [4\pi^2\ 10^3 10^4 (1 + 0.5\ 10^6)]^{1/2}$$

$$\omega_n = 2\pi\ [1010^6 (1 + 0.5\ 10^6)]^{1/2}$$

as $1 << 0.5\ 10^6$ then

$$\omega_n = 2\pi\ [1010^6\ 0.5\ 10^6)]^{1/2}$$

$$\mathbf{\omega_n = 2\pi\ 2.23\ 10^6}$$

The natural frequency is at 2.23 MHz

The damping factor is as:

$$K = (\omega_1 + \omega_2) / 2\omega_n$$

$$K = (2\pi 10^3 + 2\pi\ 10\ 10^3) / (2\ \ 2\pi\ 2.23\ 10^6)$$

$$K = 11\ 10^3 / 4.43\ 10^6$$

$$\mathbf{K = 2.48\ 10^{-3}}$$

The peak frequency is at:

$$\omega = \omega_n (1 - 2K^2)^{1/2}$$

$$\omega = 2\pi\ 2.23\ 10^6 (1 - 2\ (2.48)^2 10^{-6})^{1/2}$$

$$\mathbf{\omega = 2\pi\ 2.229\ 10^6}$$

The amplitude is defined as:

$A = 1 / [2K (1 - K^2)^{½}]$

$A = 1 / [2\ 2.4810^{-3} (1 - 6.15\ 10^{-6})^{1/2}]$

A = 203.6

2. Solution for question 2

(a) Pin A represents End Of Conversion - EOF
Pin B is Start of Conversion - SC

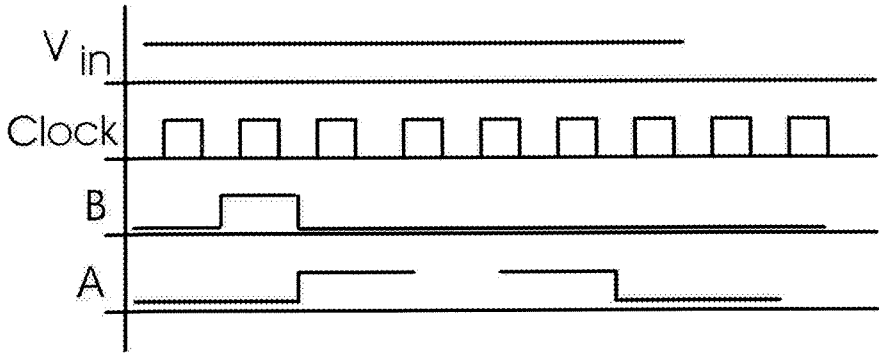


Fig 7.

(b) On a positive edge of the signal SC the COUNTER is reset and signal EOF is at a logical high enabling clock to increment the COUNTER. When the voltage from the D/A converter is bigger than the input voltage V_{in}, signal EOF is low and further counting is disabled. The digital representation of the input voltage is at the output of the COUNTER.

(c) First determine D/A step:

$V_{d/a\ step} = F.S. / (2^{n} - 1)$

$V_{d/a\ step} = 1023\ mV / (2^{10} - 1)$

$V_{d/a\ step} = 10\ mV$

$V_{d/a} = V_{in} + VT$

$V_{d/a} = 6530 + 0.1 = 6530.1\ [mV]$

$N_{d/a} = V_{d/a} / V_{d/a\ step}$

$N_{d/a} = 6530.1 / 10 = 653.01$

$N_{d/a} =$ **654 [clocks]**

(d) The conversion time will be when the $CLOCK_T = 1\ \mu s$:

$T_{conversion} = N_{d/a} * CLOCK_T$

$T_{conversion} = 654 * 1 =$ **654** μs

(e) If A/D is a successive-approximation, the conversion time is as follow:

$T_{conversion} = N_{d/a\ bit} * CLOCK_T$

$T_{conversion} = 10$ [bits] $* 1$ [us] = **10** μs

3. Solution for question 3

(a) The three main blocks in Phase Locked Loop circuits are:
1. Phase comparator
2. Low pass filter
3. Voltage controlled oscillator

The voltage at the output of the comparator is defined as:

$$V_1 = K_p (\theta_0 - \theta_i) \qquad [1]$$

The voltage at the output of the comparator is proportional to the difference of the input frequency and voltage controlled frequency.

The transfer function of the filter is defined as:

$$V_2 / V_1 = - (R_F + 1/j\omega C)/ R_1 \qquad [2]$$

The output voltage V2 integrates fast changes from the phase comparator.

The transfer function for the voltage controlled oscillator is defined as:

$$\theta_0 = e^{j\omega t}$$

$$d\theta_0 / dt = K_o V_2 = j\omega \theta_0 \qquad [3]$$

The frequency at the output of the voltage-controlled oscillator is proportional to the input voltage V2.

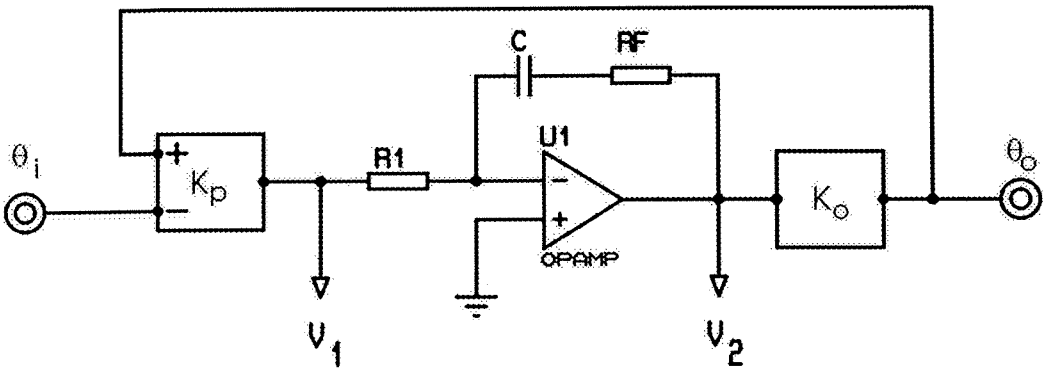


Fig 8.

(b) From [2] and [3] follows:

$V_2 = - V_1(R_F + 1/j\omega C)/ R_1$

$K_o V_2 = j\omega \theta_0$

$-K_o V_1(R_F + 1/j\omega C)/ R_1 = j\omega \theta_0$

From [1] $V_1 = K_p (\theta_0 - \theta_i)$ follows:

$-K_o K_p (\theta_0 - \theta_i) (R_F + 1/j\omega C)/ R_1 = j\omega \theta_0$

$-K_o K_p (\theta_0 - \theta_i) (j\omega C R_F + 1) / j\omega C R_1 = j\omega \theta_0$

$-K_o K_p j\omega C R_F\theta_0 - K_o K_p \theta_0 + j K_o K_p \omega C R_F \theta_i + K_o K_p \theta_i = -\omega^2 C R_1 \theta_0$

$\omega^2 C R_1\theta_0 - K_o K_p j\omega C R_F\theta_0 - K_o K_p \theta_0 = - j K_o K_p \omega C R_F \theta_i - K_o K_p \theta_i$

$\theta_0 (K_o K_p + j K_o K_p \omega C R_F - \omega^2 C R_1) = (jK_o K_p \omega C R_F + K_o K_p)\theta_i$

$\theta_0 / \theta_i = (K_o K_p + j K_o K_p \omega C R_F) / (K_o K_p + j K_o K_p \omega C R_F - \omega^2 C R_1)$

$\theta_0 / \theta_i = 1 / [1 - \omega^2 C R_1 / (K_o K_p + j K_o K_p \omega C R_F)]$

$\theta_0 / \theta_i = 1 / [1 - \omega^2 C R_1 / (j K_o K_p (\omega C R_F - j))]$

$\mathbf{\theta_0 / \theta_i = 1 / [1 + j \omega^2 C R_1 / (K_o K_p (\omega C R_F - j))]}$

(c) when $R_F = R_1$ and C is infinite

equation

$\theta_0 / \theta_i = 1 / [\ 1 + j\ \omega^2 C R_1 / (K_o\ K_p\ (\omega C\ R_F - j\ ))]$

can be rearranged so:

$\theta_0 / \theta_i = 1 / [\ 1 + j\ \omega^2 C R_1 / (K_o\ K_p \omega C\ R_F\ (\ 1 - j / \omega C\ R_F\ ))]$

and

$\theta_0 / \theta_i = 1 / [\ 1 + j\ \omega / (K_o\ K_p\ (\ 1 - j / \omega C\ R_F\ ))]$

$\theta_0 / \theta_i = 1 / [\ 1 + j\ \omega / K_o\ K_p\ ]$

then bandwidth of the locked loop is defined as

$B = K_o\ K_p$

(d)

(i) The block diagram of the frequency synthesizer is presented in Fig 9.

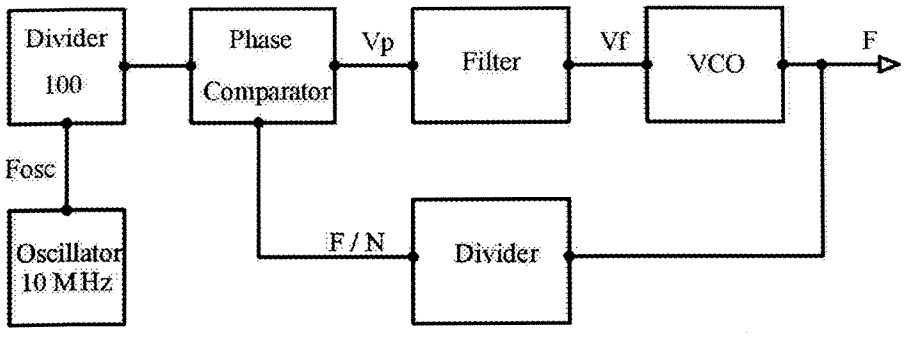


Fig 9.

The oscillator generates reference frequency Fosc = 10 MHz.
Divider 100 divides Fosc by 100 generating 100 kHz.
The Phase comaparator generates voltage Vp which is directly proportional to the difference of the Fosc and F / N.
The Filter integrates sharp changes in Vp.
The VCO is Voltage Controlled Oscillator, generating Frequency F.

Divider generates frequency F/ N.

(ii)

Vp = Kp(F/N – Fosc/ 100)

For locked frequency Vp must be equal zero:

F / N = Fosc / 100

F = N Fosc / 100

For requested range 100 – 200 MHz with reference frequency 10 Mhz the divider is as defined :

$$N_{min} = 100 \ F_{min} / Fosc$$

$$N_{max} = 100 \ F_{max} / Fosc$$

$$N_{min} = 100 \ 100 / 10$$

$$N_{min} = 1000$$

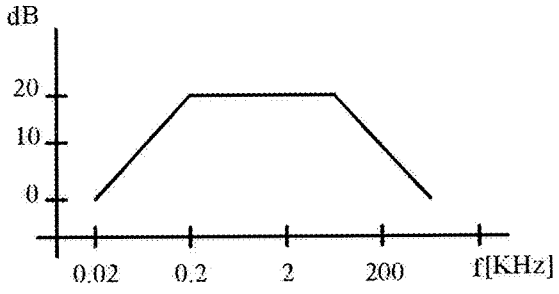
$$N_{max} = 100 \ 200 / 10$$

$$N_{max} = 2000$$

$$1000 <= N <= 2000$$

4. Solution for question 4

(a) (plot diagram starting at 200 Hz and end to 10^5 (roll-off points)



So –3dB bandwidth is 200 Hz to 100 kHz

LF = 200 Hz HF = 100 kHz (Turn over frequencies)

(b) Consider the amplifier A_2; input V_2 and input resistance R_3 and feedback impedance 1/sC give the output

$$V_0 = - V_2 / sCR_3$$

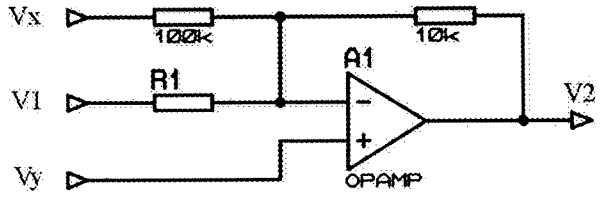
Similarly the output of amp A3

$$V_x = V_2 / (sCR_3)^2$$

The output of A2 is also fed to A1 whose non-inverting input is therefore

$$V_y = -V_2 R_2 /[sCR_3(R_2 + 10^5)]$$

So the signals into A1 are as below



Being a high-gain amplifier, the signal at the inverting input of the A1 is very close to V_y so KCL(2) = >

$$(V_1-V_y)/R_1 + (V_x-V_y)/ 10^5 + (V_2 - V_y)/10^4 = 0$$

$$V_1 / R_1 = -V_2 (1/ 10^4 + V_x/ 10^5 - V_y(1/R_1 + 1/10^4 + 1/10^5))$$

$V_1 = -V_2R_1/10^4(1 + 1/(10(sCR_3)^2) + 1/(sCR_3) * R_2/(R_2+ R_5) * (1 + 0.1 + 10^4/ R_1))$

(c) Using the rewritten expression

$$V_1 = V_2 / A * (1 + 3\omega_0/s + 3\omega_0^2/s^2)$$

By comparing terms; $A = 10^4 / R_1 \Rightarrow R_1 = 10^4 / A = 1\ k\Omega$

The $1/ s^2$ term gives

$$3\omega_0^2= 1/(C^2 R_3^2 10)$$

So $R_3 = 1 / (30^{1/2}C\omega_0) = 1 / (30^{1/2} 10^{-8} 2\pi 200) = 14.53\ k\Omega$

The 1/s term gives $3\omega_0 = 1/(CR_3) * R_2/(R_2+ R_5) * (1 + 0.1 + 10^4/ R_1))$

Which leads to $3\omega_0 CR_3 / (1 + 0.1 + 10^4/ R_1) = R_2/(R_2+ R_5)$
By inverting $(R_2+ R_5)/ R_2 = (1 + 0.1 + 10^4/ R_1)/ 3\omega_0 CR_3$
And $R_5 / R_2 = (1 + 0.1 + 10^4/ R_1)/ 3\omega_0 CR_3 - 1$
Then $R_2 = R_5 / ((1 + 0.1 + 10^4/ R_1)/ 3\omega_0 CR_3 - 1)$

Substituting values $R_2 = 5.24\ k\Omega$

So R_3 sets the frequency and R_1 sets the Gain

(d) High pass filters are particularly prone to emphasising any noise picked up. The Bessel response is best, when signals are pulses with Butteworth and Chebyshev has ringing at pulse input –is worse.

5. Solution for question 5

(a) The diode rectifier is presented in Fig – diode rectifier.

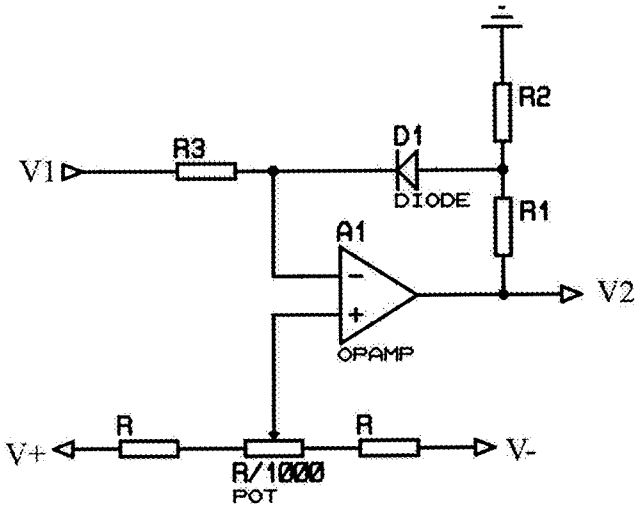


Fig – diode rectifier.

$$V_2 = (R_1 + R_2) * V_d / R_2$$

Diode points towards the input.

When it conducts I_d for (-) polarity input, (+) polarity output are given.

(b) Input resistance => $R_3 = 2\ k\Omega$ (virtual earth amplifier)

Naw diode current => $I_d = V_1 / R_3$

Using the unloaded potential divider expression

$$V_2 [R_2 /(R_1 + R_2)] = V_d = 0.06 (\log_{10} V_1 - \log_{10} I_s R_3)$$

$$V_2 = (R_1+R_2)/R_2 * 0.06 \log_{10} V_1 \qquad (1)$$

provided that other term is nulled by offset trim.

The wanted result is:

$V_2 = 2 \log_{10} V_1$

Then from (1)

$(R_1+R_2)/R_2 * 0.06 = 2$

or

$R_1 / R_2 = 32.2$

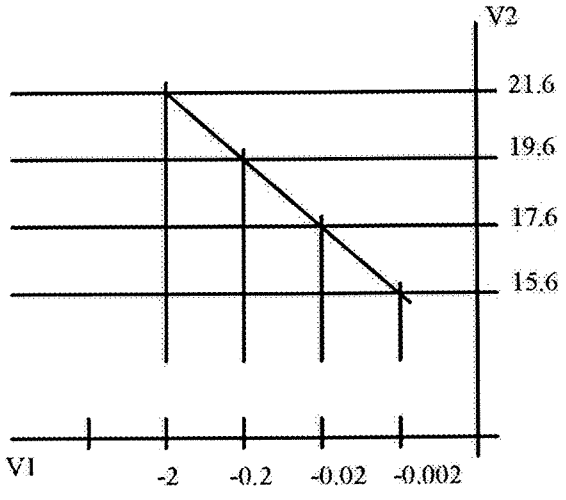
By selecting => $R_1 = 1000\ \Omega$ then

$R_2 = 1000/32.2 = 31\ \Omega$

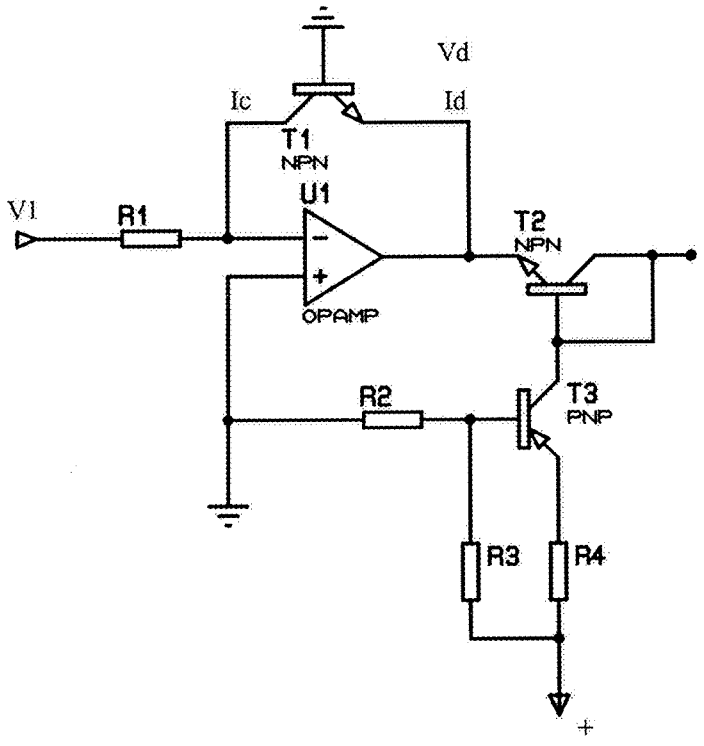
Low impedance wanted so that the Thevenian equivalent in the output of the divider has some resistance ~ 31 Ohm which is low and does not add significantly to the diode slope resistance. However, low resistance R_1 draws current from the op amp. (Note usually ~25 mA)

(c) Now consider the max diode conditions:
$I_d = 1$ mA transfers to V1 = -2V
$V_d = 0.65$ V transfers to $V_2 = 21.65$ V (output)

(checks (just) with 25 mA output current



(d) Transistor can be bought in well matched pairs in terms of leakage current I_s, they are close so they track each other in temperature which raises I_s.



Transistor T2, connected as a diode which gives an offset when $V_d = \log_{10} I_s R$ of the first stage.
Transistor T1 connected as transistor-diode (Collector is on virtual earth and base on real earth). However I_c= flows through R_1 and since

$$I_c / I_b = h_{fe} \text{ and } I_d = I_c + I_b = I_c / H_{fe} + I_c = V_{in} / R_1 (1 + 1/h_{fe})$$

If $h_{fe} \sim 200$ than error is 0.5% (so that element can be nulled so that current through the transistor T_1 depends only on input voltage and input resistance).

$$I_d = V_{in} / R_1$$