ENGINEERING TRIPOS PART IIB

ELECTRICAL AND INFORMATION SCIENCES TRIPOS PART II

Saturday 26 April 2003 9 to 10.30

Module 4B2

POWER ELECTRONICS AND APPLICATIONS

*Answer not more than **three** questions*

All questions carry the same number of marks

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin*

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1 (a) Explain carefully the terms *conductivity modulation* and *injection efficiency* in a semiconductor device. How are these effects be related? Using these terms, discuss the on-state voltage of a converter grade thyristor. [40%]

(b) Compare the physical mechanisms occurring in high voltage thyristors and diodes at turn off. Illustrate your answer with appropriate sketches of the mobile carrier distribution. [30%]

(c) How may carrier lifetimes be controlled in power semiconductors? With respect to a fast soft-recovery diode and a converter grade thyristor, describe briefly the desired effects of carrier lifetime control. [30%]

2 (a) For turn off in MOSFETs with inductive loads and simple gate drives, describe briefly the conditions which lead to the distinct features seen in the gate voltage. [30%]

(b) Give two reasons why snubbers are rarely used in MOSFET circuits. [20%]

(c) A MOSFET chopper circuit is shown in Fig. 1. The switching frequency is 300 kHz, the turn on snubber is 1.6 μH and the turn off snubber is 0.064 μF. If the inductive load current is 10 A, calculate the power losses at turn off. The MOSFET current may be assumed to fall linearly in 100 ns.

Find the peak overshoot drain-source voltage appearing across the MOSFET. [40%]

Comment briefly on the advantages and disadvantages of this design. [10%]

(cont./

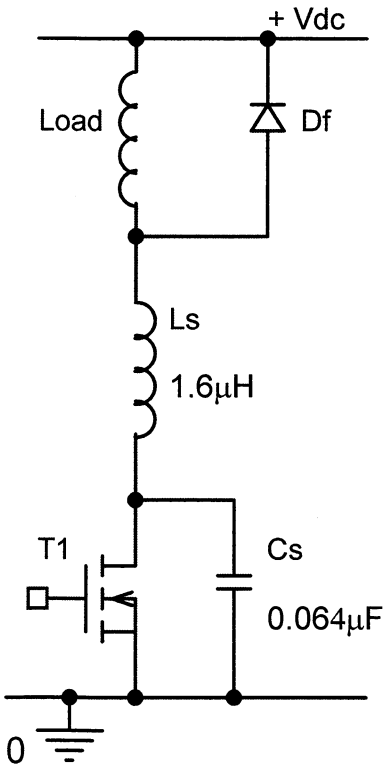

Fig. 1

(TURN OVER

3 (a) Sketch the excess carrier distribution in an IGBT at full current. Carefully explain the behaviour of the IGBT during turn off in a simple chopper circuit with an inductive load and a typical gate drive, making reference to further carrier distributions added to your sketch.

Explain briefly why the excess carriers may be represented by an additional parallel collector-emitter capacitance. [40%]

(b) A pair of IGBT chips are connected in parallel as shown in the circuit of Fig. 2, which includes the stray emitter connection inductances L_S. Under certain conditions, the parasitic gate-emitter, collector-emitter and collector-gate capacitances are 10 nF, 1 nF and 1 nF respectively, the transconductance of each IGBT, g_m is 12 S and the value of L_S is 10 nH . The gate resistance Rg is negligible. Draw an equivalent circuit describing small signal operation.

Extract the half circuit appropriate for describing differential mode small signal operation for a constant voltage V_G supplying the gate and a constant load current. Hence derive an equation describing small signal changes in the gate-source voltage of one transistor and estimate the characteristic frequency of oscillation. [40%]

Redraw your small signal half circuit to include a gate resistor in series with the gate connection to each chip. Suggest one disadvantage of this approach for stabilising the parallel operation of IGBT chips. [20%]

(cont./

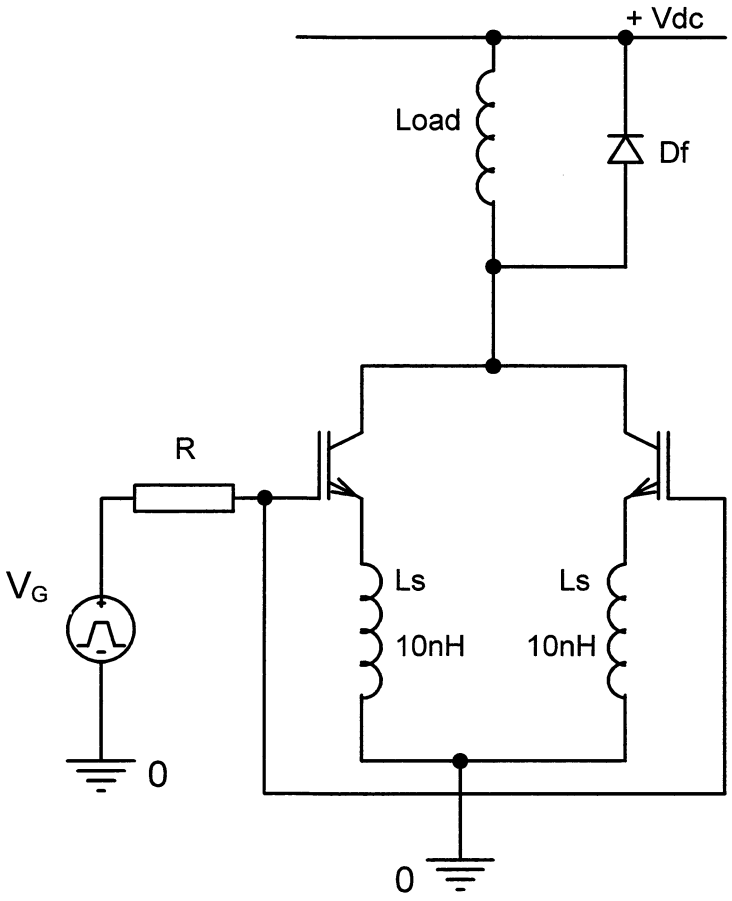

Fig. 2

(TURN OVER

4 (a) Sketch a lateral MOSFET constructed using the Reduced Surface Field (RESURF) principle. On your sketch, carefully identify the main features of the design which allow a high off-state voltage and high dv/dt at switching. [30%]

(b) Fig. 3 shows a novel dual gate lateral MOS device. Consider the action of the two gates and state the modes in which the device may operate.

Sketch timing waveforms for the two gates and describe the operation of the device. Illustrate your answer using current and voltage switching waveforms. [50%]

List the features necessary for a low on-state voltage and good switching properties. [20%]

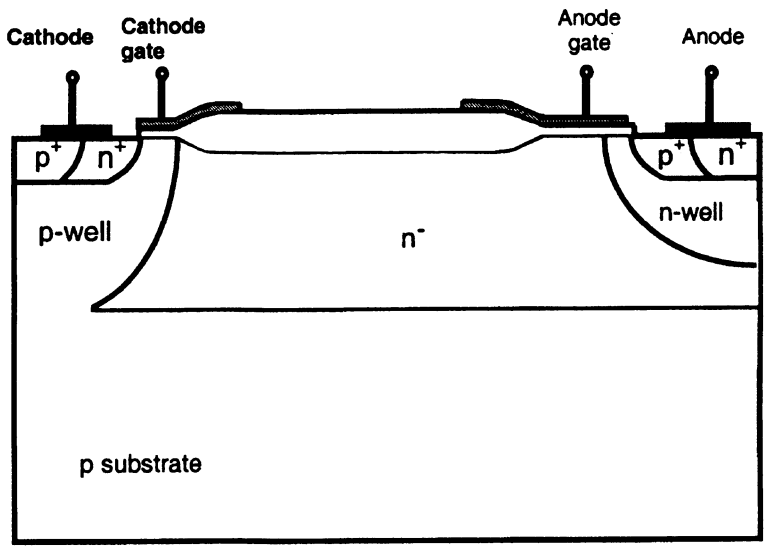

Fig. 3

5 Contrast and compare the possible use of MOSFETs, Bipolar Junction Transistors and IGBTs in the principal power circuits for the following applications :

(a) An uninterruptable power supply (UPS) operating from batteries at 24 V for use with a PC; [25%]

(b) An inverter for a high frequency resonant 'electronic' ballast for an 14 W compact fluorescent light; [25%]

(c) An industrial inverter (415 V ac input) rated at 3 kW ; [25%]

(d) A 300 V, 30 kW electric drive system for a hybrid car. [25%]

Make brief reference to the likely gate drive circuits and consider the efficiency and costs associated with each device.

END OF PAPER