ENGINEERING TRIPOS PART IIB
ELECTRICAL AND INFORMATION SCIENCES TRIPOS PART II

Monday 5 May 2003 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right hand margin.*

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1 (a) Describe briefly the extra process steps involved in the SOI CMOS VLSI technology and explain the advantages and drawbacks of this technology when compared to standard n-well, p-well and twin-tub CMOS technologies. [30%]

(b) Explain why CMOS devices made using a twin-tub process are less prone to static latch-up when compared to those made in p-well or n-well processes. [20%]

(c) The cross section of a CMOS inverter cell made in a specialised technology based on a combination of SOI and p-well VLSI technologies is shown in Fig. 1.

A copy of Fig. 1 is attached at the end of this paper for use as an answer sheet. On the answer sheet copy of the cross-section, draw the equivalent circuit responsible for the latch-up showing specifically the transistor terminals, parasitic resistors and the connections between them. Which of the parasitic transistors is more likely to trigger the latch-up, and why? [30%]

Write down the static condition for the latch-up to occur as a function of the electrical parameters of the parasitic components. [20%]

(cont.

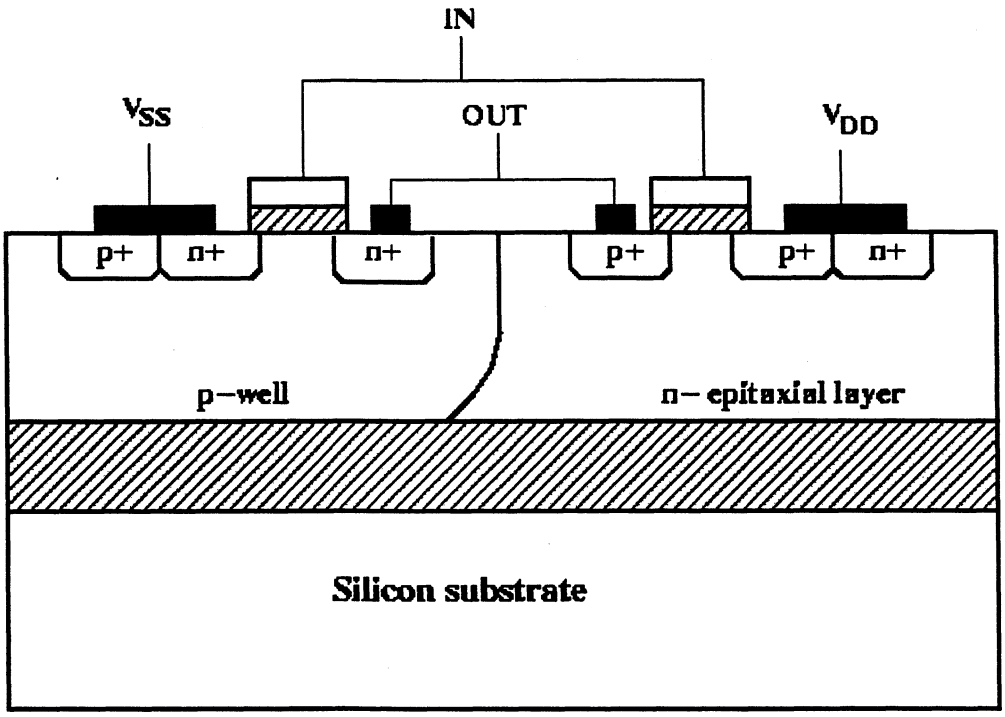


Figure 1

(TURN OVER

2. (a) Describe briefly the photolithography process in standard VLSI technology. Comment on the current status of photolithographic resolution. [30%]

(b) An incomplete layout of a 2-input CMOS gate is shown in Fig. 2. The power rails V_{DD} and V_{SS} are represented by the metal lines labelled A and E respectively.

On the copy of Fig. 2 provided at the end of this paper as an answer sheet, add the polysilicon layers (B and C) and the output metal layer (D) to obtain a logic gate. What logic function would be most appropriate to describe this layout design? [25%]

(c) State the conductivity type of the MOS transistors and explain the reasons for the upper transistors to have a wider active region. [15%]

(d) No well has been included in Fig. 2. If the substrate is n-type, state the conductivity type of the well and show on the answer sheet copy where it should be placed. [10%]

(e) Sketch a cross-section along the line $x = 42$ from the point $y = 40$ to the point $y = 80$ and clearly identify the various conductor, semiconductor and insulating regions. [20%]

(cont.

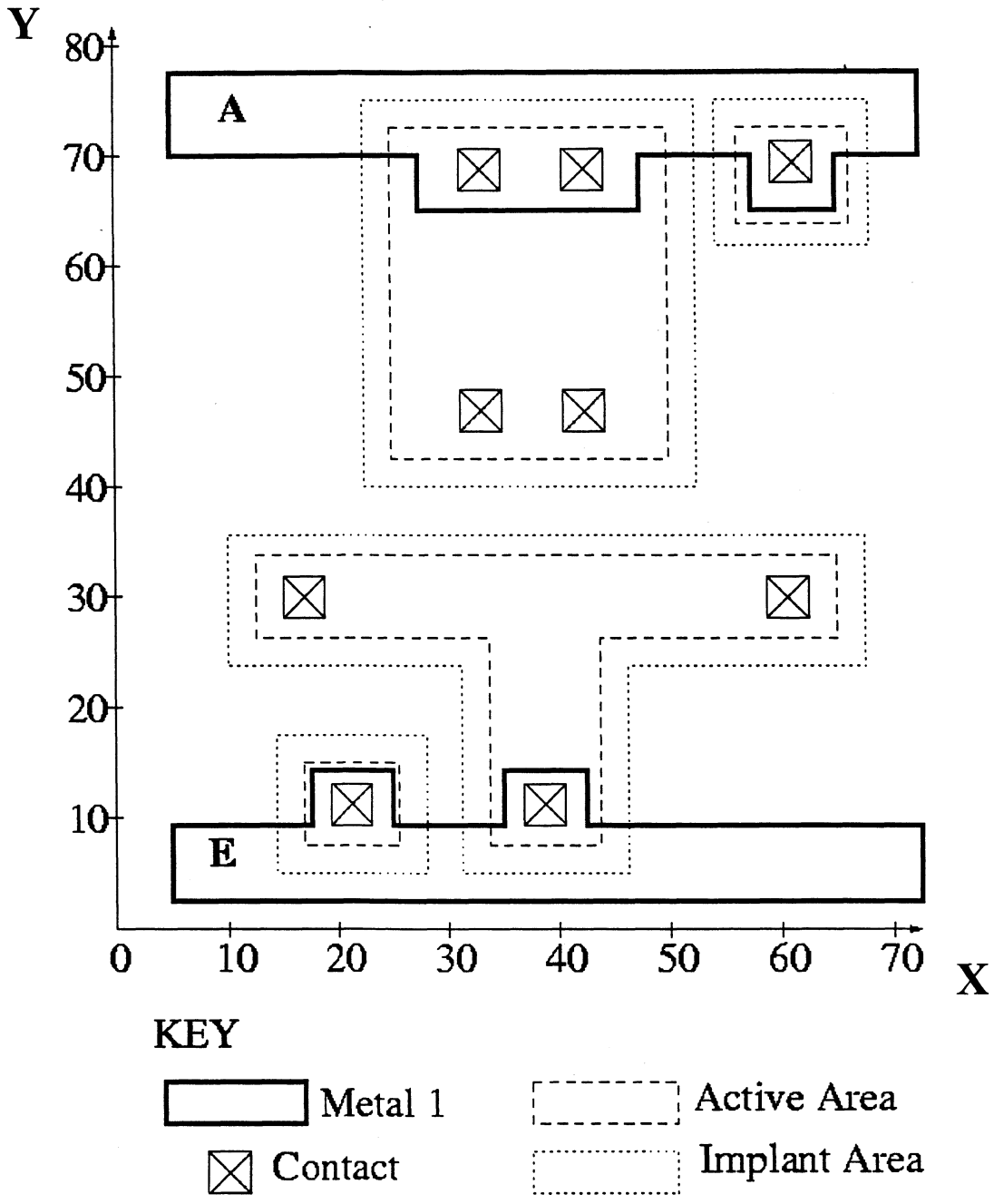


Figure 2

(TURN OVER

3 Figure 3 shows a current mirror circuit fabricated from n-channel MOS transistors.

(a) Show that, under appropriate conditions, the current I_2 passing through the load R_L depends only on the current I_1 and the dimensions of the active regions of the transistors M1 and M2. State any assumptions made. [30%]

(b) Explain why lithographic tolerances and fabrication process variations may result in I_2 deviating from the design value, and discuss measures that can be taken by the designer to alleviate certain of these difficulties. [20%]

(c) Determine suitable relative dimensions for the active devices if I_2 is required to be 400 μA when I_1 is 100 μA. [30%]

(d) What main factors govern the output resistance of a current generator designed in this way? Suggest a simple means by which the output resistance characteristic of the generator in Fig. 3 might be improved by inclusion of additional components. [20%]

You may assume the following expressions for the drain current I_D in a MOS transistor, where the symbols have their conventional meaning.

$$I_D = \frac{\mu\varepsilon}{t_{OX}}\frac{W}{L}\left((V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right) \qquad 0<V_{DS}<V_{GS}-V_T$$

$$I_D = \frac{1}{2}\frac{\mu\varepsilon}{t_{OX}}\frac{W}{L}(V_{GS}-V_T)^2 \qquad 0<V_{GS}-V_T<V_{DS}$$

(cont.

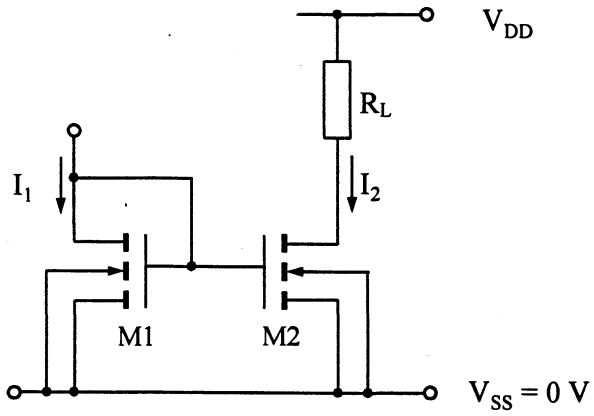


Figure 3

4. (a) What is the meaning of the term *clock skew* in the context of digital VLSI designs using CMOS technology? [10%]

(b) Draw a diagram to show how a form of 1-bit dynamic memory cell may be constructed using only a single MOS transistor and parasitic capacitance elements. Describe briefly how your circuit operates for *read* and *write* operations. [30%]

(c) Explain how the phenomenon of *charge sharing* may lead to incorrect operation of a dynamic memory cell. Deduce an appropriate condition, based on estimation of capacitance, which will ensure satisfactory operation. What measures are taken in the design and fabrication of practical dynamic memories to minimise these kinds of problem? [30%]

(d) The storage element in a dynamic memory has capacitance 60 fF and is charged to 5 V. A leakage current of 0.1 nA flows from the storage element to substrate. Stating any assumptions made, estimate how frequently the data stored in the memory needs to be refreshed. The storage element is switched onto a bit sense line of capacitance 1.5 pF, precharged to 2.5 V. What is the instantaneous change in potential observed on the sense line? [30%]

5 (a) Explain the meaning of the terms *sheet resistance*. Show how this concept can be used during the design of an integrated circuit to predict the resistance of electrical interconnects containing a number of right-angle bends. [30%]

(b) Discuss the origin of *body effect* or *back gating*, as encountered with MOS transistors. How does this phenomenon affect the measured characteristics of a transistor? By considering the circuits for two-input CMOS NAND and NOR gates, explain how the body effect influences:-

(i) logic levels and noise margins;

(ii) gate delay. [40%]

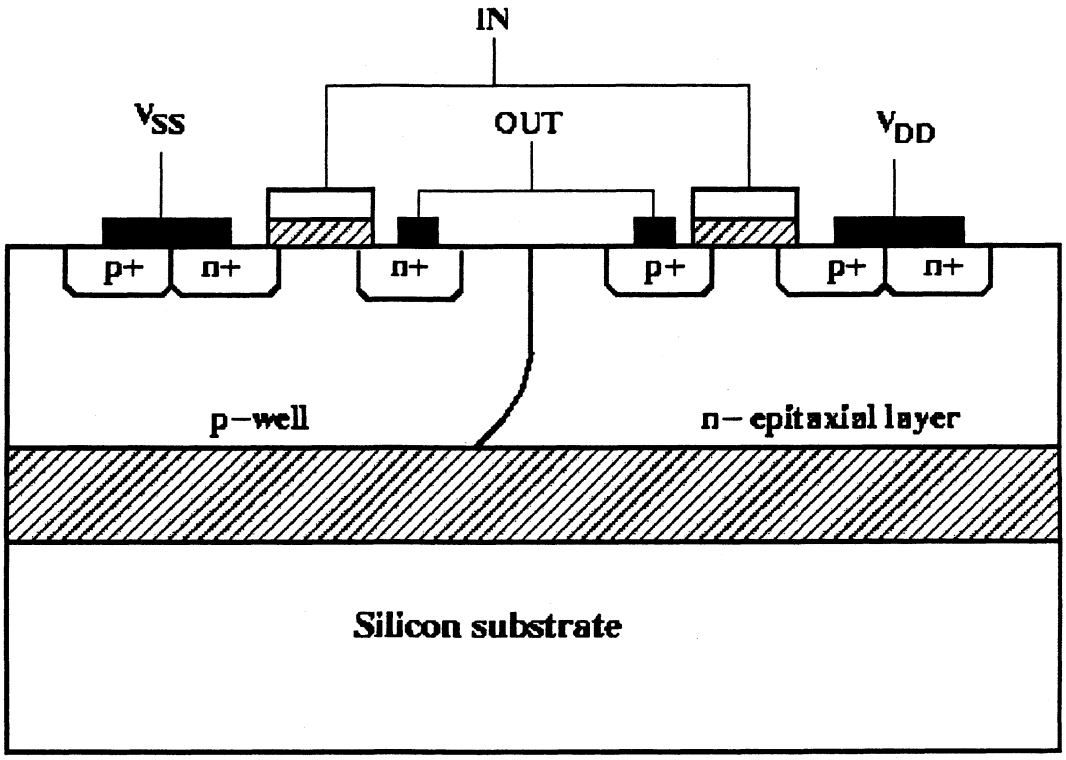
(c) Give a simple explanation of the phenomenon of *electromigration* and the factors affecting its appearance. What steps can the integrated circuit designer take to alleviate its effects? [30%]

END OF PAPER

ENGINEERING TRIPOS PART IIB

Monday 5 May 2003 2.30 to 4

Module 4B7 – VLSI DESIGN, TECHNOLOGY AND CAD



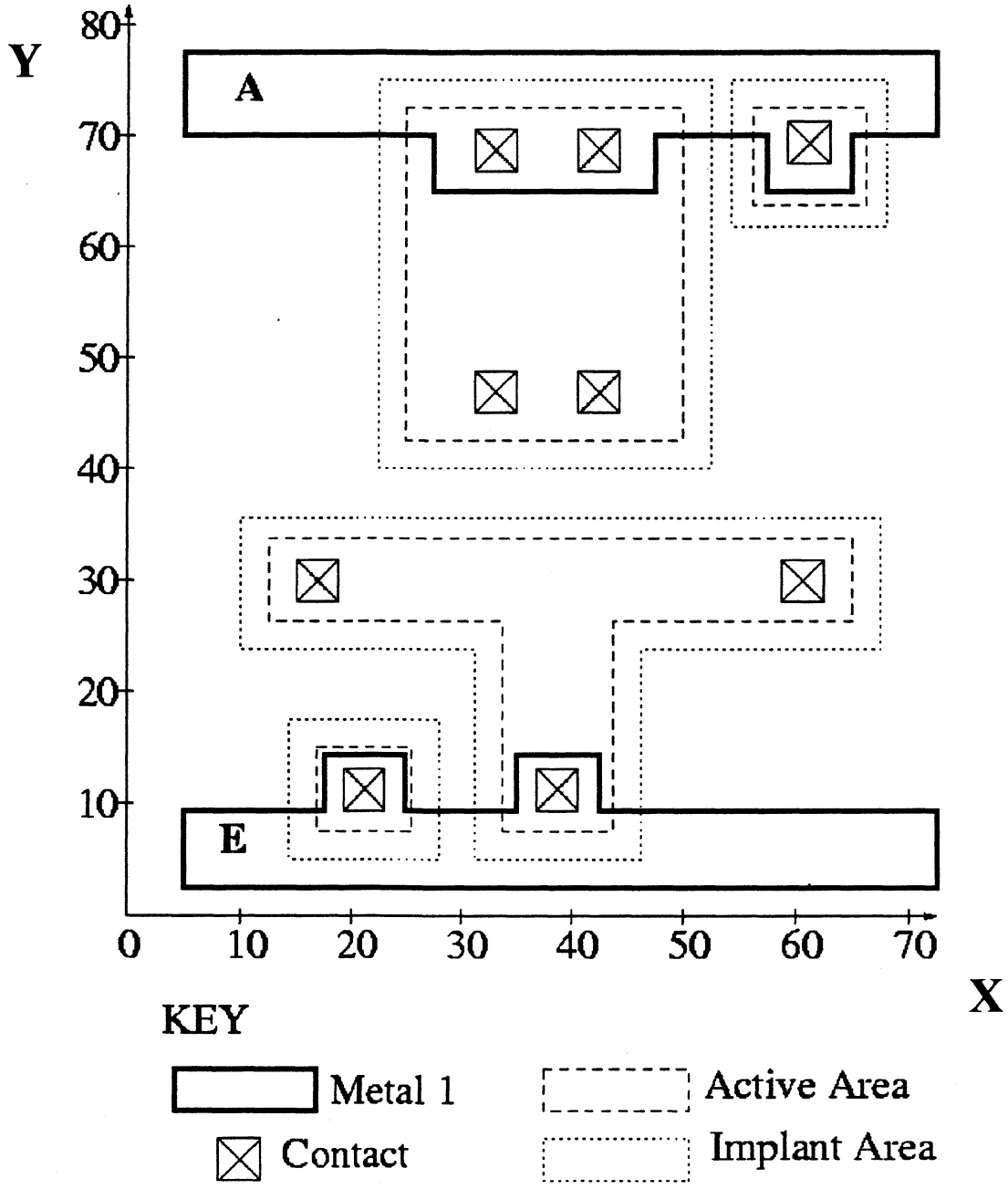
Answer sheet for Q 1

(may be handed in with your script)

ENGINEERING TRIPOS PART IIB

Monday 5 May 2003 2.30 to 4

Module 4B7 – VLSI DESIGN, TECHNOLOGY AND CAD



Answer sheet for Q 2

(may be handed in with your script)