ENGINEERING TRIPOS PART IIB
ELECTRICAL AND INFORMATION SCIENCES TRIPOS PART II

Wednesday 23 April 2003 9 to 10.30

Module 4B8

ELECTRONIC SYSTEM DESIGN

Answer no more than ***three*** *questions.*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) An operational amplifier is used in a non-inverting configuration as presented in Fig 1. Assuming that the operational amplifier is ideal show that

$$V_o = V_e (1 + R_2 / R_1)$$

where:

V_o = output voltage
V_{in} = input voltage
V_e = noise voltage [20%]

(b) Show that for the amplifier in Fig 2., in order to minimise bias current I_b, the value for the resistor R is defined with following relation:

$$R = (R_1R_2) / (R_1 + R_2)$$ [30%]

(c) An operational amplifier has two poles in its frequency response, at frequency ω_1 and frequency ω_2. The open loop gain at DC is A_o. The layout of the amplifier is presented in Fig 3.

(i) Show that natural frequency for the closed loop response is :

$$\omega_n = [\omega_1\omega_2 (1 +\beta A_o)]^{1/2}$$

and damping factor is defined as:

$$K = (\omega_1 + \omega_2) / 2 \omega_n.$$ [30%]

(ii) If the poles are at 1 kHz and 10 kHz and the open loop gain at DC is 120 dB with negative feedback of $\beta = 0.5$ find the frequency at which the gain peaks and the magnitude of the peak. [20%]

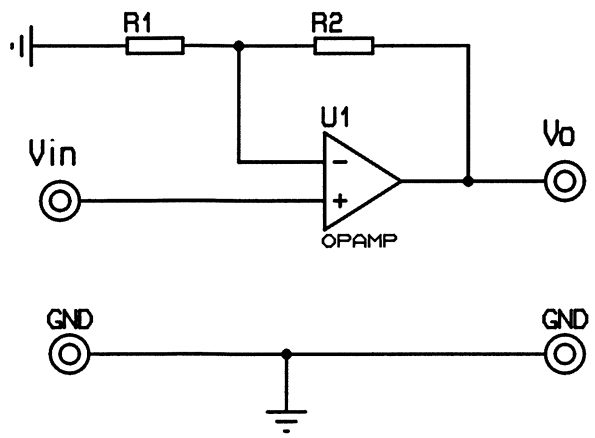

Fig. 1

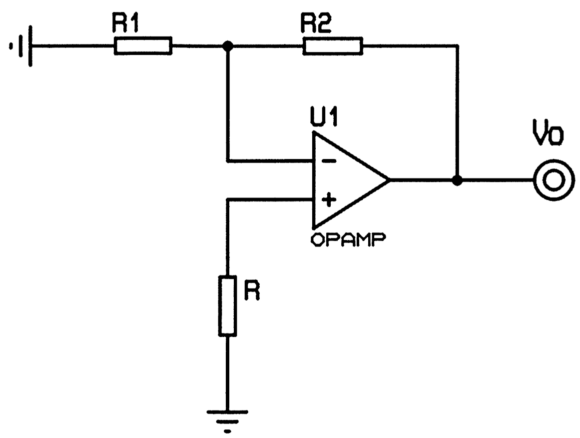

Fig. 2

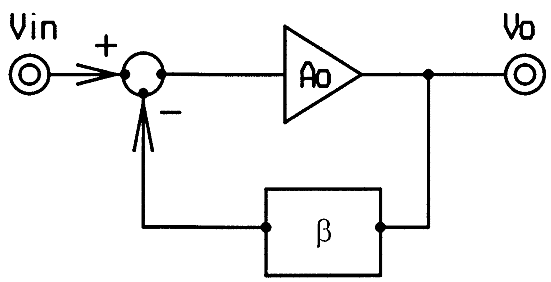

Fig. 3

2 Figure 4 shows an A/D converter with following characteristics:

- CLOCK = 1 MHz
- VT = 0.1 mV (Comparator threshold)
- F.S. = 10.23 V (Full scale D/A output)
- D/A 10 bit converter

(a) Describe the role of the pins A and B in A/D converter shown in Fig. 4. [10%]

(b) Describe the functioning of the A/D converter shown in Fig. 4 and draw the timing diagrams. [40%]

(c) If the input voltage V_{in} is 6.53 V, determine the input number at the D/A converter shown in Fig. 4. [20%]

(d) Calculate the conversion time for the input voltage V_{in} = 6.53 V. [10%]

(e) If the A/D converter in Fig. 4 were a successive-approximation A/D converter, calculate the conversion time when V_{in} = 6.53 V. [20%]

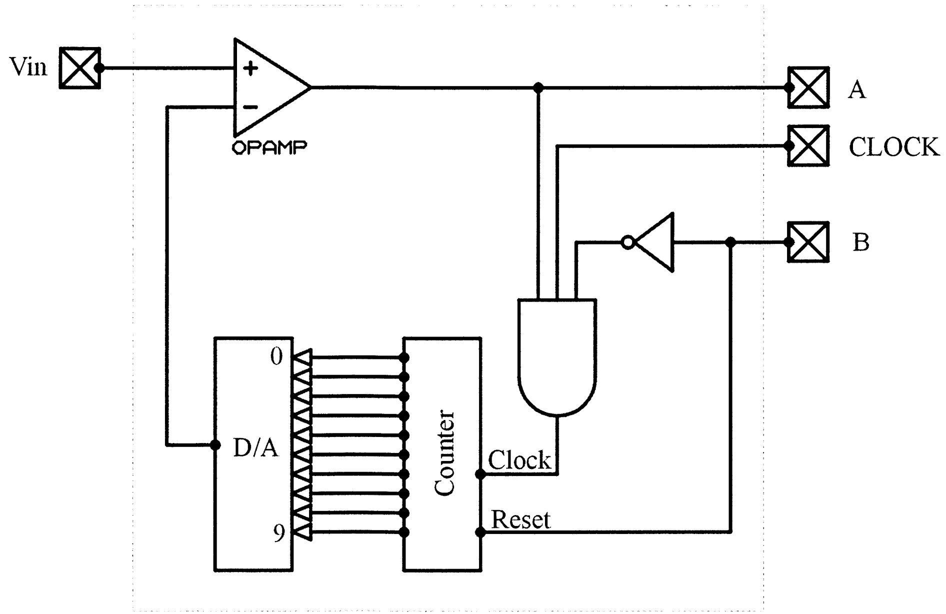

Fig. 4

3 (a) The block diagram of a Phase Locked Loop (PLL) is shown in Fig 5. Describe briefly the function of each block and give their transfer functions. [20%]

(b) For the block diagram of the PLL circuit in the question 3(a) derive the transfer function in terms of frequency. [30%]

(c) In the case that $V_2 / V_1 = -1$ derive the relation for the loop bandwidth B. [20%]

(d) You are requested to synthesize frequencies from 100 MHz to 200 MHz with resolution of 100 kHz using PLL (Phase Locked Loop) circuit. The frequency of the reference crystal oscillator is 10 MHz.

(i) Draw the block diagram and explain the role of each element within your block diagram. [20%]

(ii) Derive the transfer function in terms of frequency and calculate the divider range. [10%]

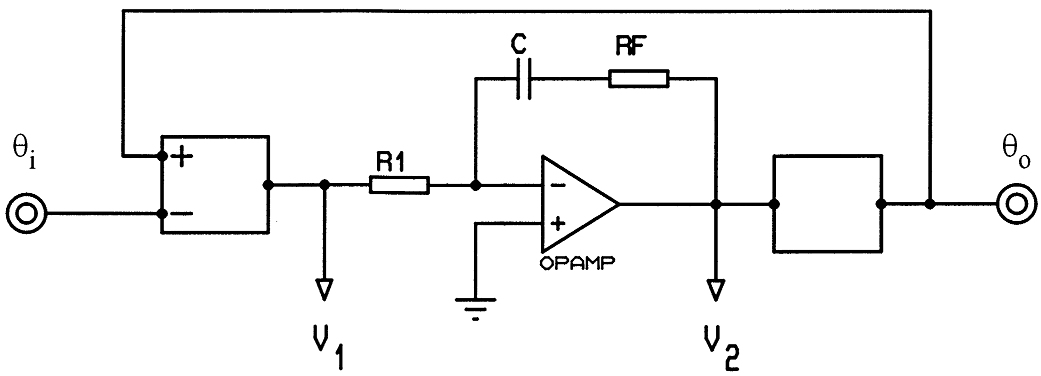

Fig 5.

4 A second order *high-pass* filter with a –3dB point at 200 Hz is to have a *numerical* gain of 10 in its passband. Op-amp types with a gain-bandwidth product of 10^6 are to be used.

(a) Draw a clear gain-frequency plot that you would expect for the filter overall. [20%]

(b) This system is to have a Bessel type response of the form:

$$V_2 / V_1 = As^2 /(s^2 + 3\omega_0 s + 3\omega_0{}^2)$$

It is to use the state-variable circuit shown in Fig. 6.

Assuming the s = jω notation, obtain an equation for the response of the circuit relating the output V_2 to the input V_1 and the values of the resistors and capacitors of the circuit at a frequency ω. [35%]

(c) It may be easier to have the relation from section (b) of this question rewritten as:

$$V_1 = V_2(1 + 3\omega_0 / s + 3\omega_0{}^2 / s^2) / A$$

Hence, or otherwise, obtain expressions and values for R_1, R_2 and the two equal value resistors R_3, if the filter uses two equal capacitors C of value 10 nF. Which resistor sets the gain and which sets the frequency? [35%]

(d) Explain briefly any problem which may arise in using the filter circuit shown in Fig 6. For what particular signal type is a Bessel response best? [10%]

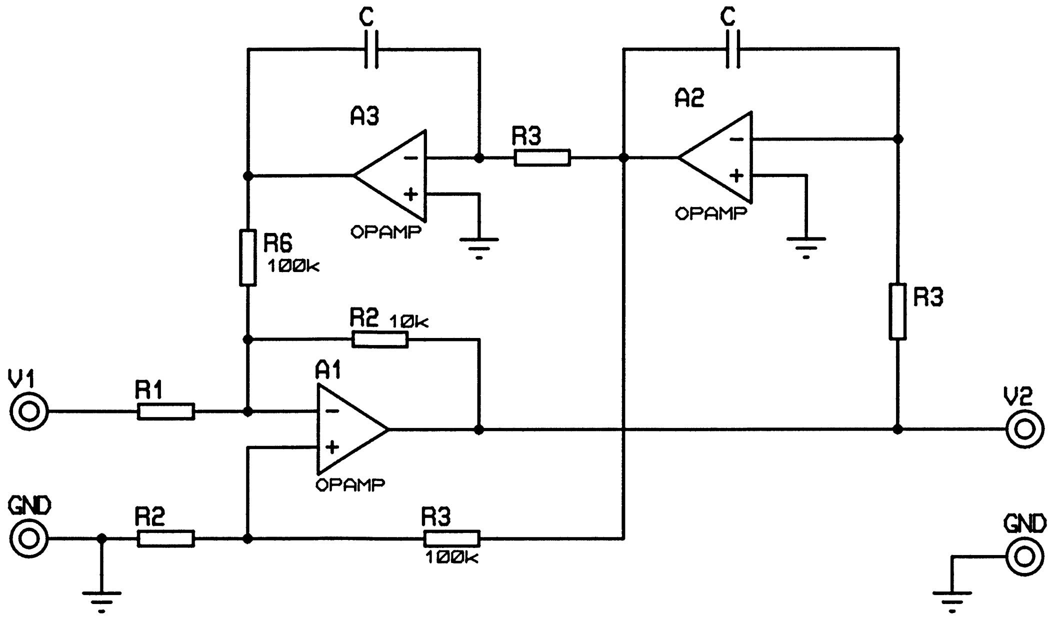

Fig. 6

(TURN OVER

5 (a) A *simple* logarithmic amplifier circuit is needed which, for a *negative* polarity input V_1, has an output V_2 which changes by $2V$ for each decade change of input. Draw a circuit diagram using a *single* op-amp putting brief notes on your circuit of its main features. [25%]

(b) The circuit is to have an input resistance of $2k\Omega$ and is to use a silicon diode of maximum forward current $I_D = 1mA$ at a forward voltage $V_D = 0.65$ V. Assume the usual diode equation:

$$V_D = 0.060 \log_{10} I_D / I_S$$

where I_S is the small reverse leakage current. Suggest values for the components of the circuit, explaining carefully the approximations that you are making. [35%]

(c) Sketch a graph of the output voltage against input voltage characteristic that you expect, marking a few salient values on your plot. [20%]

(e) What are the main reasons for using a matched transistor pair in a better logarithmic circuit? Show how such a transistor pair is connected. What other feature do the transistors need for good performance in the circuit? [20%]

END OF PAPER