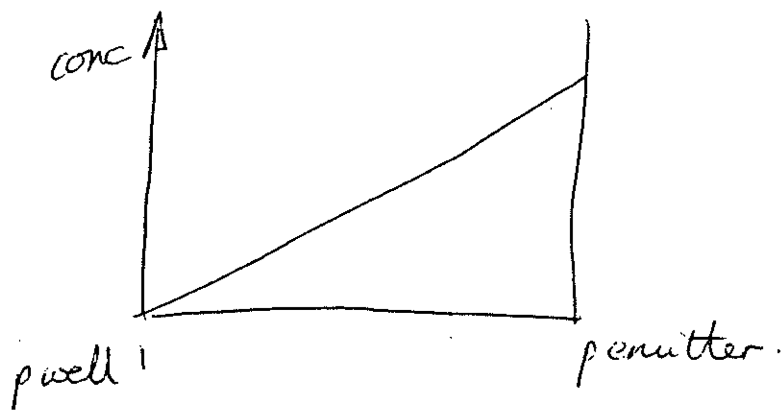
4B2 - 2004

Marks out of 20

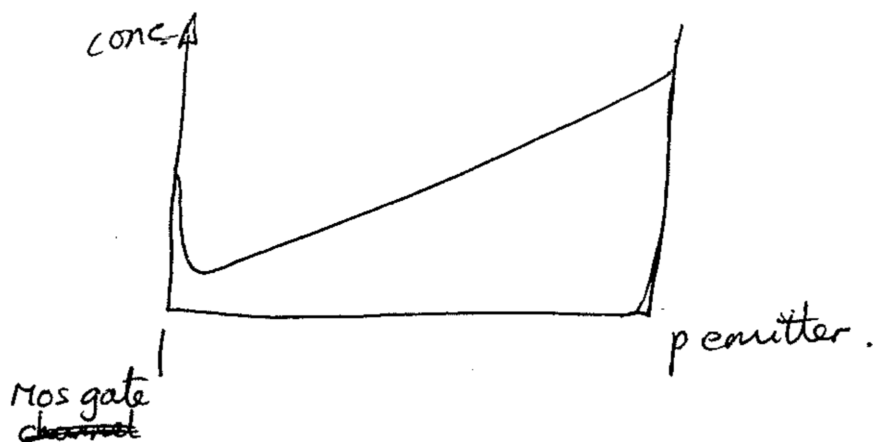
1(a) High voltage devices must contain the voltage with a p-n junction in reverse bias. A limitation is the max e-field possible, thus high voltages mean a wide depletion region, and therefore a wide lightly doped region. By definition this is quite resistive and incompatible with the idea of a switch. However, its resistivity may be reduced if a significant stored charge can be introduced. An injecting junction can achieve this and space charge neutrality implies that carriers of both types are stored, making it quite conductive, as desired. (4)

In an IGBT the electron current flows, inducing a hole current to flow from the p emitter into the n^- wide region. The electrons and holes charge up the n^-. Since the holes may exit fairly easily near the MOS channel due

to the short, the profile tends to be triangular.



holes cannot exit so easily from under the MOS gate so another profile apears in some devices.

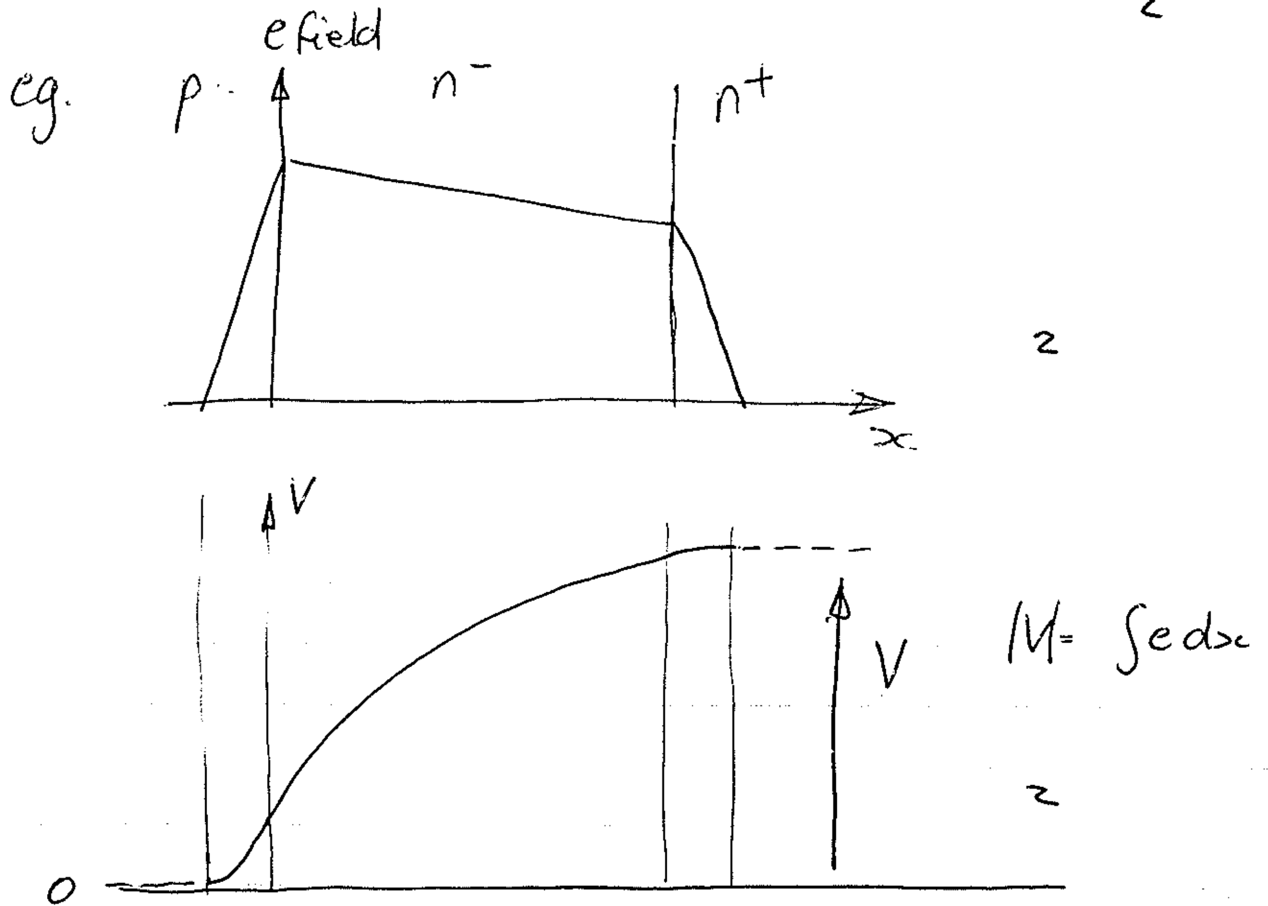


Since resistance is an inverse of concentration, the last low part is of great importance.

4

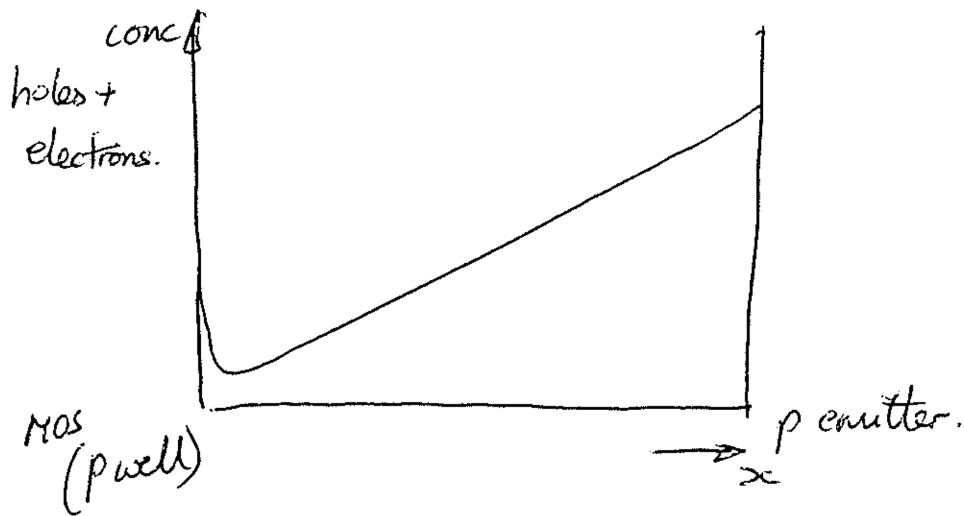
1(b) Buffer layers are incorporated to enclose the e field around a blocking junction. Used with a low doped region a high voltage can be contained in a minimal width. 2

eg.



Using an intrinsic layer would be most efficient but probably has other undesirable consequences.

1(c) Recall (a) above. – the on-state charge profile



Turn off requires that the supply of electrons is starved at the MOS end. The current is then maintained by an increased hole flow. Charge is quickly eaten away from the MOS end, and a depletion layer forms. [Initially Nothing changes at the p emitter end.] Eventually the volts have risen enough that the external circuit allows the current to fall. With less current, the supply of holes at the p emitter falls, and the level of charge cannot be maintained for the given recombination rate. Electrons are no longer

1(c) cont

supplied by the MOS channel OR the moving boundary at the depletion layer edge, so the level of electrons and holes tends to fall. 2

Once the charge at the p-emitter is reduced to a low value, high level injection ceases and only holes may flow. The electrons are now trapped. As they recombine with holes, holes are still being extracted at the edge of the depletion layer and supplied at the p emitter. This hole current is known as the tail current, and persists until the electrons have recombined. 2

Clearly it is reduced if the device is operated near its maximum voltage so the carriers are swept out properly. An alternative is to use anode shorts (electron sinks). Naturally reducing the conductivity modulation works well (eg. BJT)

Lifetime control

2

2(a) $\alpha_{pnp} I_A + \alpha_{npn} I_K + I_L = I_A$

KCL $I_K = I_A + I_G$.

$$\Rightarrow I_A = \frac{\alpha_{npn} I_G + I_L}{1 - \alpha_{npn} - \alpha_{pnp}}$$ 2

In the off state $\alpha_{npn} + \alpha_{pnp} < 1$

A positive gate current allows I_A to flow;

as I_A increases α_{npn} & α_{pnp} increase.

$\alpha = \gamma \delta M$ where γ is the emitter injection efficiency.

" δ is the base transport factor.

It is mostly the increase in γ that is important at turn on, and it increases with I_A to start with.

4

As it increases with I_A, it is possible to get current concentration. Reducing the $\frac{dI_A}{dt}$ stops this becoming a thermal runaway.

Since I_L is indistinguishable from $\alpha_{npn} I_G$

I_L must be kept low especially with a $C\frac{dV}{dt}$ 'leakage'. So limit $\frac{di}{dt}$ and $\frac{dV}{dt}$ with snubbers

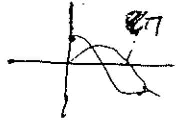
uneven unwanted 2

2(b)

Energy.

$\omega_0 = \frac{\pi}{\tau}$

$$\hat{V} I_{rr} \int_0^{\tau} \sin(\omega_0 t)(1 - t/\tau)\, dt^{2}$$



$$\int_0^{\tau} \sin\omega_0 t\, dt - \frac{1}{\tau}\int_0^{\tau} t \sin\omega t\, dt$$

$$-\frac{\cos\omega_0 t}{\omega_0}\Big|_0^{\tau}$$

$$+\frac{1}{\omega_0 \tau}\int t\, d\cos\omega t.$$

$$\frac{1}{\omega_0 \tau} t\cos\omega t - \frac{1}{\omega_0 \tau}\int \cos\omega_0 t\, dt$$

$$-\frac{1}{\omega_0 \tau}\frac{\sin\omega_0 t}{\omega_0}$$

$$= \hat{V} I_{rr}\left[-\frac{\cos\omega_0 t}{\omega_0} + \frac{1}{\omega_0 \tau} t\cos\omega_0 t - \frac{1}{\omega_0^2 \tau}\sin\omega_0 t\right]_0^{\tau\ (\omega_0\tau = \pi)}$$

dimensions are OK.

$$= \hat{V} I_{rr}\left[\frac{2}{\omega_0}\ \cos\omega_0\tau - \frac{1}{\omega_0^2\tau}\sin\omega_0\tau\right]$$

$$= \hat{V} I_{rr}\left[\frac{2}{\omega_0} + \frac{1}{\omega_0}\cdot -1\right] = \frac{\hat{V} I_{rr}}{\omega_0}$$

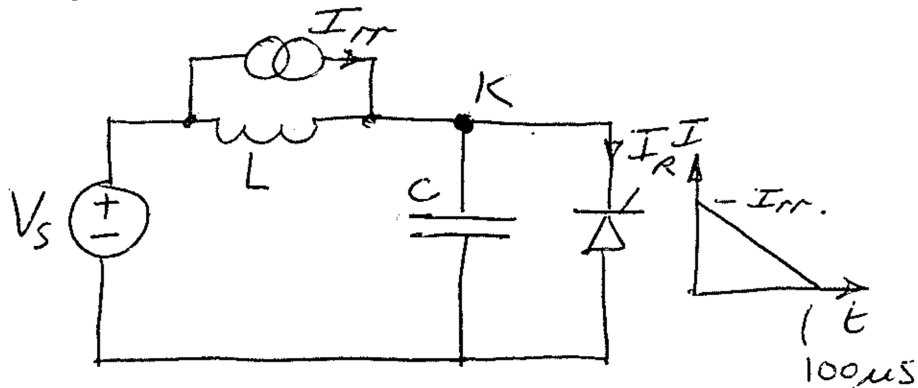
$$= \hat{V} I_{rr}\frac{\tau}{\pi}$$

Numbers. $3500 \times 500 \times \frac{100\mu}{3.14} \times 50\,Hz$

check $\frac{V_m I_m t_2}{2} \times 50 = 4375$ $= \underline{2785\,W}$ OK. high.

2(b) cont.

Whilst Fig 3 gives the subcircuit, it is much easier to redraw to include the initial current in L.



Σi at K.

$$I_{rr}(s) - I_R(s) - \frac{V_K(s)}{1/sC} + \frac{V_s(s) - V_K(s)}{sL} = 0$$ 2

$$\frac{I_{rr}}{s} - \frac{I_{rr}}{s} + \frac{I_{rr}}{s^2\tau} + \frac{V_s}{s^2L} = V_K(s)\left[sC + \frac{1}{sL}\right]$$

$$V_K(s) = \frac{sL}{(s^2LC+1)} \cdot \frac{1}{s^2}\left[\frac{I_{rr}}{\tau} + \frac{V_s}{L}\right] = \frac{1}{s(s^2LC+1)} \cdot (V_s + LI_{rr}/\tau)$$

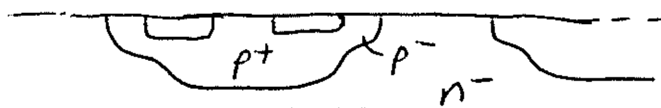
$$V_K(s) = \left(V_s + \frac{LI_{rr}}{\tau}\right)\left[\frac{1}{s} - \frac{LCs}{(s^2LC+1)}\right]$$

$$V_K(t) = \left(V_s + \frac{LI_{rr}}{\tau}\right)(1 - \cos\omega_0' t) \qquad \omega_0' = \frac{1}{\sqrt{LC}}$$

$$1500 = 2000(1 - \cos\omega_0' t) \qquad t = 100\mu s.$$

$$C = \frac{1}{L\omega_0'^2} \Rightarrow 57.6\mu F$$ 2 Huge!

3 (a). The MOS channel behaves in a classic MOSFET manner. However, the tight cell spacing means that the depletion layer quickly moves away from the gate overlap and consequently the end of the n-channel. (in p⁻ remember!) Hence, beyond a certain voltage, the channel dimensions (biasing) do not change with voltage. The relevant voltage depends on design but is around 10% of the total.

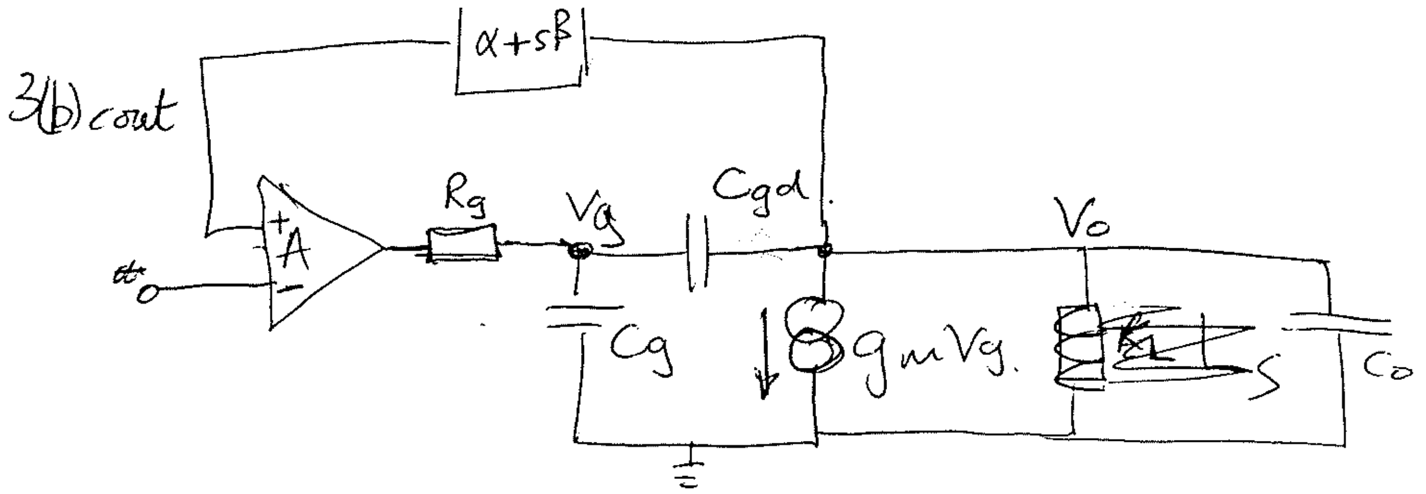


To make sure the p well does not punch through an extra diffusion is always added. 4

This is a p^+ diffusion which is important as it has a low lateral resistance — holes are accumulated at the drain end of the channel and the hole current tends to flow directly <u>UNDER</u> the electron current. To reduce the body effect and eliminate latch up the p well must have a low resistance 4

3(b). The low pass filter is made with R_G and C_{ies}. C_{ies} is heavily non-linear and takes on a very high value at low voltages. Thus the performance of the loop stabalised for high voltages (say at turn on) will be distinctly sluggish at turn-off at least until the collector volts have risen a bit, so C_{ies} falls. 4

C_{ies} is also current dependent as charge accumulates under the gate in an IGBT.



Neglect I_o

$$V_o = -g_m V_g \frac{1}{sC_o}$$

Σi at g.

$$\frac{V_o(\alpha + s\beta).A. - V_g}{R_g} + \frac{0 - V_g}{1/sC_g} + \frac{V_o - V_g}{1/sC_{gd}} = 0$$

4

3(b) cont.

$$V_o\frac{(A\alpha + sA\beta)}{R_g} - \frac{V_g}{R_g} - sC_g V_g + V_o sC_{gd} - sC_{gd}V_g =$$

$$-\frac{g_m V_g}{sC_o R_g}(A\alpha + sA\beta) - \frac{V_g}{R_g} - V_g . s(C_g + C_{gd}) - g_m \frac{sC_{gd}V_g}{sC_o} = 0$$

$\times$ by $-sC_oR_g$

$$g_m V_g (A\alpha + sA\beta) + V_g sC_o + V_g . s^2(C_g + C_{gd})C_oR_g + \frac{V_g}{} g_m sC_{gd}R_g = 0$$

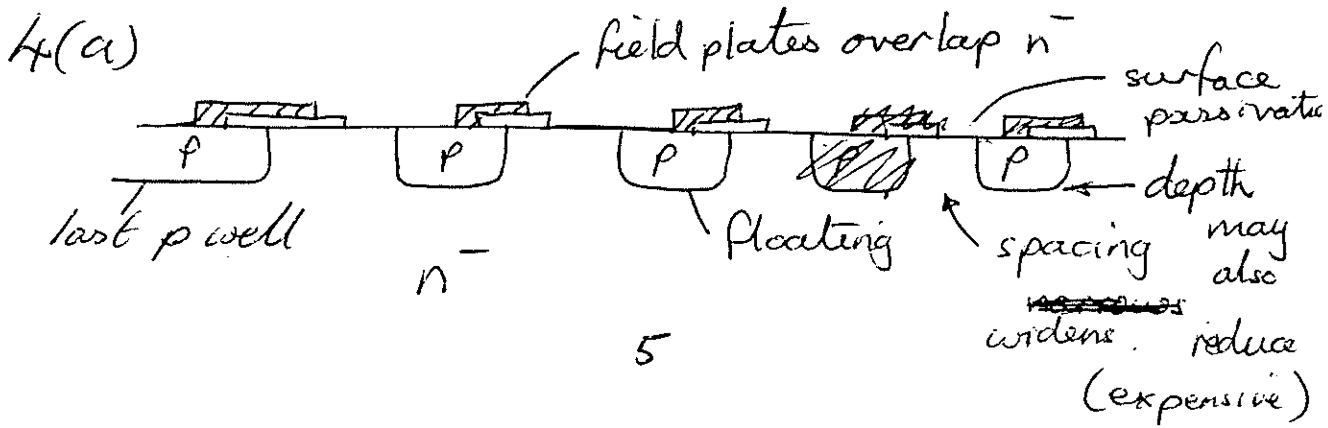
Collect up coefficients.

$$s^2(C_g + C_{gd})C_oR_g + s(g_m C_{gd}R_g + A\beta g_m \cancel{V_g} + C_o) + g_m A\alpha = 0$$

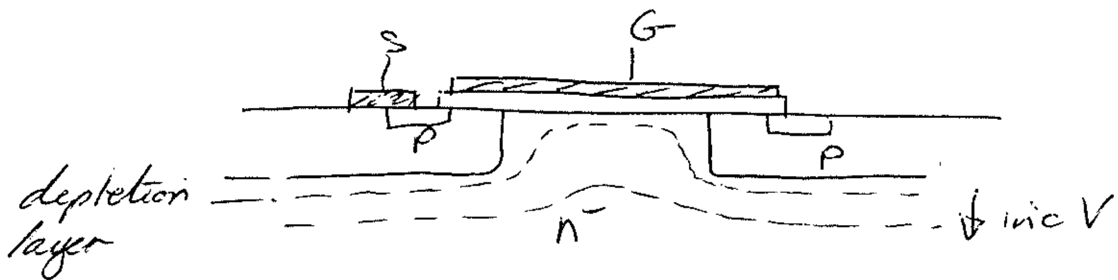
2

So damping is increased by the $\frac{dV}{dt}$ feedback expressed here as "$s\beta$". Note that it is amplified by A, so practically a small feedback capacitor may be used. By adding $s\beta$, a small R_g may be used allowing a very high performance to be obtained. 2

4(a)

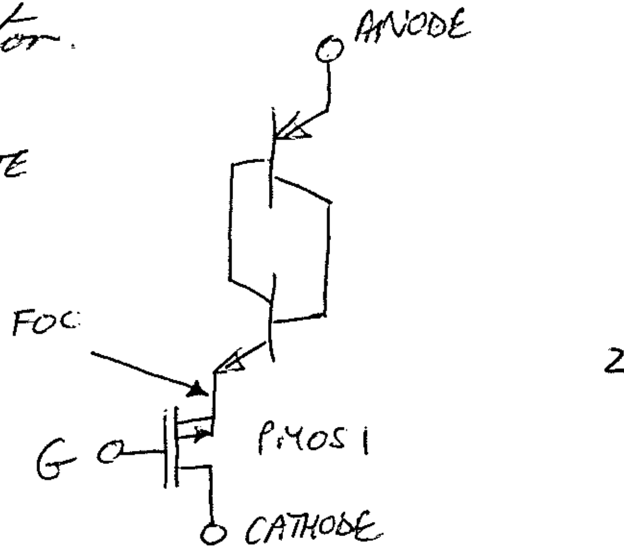


These principles are used in the MOSFET cell structure.

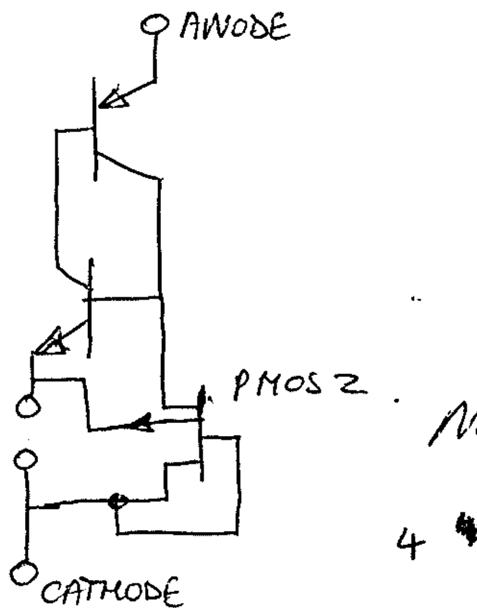


The p-wells are reasonably close so that the e field 'punches through' the n^- between the two cells shown. The gate also acts as a field plate, to curve the depletion layer away from the surface. Finally, a p^+ is often used at the bottom and centre of the well to avoid punch through of the p well. 5

4(b) An Emitter Controlled Thyristor. This version uses a PMOS in series with the main thyristor.



2



Note the body connection.

4

The main drawback is that the p-base is full of charge at the point of turn off of PMOS 1. So hole current flows into the n emitter. Junction J_1 may breakdown before enough current passes through PMOS2

5 points each part, 1 point each sensible new comment.

5/ The applications are chosen to cause some real dilemmas, usually between two main choices.

(a) 100 kHz, 40 kVA. 400V ⇒ 100A. Fast IGBTs.
40V ⇒ 1000A excellent MOSFE

GTOs at these ratings cannot do 100kHz.
IGBTs & MOSFET gate drives are similar, although the IGBTs may need a little more care.
600V IGBTs and 60V MOSFETs are both excellent in terms of losses. IGBT ⇒ 2V @ 100A '200W
MOSFET 0.5V @ 100A × 10 = 500W
0.25V @ 50A × 20 = 250W.
Much depends on the circuit layout and strays. The MOSFETs can be arranged neatly.

(b) Suburban. – say 1MW 1400V ⇒ 700A. For robustness use 3kV devices. MOSFETs may be seriesed but this is not appropriate here, with high currents.
A single GTO may be used. Possibly a single IGBT module, but more likely a pair paralleled.
GTO losses 3V @ 700A ⇒ 2.1kW.
IGBT " ≈ 4V @ 700A ⇒ 2.8kW. still close.

GTO's have complex gate drive requirements, whereas a simple low power gate drive will be sufficient for the IGBTs at say 2kHz. The GTOs are more compact, but suburban is probably easy to air cool. IGBTs are most attractive in new designs

5(c) A power IC needs to contain the whole function in such a cost sensitive application.

Probably runs the motor at a fairly high voltage to keep the wire sizes small, and to fit in with the IC package. Say 30V: Lateral devices are a problem as the device is very poorly cooled in most instances so losses are very important.

The MOSFET and IGBT are very similar in such devices. The channel density is not high as the device is lateral. However the IGBT has a 0·6V penalty with the extra junction.

A GTO cancels out two of the three junction voltages. The current is low so a GTO can be easily driven within the IC. ⇒ GTO losses may be the lowest and the gate drive requirements could be accommodated in the IC in all cases. (may need a negative voltage rail).

5(d) UPS. 100 storey — so better work at a high voltage, say 6·6kV. ie. it needs a transformer. Power? 100kW per floor or less. Say 5MW.
heating!

Out of the range of MOSFETS. IGBT's? 5000A at 1000V. Possible, but lossey. (nice gate drives)

GTO's 2500A at 2000V. (single device possible, Gate drive complexity is mitigated as there is only one device per 'switch'.

Certainly IGBTs could do it, but the lower losses of the GTO is probably nice in a building.