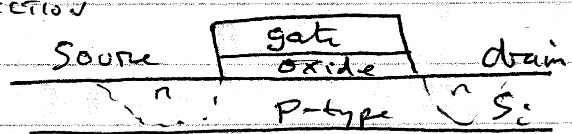
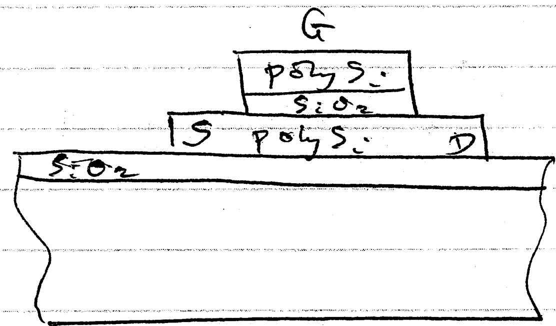
a)(i) Single crystal silicon field effect transistor



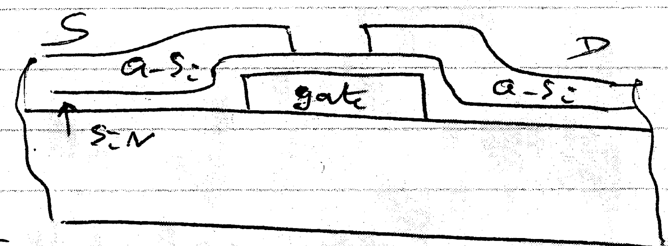
The thermally grown SiO_2 gate insulator has excellent properties. The carrier mobility in the single crystal silicon channel is high. As a result the device performance is good and transistor dimensions can be scaled down as the technology becomes available to obtain further increases in performance. This is the preferred technology for everything except large area.

(ii) polycrystalline silicon thin film FET.



In this case vapour deposited poly Si is used for both the channel and the source and drain regions (n^+ doped). The transistor is built upon an SiO_2 layer which can be deposited on a relatively cheap substrate for driving liquid crystal displays.
Poly Si TFT perform less well than similar dimension bulk MOSFET because of reduced channel mobility, increased gate dielectric thickness and leakage current. But they have the necessary properties for driving the decoding circuits as well as the pixels in LCD display applications.

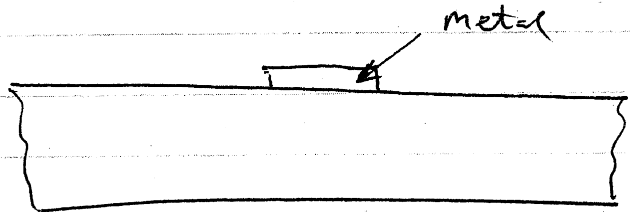
(iii) Amorphous Si thin film transistors are typically constructed by first depositing the gate and building the transistor on top. The carrier mobility is less than that achieved for poly TFT but the fabrication process is relatively low temperature and low cost. Good for displays.



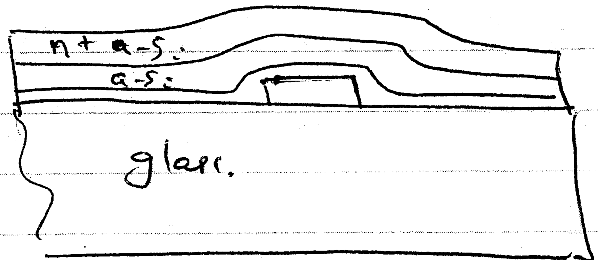
2004 4B6 Q1 continued. 1.2.2004 *

b) Fabrication process for a-Si TFT

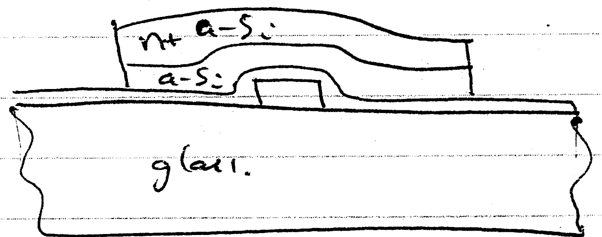
deposit gate electrode metal and pattern gates and drive buses.



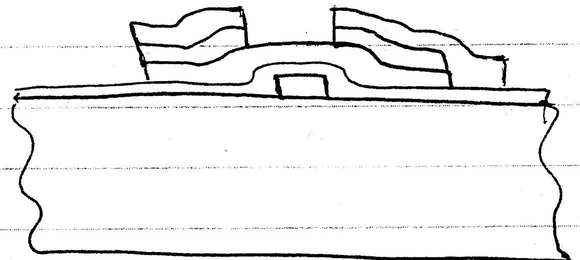
deposit Si_3N_4/a-Si/n^+a-Si in sequence to form the gate material, the channel and the contact metal, respectively



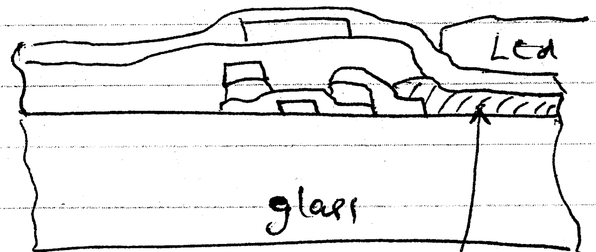
apply photoresist, pattern and etch to form islands for isolated individual transistors.



deposit and pattern the n^+ a-Si source drain contacts and data lines.



pattern the pixel electrode putting a reflective metal light shield above the transistor and deposit a polyimide lcd alignment layer



c) New developments in poly-Si transistors deposited using fewer high temperature processes are leading to a wide range of applications including computer Lcd displays and system on glass technology. A-Si TFT do not offer the high device switching speed but are the lower cost technology at least at present. Poly TFT will be used for smart card, integrated MEMS and an increasingly wide range of applications.

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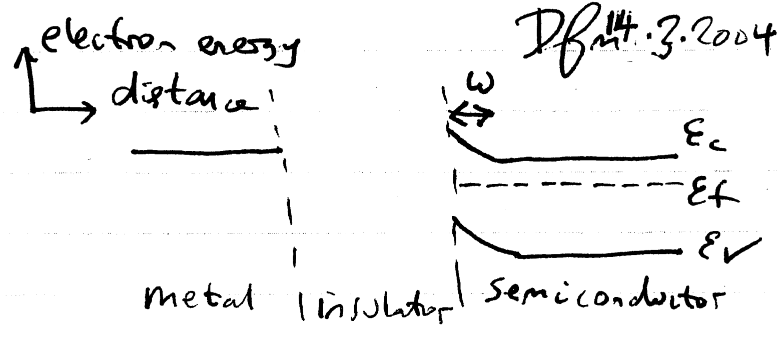
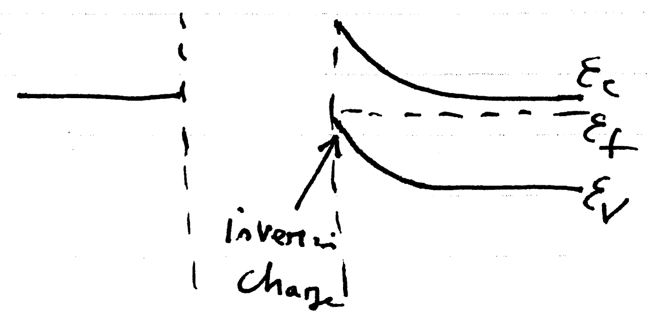
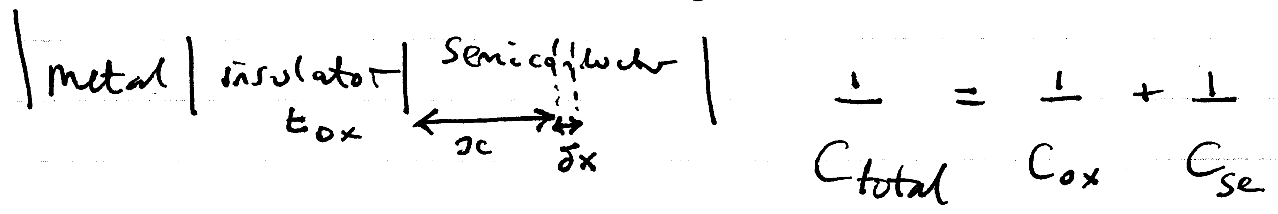


a) When a negative voltage is applied to the metal with respect to the gate then the bands are bent in the semiconductor which is depleted of carriers (conduction band electrons) to a depth W into the semiconductor

Inversion occurs when a larger voltage (d.c.) is applied to the metal and holes are induced at the interface



b) If the semiconductor is depleted to a depth x and the applied voltage is made more negative the depth increases by δx



$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{se}}$$

Per unit area $$\frac{1}{C} = \frac{t_{ox}}{\mathcal{E}_0 \mathcal{E}_{ox}} + \frac{x}{\mathcal{E}_0 \mathcal{E}_{se}}$$

Differentiate with respect to voltage.

$$-\frac{1}{C^2}\frac{dC}{dV} = \frac{1}{\mathcal{E}_0 \mathcal{E}_{se}}\frac{dx}{dV} \quad (1)$$

When the depth increases by δx the charge uncovered is $qN\delta x$
but for a simple capacitor $\delta Q = C\,\delta V$

Hence $C\,\delta V = qN\,\delta x$

$$\therefore \frac{dx}{dV} = \frac{C}{qN}$$

In equation (1) $-\frac{1}{C^2}\frac{dC}{dV} = \frac{1}{\mathcal{E}_0\mathcal{E}_{se}}\frac{C}{qN}$ $\quad \therefore N = \dfrac{-C^3}{\mathcal{E}_0\mathcal{E}_{se}\, q\, \frac{dC}{dV}}$

A small signal is used to obtain the differential quantity $\frac{dC}{dV}$ from the measured C-V curve. [C is capacitance per unit area of MIS]

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2004
4B6 Q2 (continued)

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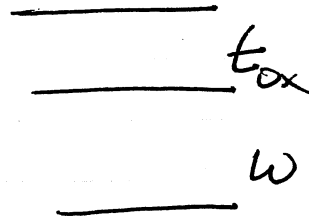
c) $C_{ox} = \frac{A\varepsilon_o\varepsilon_{ox}}{t_{ox}}$



$A\varepsilon_o\varepsilon_{ox} = 2\times10^{-8}\times8.9\times10^{-12}\times5$
$= 89\times10^{-20}$

$C_{se} = \frac{A\varepsilon_o\varepsilon_{se}}{w}$ ②

$A\varepsilon_o\varepsilon_{se} = 2\times10^{-8}\times8.9.10^{-12}\times12$
$= 214\times10^{-20}$

The 40pF measurement at +3V corresponds to oxide only

$\therefore t_{ox} = \frac{A\varepsilon_o\varepsilon_{ox}}{C_{ox}} = \frac{89\times10^{-20}}{40\times10^{-12}} = \boxed{2.23\times10^{-9}\ m}$

For the two capacitors in series in the 15 pF measured at -3V

$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{semi}}$ $\therefore \frac{1}{15\times10^{-12}} = \frac{1}{40\times10^{-12}} + \frac{1}{C_{semi}}$

$\frac{1}{C_{semi}} = 4.2\times10^{10}$ $\therefore C_{semi} = 24\times10^{-12}$ F

From equation ② $W = \frac{A\varepsilon_o\varepsilon_{se}}{C_{se}} = \frac{214\times10^{-20}}{24\times10^{-12}}$
$= \boxed{8.9\times10^{-8}\ m}$

In the depleted region $\varepsilon_o\varepsilon_{se}\frac{d^2V}{dx^2} = qN$ Poisson Equation.

$\therefore V = \frac{1}{2}qN\frac{w^2}{\varepsilon_o\varepsilon_{se}}$

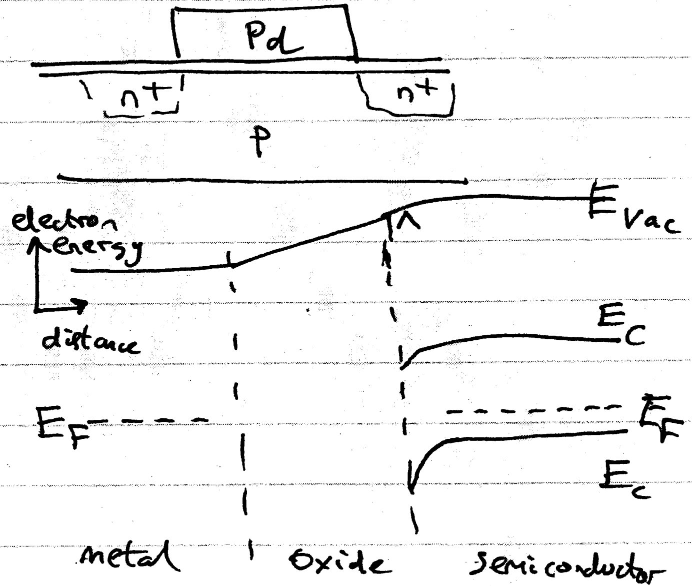
$N = \frac{2\varepsilon_o\varepsilon_{se}V}{qw^2}$

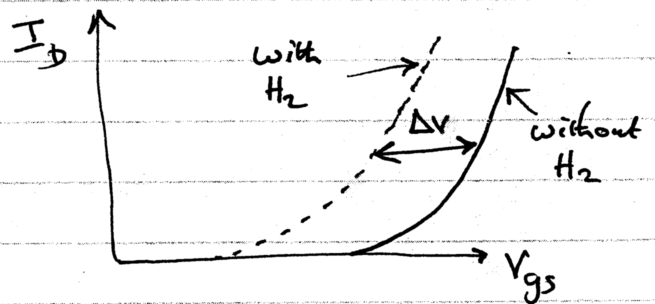
If the band gap of silicon is ~1V take the band bending to be a maximum of ~0.8V

$N = \frac{2\times8.9\times10^{-12}\times12\times0.8}{1.6\times10^{-19}\times(8.9\times10^{-8})^2}$
$\simeq \boxed{1.3\times10^{23}}\ m^{-3}$

2004 4B6 Q3 — ldm 1.2.2004 *

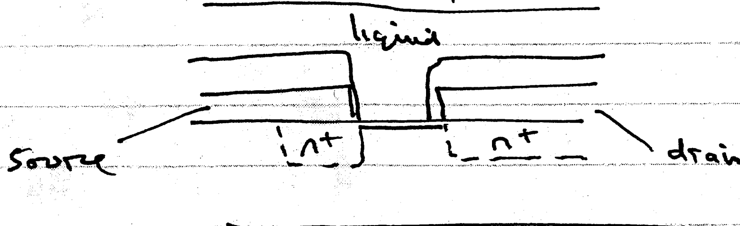
a) A metal oxide semiconductor with a gas permeable gate electrode such as palladium can be used as a gas sensor (Hydrogen in this case). When H_2 diffuses through the Pd the metal work function is changed. This changes the threshold voltage of the MOS transistor and the shift in the $I_D - V_{GS}$ characteristic is the output of the sensor.





b) A biosensor is a bioreceptor immobilized on a compatible transducer.
eg. enzyme FET or ENFET
glucose sensor

Glucose oxidase (GOD) promotes the reaction of glucose with oxygen to form hydrogen peroxide and gluconolactone. gluconolactone hydrolyses with water to form gluconic acid. the FET acts as a pH sensor which detects the gluconic acid.



the pH change in the liquid which forms the gate of the FET results in a threshold change which is detected in the transistor.

2004 4B6 Q3 (continued) DFM 1.2.2004

c) The ISFET in Figure 3 senses and amplifies changes in the double layer potential due to changes in pH in the liquid.
By functionalizing the gate insulator organic or biological compounds of interest can be detected.

I conventional silicon substrate, typically doped p-type
II doped source and drain regions of the transistor (n-type)
III insulator SiO_2 or SiN which has a thin region in the important part of the channel
IV ohmic contact to the silicon source and drain
V insulator to shield the bond wires and contacts from the electrolyte
VI electrolyte which constitutes the gate of the transistor

The critical steps in the fabrication include (i) the formation of the gate insulator and possibly device layers on top of it, and (ii) sealing the other parts of the ISFET for the water based electrolyte

A and C are the source and drain connections.
D is the substrate connection which is typically connected to the source
A is the Pt reference electrode and is usually biased positive to invert the channel under the gate dielectric and turn the transistor on at a suitable operating point

The detection is usually by monitoring the current as a function of time which reflects variations in the threshold (ie pH)

ISFETs are used with a SiN membrane for pH sensing but with other neutral or ion-exchanger membranes for sensing
K^+ Na^+ Li^+
NH_4^+
Ca^{2+} Ba^{2+} Mg^{2+} Zn^{2+}
ClO_4^- $FeCl_4^-$ etc.

2004 4B6 Q4. Nfm 1.2.2004 *

a) (i) The polarization of a ferro-electric material is the alignment of the electric dipoles (which can be accomplished by application of an external field)

surface charge σ

V

P

polarization

Electric Field

hysteretic curve.

(ii) A macroscopic sample of ferroelectric material is typically not uniformly polarized but breaks up into domains of opposite polarization which corresponds to a lower energy state.

The application of a sufficiently strong external field aligns the domains.

A field effect transistor like non volatile memory device can be constructed with a ferro electric material by putting a thin film under the gate electrode.

In the charge approach to readout $\Delta Q = A \Delta P$

In the field " " $E \sim P$

b) In Figure 4

A is an n type doped region in the p type silicon substrate forms the source and drain regions of the access transistor and forms one electrode of the ferro electric storage capacitor

B is a diffusion barrier such as Pt/Ti to avoid the possibility of interaction between the silicon and the ferroelectric

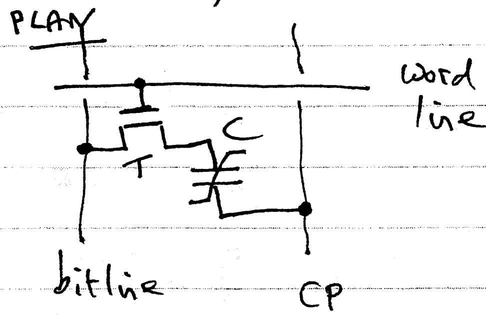
C/ is the ferro electric layer

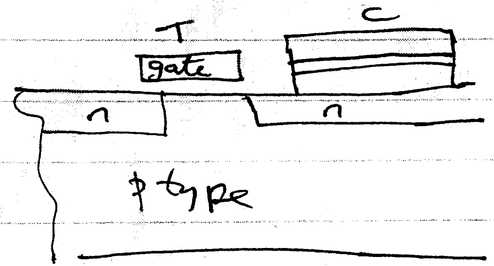
D/ is the top electrode of the capacitor

E/ is an insulator which also provides a hermetic seal.

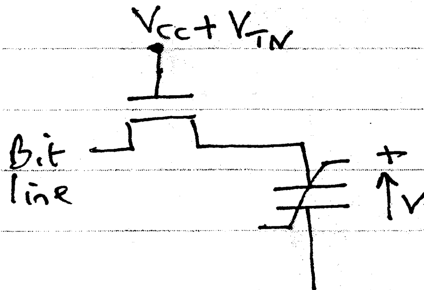
2004 4B6 Q4 (continued) Dfm 1.2.2004

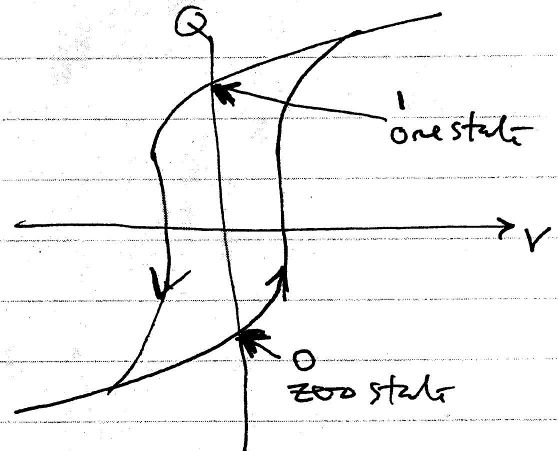
1T/1C ferroelectric cell.





Write operation





Ferroelectric memory is becoming widespread for low power portable applications.

The technology issues include scaling down devices to improve memory density. Stacked capacitor geometries can be used and ferroelectrics with higher polarization are under development.

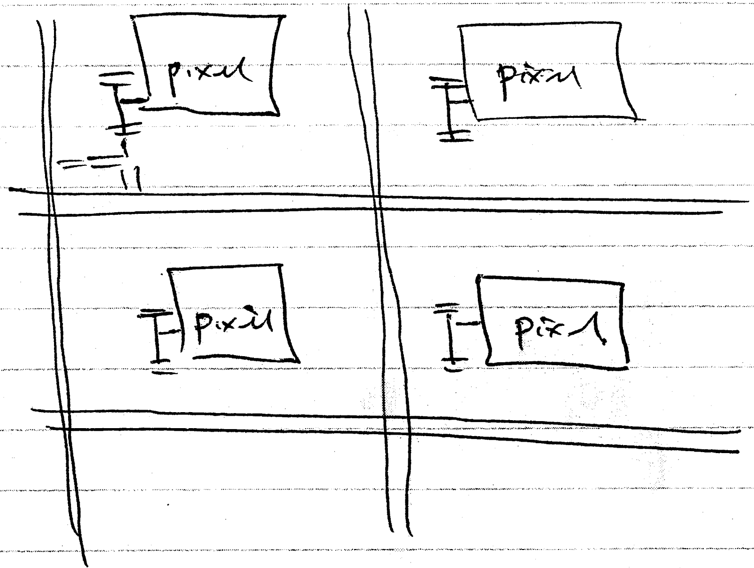
Reliability is an issue because of diffusing hydrogen (even at room temp.) and interface states between the ferroelectric layer and diffusion barrier layers have to be controlled.

Lower voltage operation is desired, which implies the use of thinner ferroelectric layers with the corresponding challenges of maintaining reliability and keeping leakage currents low.

In 2003 ferroelectric memory was available with a stacked geometry and 0.18 μm minimum linewidth technology

2004 4B6 Q5. DBM 1.2.2004 *

a) (i) thin film transistor for liquid crystal display
TFT LCD



the liquid crystal is effectively a capacitor

this is driven by the output of the thin film transistor

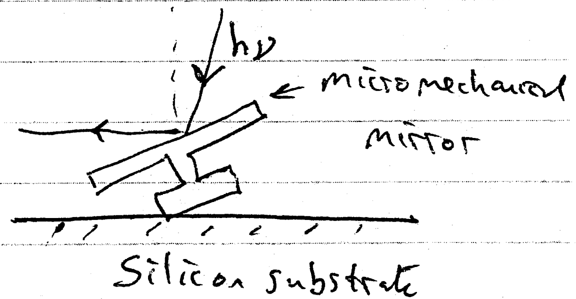
the transistors effectively act as memory elements allowing xy addressing of large displays.

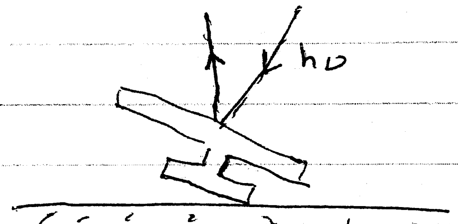
The transistors can be deposited on relatively inexpensive glass substrates. Even though the fabrication process requires a large number of steps the technology is widespread and cost effective because of the large investment in developing production plant technology.

(ii) Digital micromirror displays are made by fabricating tiltable mirrors on silicon substrates with relatively conventional integrated circuits providing the electrostatic voltage necessary to drive the mirrors.

The main application is in bright projection displays and the fast response makes them very suitable for moving images. At present the cost is relatively high, possibly because it is a relatively new technology.

(b) An x-y addressing scheme is used to control the individual mirrors. Tilting the mirror ± 10% from horizontal results in the illuminating light either being reflected along the optic axis and onto the display screen or off the axis.

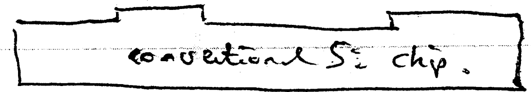


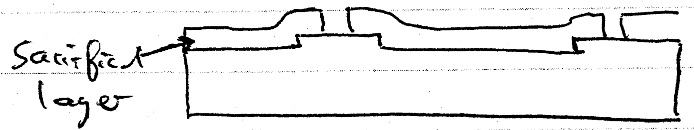


2004 4B6 Q5 (continued) Dfm 1.2.2004 *

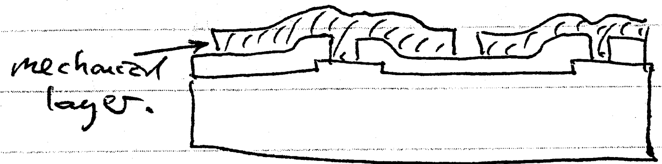
The surface micromachining used to manufacture the micro mirrors involves the deposition of a sacrificial layer which is removed at the later step.

CROSS SECTION



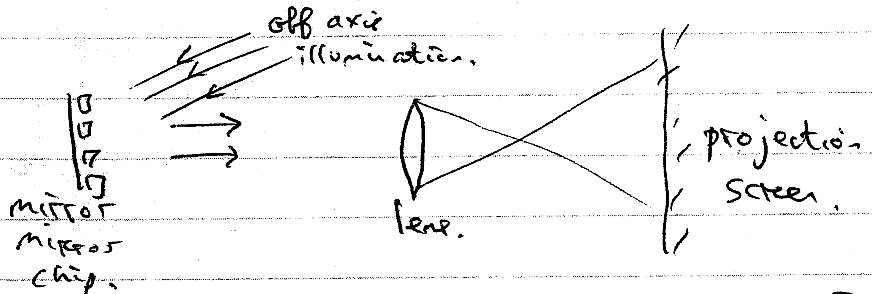


This may be a carbon based polymer which is removed using a plasma in oxygen. The process is a



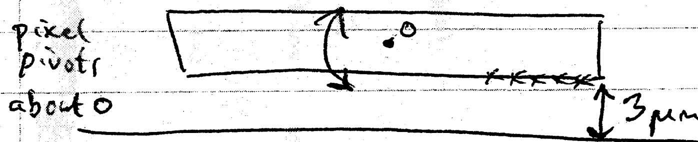
relatively small change from standard IC processing and the yield is high.

OUTLINE SYSTEM



(c) Take the density of the mirror material to be $2000\ \mathrm{kg\,m^{-3}}$

Mass of mirror $16\times10^{-6}\times16\times10^{-6}\times1\times10^{-6}\times2000 = 2\times2.56\times10^{-13}$ kg $\simeq 5\times10^{-13}$ kg



Model the attractor as a capacitor $16\ \mu m \times 4\ \mu m$ area with $3\ \mu m$ gap.

Take the available voltage as 5 V for the electrostatic attractor.

$$\text{Force} = \tfrac{1}{2}QE = \tfrac{1}{2}CV\,\frac{V}{d} = \tfrac{1}{2}C\,\frac{V^2}{d} = \tfrac{1}{2}\,\text{Area}\,\varepsilon_0\,\frac{V^2}{d^2}$$

$$= \tfrac{1}{2}\times16\times10^{-6}\times4\times10^{-6}\times8.9\times10^{-12}\times5\times5\times\frac{1}{3\times10^{-6}\times3\times10^{-6}}$$

$$= 8\times10^{-10}\ \mathrm{N}$$

To make an order of magnitude estimate of the mechanical switching time, calculate the initial (~linear) acceleration and find the time taken to close the $3\ \mu m$ gap.

$$\text{Acceleration} = \frac{\text{force}}{\text{mass}} = \frac{8\times10^{-10}}{5\times10^{-13}} = 1.6\times10^{3}\ \mathrm{m\,s^{-2}}$$

Use $s = \tfrac{1}{2}at^2$ $\therefore$ time $t = \sqrt{\frac{2s}{a}} = \sqrt{\frac{2\times3\times10^{-6}}{1.6\times10^{3}}} = \sqrt{4\times10^{-9}}$

$t \sim 6\times10^{-5}$ secs

This is plenty fast enough for tv rate images and gray scale by time division.