Paper 4B18: Advanced Electronic Devices. Crib Sheet for paper of 2004.

Q1

(a) Multilayer sequence for high electron mobility transistor

1 wafer: GaAs, semi-insulating, 200μm thick
2 GaAs buffer layer, undoped, typically 30-100nm thick as a minimum
3 $In_{0.15}Ga_{0.85}As$ channel layer, narrow gap, strained, low m*, typically 10-50nm thick, undoped, but hosts the 2DEG
4 $In_{0.15}Al_{085}As$ spacer layer, undoped, 10nm thick, wide gap
5 $In_{0.15}Al_{0.85}As$ supply layer, $10^{18}cm^{-3}$ Si doped, 40-100nm thick
6 GaAs cap layer, heavily silicon (n+) doped for ease of ohmic contacts

(b) Processing

1 Optical lithography on wafer to define ohmic contact areas for source and drain
2 Deposit metals for ohmic contacts
3 Etch to remove n+ GaAs cap layer between source and drain
4 Use two-level resist and e-beam lithography for formation of T-gate, about 0.1μm footprint, slightly closer to drain than source
5 Deposit Schottky T-gate
6 Remove resist
7 Alloy ohmic contacts

(c) Show graph of f_T from 1 –100Ghz versus gate length in 0.1 to 10μm (as in lecture notes)

1 Si NMOS scale set by mobility of electrons in Si near Si/SiO2 interface
2 GaAs MESFET scale set by mobility in n+ GaAs (x5 in silicon)
3 AlGaAs HEMT scale set by mobility of 2DEG in pure undoped GaAs (x2 GaAs)
4 InGaAs/InAlAs/GaAs – pseudomorphic HEMT, scale set by lower mass higher mobility in stained InGaAs (x2 over AlGaAs HEMT)
5 $In_{0.48}Ga_{0.52}As/In_{0.47}Al_{0.53}As$/InP unstrained

Q2:

(a)

Attributes:	FET	HBT
Speed	high using litho	high using epitaxy
Power handling	low with 2D channel	high: wide emitter area
Noise	low at low current	higher with hot electrons
Manufacture	effort in litho	effort in epi and processing

(b) Methods of qualification

HBT: substrate GaAs - semi-insulating

Wide gap collector	n++ $10^{19}cm^{-3}$, 10μm
Wide gap subcollector	undoped, 1μm
Narrow gap, thin, base	p++, $10^{20}cm^{-3}$, 100nm
Wide gap emitter	n+ $10^{18}cm^{-3}$, 500nm.

Layer thickness	Manufacturing Line
SIMS +/- 5%	No
Optical: pick up base +/- 10%	Yes
TEM Total GaAs, AlGaAs layers +/- 1nm	No
X-rays – layers +/- 10nm	Yes

Only optical and TEM non-destructive and capable for wafer mapping

Layer Doping

SIMS +/- 20%	No
CV +/- 20%	Yes
Strip and Hall +/- 20%	No

Surface plasmons and IR reflectivity for emitter doping only

(c) Reasons why HBT has overtaken BJT in most applications

(i) Wide gap emitter implies

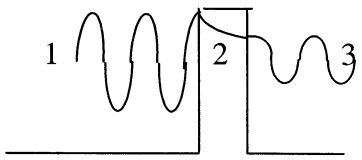
(a) higher doping (x100 to 10E20cm-3) allowed in base without compromising reverse injection of holes into emitter
(b) thinner base makes higher gain possible
(c) still can have lower base resistance with thinner base because of (a)
(d) higher speed from reduced RC time constants as well as short transit time
(e) operation at lower temperature before freeze out and higher temperature before thermionic emission kills device.

(ii) Wide gap collectors

(a) higher reverse bias fields allowed implied higher gain
(b) higher power handling possible.

Q3

(a) Single and Multiple Barrier Tunnelling
Conduction band profile shown.



Incident electron stream (1) exp(ikx), electron with momentum hk in GaAs
h =h/2π

Reflected stream also in (1), exp(-ikx) going to left.

Region (2) AlGaAs barrier layer, thickness a, with potential barrier height

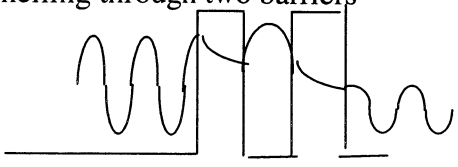
$$V>E=(hk)^2/2m^*$$

Wave attenuates in amplitude as $t=\exp(-\kappa a)$, where $(h\kappa)^2/2m^*= V-E$

Region 3 wave with amplitude t: texp(ikx)

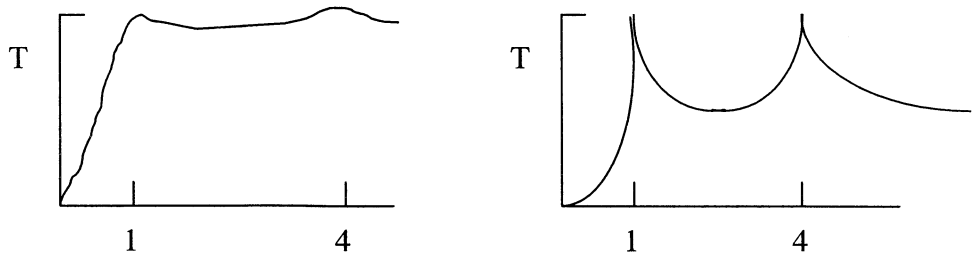
Full actual transmitted signal $T=|t|^2 = 1/[1-4V^2/\{E(V-E)\mathrm{Sinh}(ka)\}]$

Resonant tunnelling through two barriers



More complex pattern as there can be a resonant build up of charge in the well if the incident energy of the electrons matches a bound state in the well if the walls were very thick.

Sketch of transmissions versus energy in units of V= barrier height, for the single barrier and E_0 the bound state energy in the well for the double barrier structure.
$E_0 = (h^2/(2m^*w^2))$ where w is the well width between the two barriers.



(b) Tunnelling device for detection
Single barrier structure with asymmetric doping profile to give asymmetric I-V characterics and the curvature needed for detection. (ASPAT diode of note)

- low noise (no thermionic emission and no hot electrons)
- low T-dependence from tunnelling process
- wide dynamic range
- comparable to Schottky and other diodes in terms of transfer efficiency (i.e. terminal voltage versus Power in)
- ideal for auto radar
- unmanufacturable

Double barrier diode produces negative differential resistance (as in course notes)

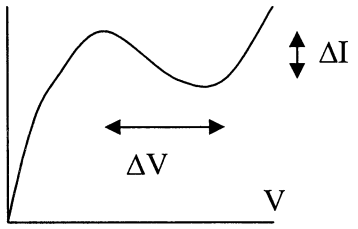
- very high frequency – up to 700Ghz
- high efficiency – 50% at up tom 100Ghz
- low input power – mA by units of 0.1V
- low output power 0.1mW, so limited application

Alternative for source: Esaki diode – forward biased p++/n++ junction.

(c) Manufacturability
Single barrier tunnelling physics: current proportional to exp(-barrier thickness)
+/- one monolayer for 10 monolayer AlAs barrier makes x / 300% in current density for given voltage: this implies need layers uniform to +/- 0.1 monolayers.
Best efforts to date: +/- 0.2 monolayers in lab, +/- one monolayer in production.
For wafer to wafer reproducibility, need absolute thockness control to +/- 0.1 monolayer.

For double barrier diode, the physics is more complex, but still need comparable accuracy for low cost manufacture (uniformity, reproducibility etc).
Tunnelling ideal in theory, but unmanufacturable in practice.

Q4
Negative differential resistance



NDR the regime where for increase of Voltage
there is a decrease in current, i.e. in the ΔV region,
i.e. dI/dV is negative.
Importance: Think of an LRC circuit where with a negative R any noise will be amplified instead of suppressed as exp(t/|R|C).
Bias the device to V_b in the middle of the NDR regime, and a small signal of $v_s\sin(2\pi ft)$ will be amplified until the voltage swing takes us sufficiently far out of the NDR regime in the diagram that the average differential resistance over the whole cycle is zero.
The resulting output power is of order P=(3/16) ΔI ΔV.
This is a broad band response, so the device needs to be put in a resonant circuit of high Q to get a defined output frequency.

Three ways of getting NDR

(i) Resonant tunnelling: diagram of how double barrier diode works (as in notes)

(ii) Intrinsic negative differential conductivity in GaAs at high fields because electrons transfer from low mass long-lifetime central valley states to high mass, low lifetime states in satellite valleys and the current reduces for the same voltage. (as in notes with diagrams)

(iii) IMPATT diode, consisting of a short very p++/n++ junction which is biased into the avalanching regime by the peak forward bias of a microwave signal and the bunch of electrons so created drift and high fields througha transit region in T/2 of the microwave field when they exit the diode just as the voltage is maximum negative.

(iv) Some transistors have an ndr regime at higher biases.

(b) Gunn diode n+ - n- - n+ multilayer in GaAs. GaAs E-K diagram with satellite valleys (as in lecture notes). With a high field applied across the n- region, electrons are heated and transfer into satellite valleys (although there is an effective parallel process of emitting optic phonons which results in device heating and much reduced efficiency).

Diagram in notes of uniform carrier density forming an instability as the slower electrons accumulate transferring electrons and move through the n- region at the saturated drift velocity which is less than the peak velocity of the original central valley electrons. The result is a current spike, and a return to a uniform electron distribution and a repeat of the process. The frequency of this process is determined by the length nof the n- region and in GaAs can range from a few to about 50Ghz, for transit lengths ranging from 20 to 2 microns. At very short lengths the domains have difficulty in forming and the device power drops off. As the output is a series of current pulses, there is much output energy tied up in multiple harmonics, so for example 94Ghz electronics in GaAs is absed on 2nd harmonic operation.

The acceleration process is in efficient, so that a ramped layer of AlGaAs with the Al concentration increasing from 0 to 30% over 50nm will provide an energy ramp followed by a heterojunction energy drop of about 0.3eV, just enough to make the inter-valley transfer much more effective an immune to phonon losses as the electrons are heated up by remaining cold with respect to the local AlGaAs conduction band minimum.
The resulting devioce is improved over the GaAs homojunction device with

- doubled efficiency over the 35-100Ghz range
- reduced temperature dependence (immune to the T-dependence of optical phonon emission, and electrons heated instantaneously to 3000K whether bthey start at 300K or 400K.
- reduced noise as the position of intervalley transfer is not stochastic.

Need to show energy band diagram under no, and under high bias as well.
Typically: 5V, 1I giving 0.1W at 100Ghz.

Q5
Johnson criteria
V_m= maximum voltage over transit length L of semiconductor
f_T is transit time frequency
E_B= dielectric breakdown field (material property)
v_s= saurated drift velocity (material property)
P= output power
Z= impedance of load.

Two Johnson equations: $V_m f_T = (E_B v_s)/2\pi$ and $PZ(f_T)^2 = (E_B v_s)^2/32\pi^2$

E_B for GaN is 3.3 time that of GaAS
v_s for GaN is 1.5 times that of GaAs so $(E_B v_s)_{GaN}/ (E_B v_s)_{GaAs} = 5$
We can drive devices with higher voltages or work at higher frequencies,
We can get much higher power into fixed Z at the same frequency with GaN than GaAs.

Also GaN is a blue light emitter compared with the IR emission of GaAs.

(b) Si and Ge have lattice constants that differ by 5%, and so strain is inherent in multilayers with different alloy compositions.

Extra complication: Si indirect gap with X-type (100) electrons
Ge indirect gap with L-type (111) electrons
Degeneracies at X and L split by strain, so electronic structure is very complex.

If $Si_{1-x}Ge_x$ is grown on Si substrate then the overlayer is strained.
If $Si_{1-x/2}Ge_{x/2}$ is the substrate then both Si and $Si_{1-x}Ge_x$ are strained by in opposite senses.

Exact band alignments depend on strain sequence of the layers.

General results:
ΔE_c is small +ve or –ve, and no good for quantum confinement fo electrons.
ΔE_v can be large enough to confine holes, and so p-type HEMTs are possible.

Strained Si/SiGe layers work well for HBTs, and have applications fro rf circuits (cf from IBM to Analog devices), and now after 15 years, there is some consideration of possible PMOS type device applications.