UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIB

Friday 30 April 2004 9 to 10.30

Module 4B6

SOLID STATE DEVICES

Answer not more than **three** *questions.*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator.

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1 (a) Compare and contrast the performance and characteristics of field effect transistors having a channel made of:

(i) single crystal Si;
(ii) polycrystalline Si;
(iii) amorphous Si. [30%]

(b) Outline a typical fabrication sequence used to produce amorphous Si thin film transistors (TFTs) suitable for driving a liquid crystal display. Identify the steps in the process which are critically important in achieving high yield. [40%]

(c) Discuss the range of applications of polycrystalline silicon TFTs and amorphous silicon TFTs with particular reference to computer displays. [30%]

2 (a) With reference to the metal-insulator-silicon structure shown in Fig. 1 where the semiconductor is n-type, explain what is meant by (i) depletion, and (ii) inversion in the silicon. Illustrate your answer with electron energy vs distance band diagrams. [20%]

(b) Explain how *small-signal* capacitance vs voltage measurements can be used to obtain information about the doping density in the semiconductor. Describe a possible experimental setup. Explain what is meant by *small-signal.* Derive an expression, in terms of easily measurable quantities, for the concentration of ionized impurities as a function of distance into the semiconductor from the insulator interface. [40%]

(c) The results of an experiment on a similar structure to that in Fig. 1 are (i) bias voltage to metal +3 V, capacitance 40 pF, and (ii) bias voltage to metal -3 V, capacitance 15 pF. When the measurement frequency was increased by a factor of ten, there was no change in the measured values of capacitance. If the test device area is 2×10^{-8} m^2, the insulator has a relative permittivity 5, and the semiconductor has a relative permittivity 12, calculate the insulator thickness and the depletion depth into the semiconductor. Assuming that the silicon is uniformly doped, calculate the doping density in the silicon, making reasonable estimates of any unknown quantities [40%]

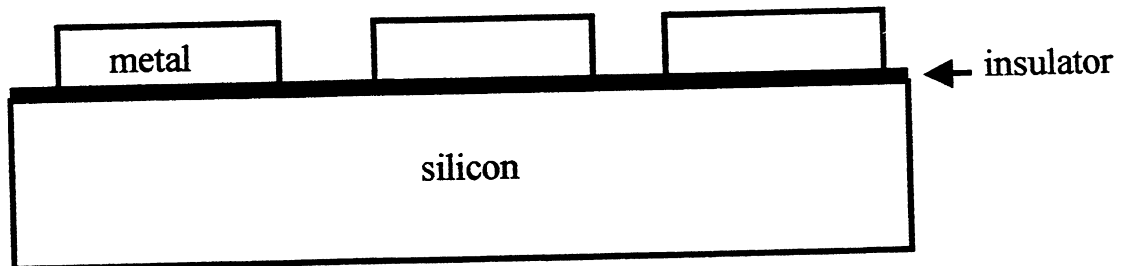

Fig. 1

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3 (a) Explain briefly what is meant by a MOS based chemical sensor, taking a hydrogen ChemFET as an example. Include in your answer a sketch of the energy band diagram. [30%]

(b) Explain briefly what is meant by a biosensor, taking an ion-sensitive field effect transistor (ISFET) as an example. [30%]

(c) Describe the construction of the ISFET shown in cross section in Fig. 2, and identify the electrical functions of the layers I, II, III, IV, V and VI. Explain the critical steps in the device fabrication process. Describe the mode of operation and the functions of the electrical connections to A, B, C and D. Give an example of the successful application of ISFET technology [40%]

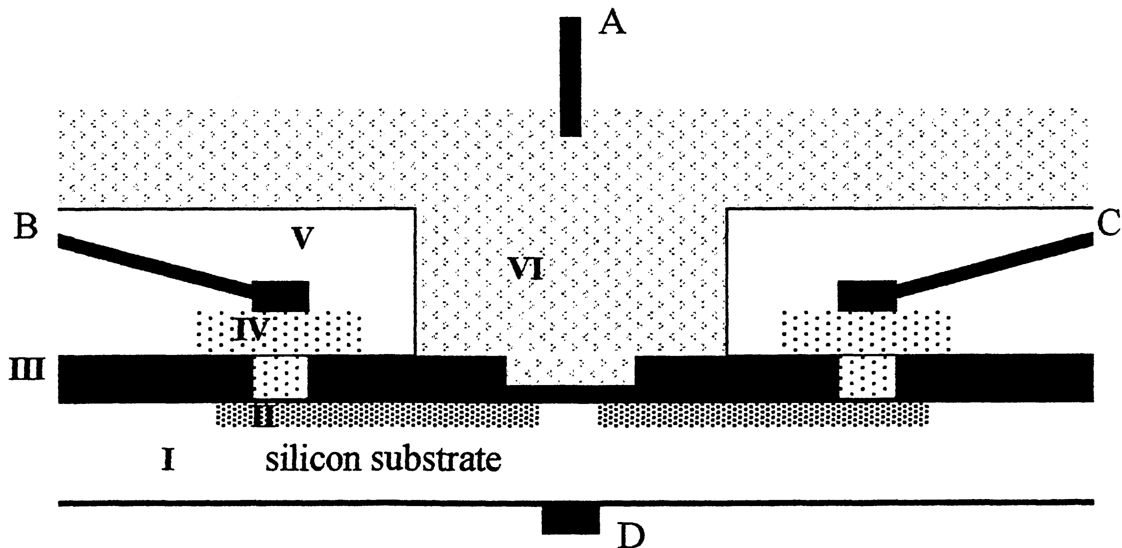

Fig. 2

4 (a) With reference to ferroelectric materials, explain briefly what is meant by (i) polarization, and (ii) domains. How can a ferroelectric material be incorporated into a field effect transistor (FET) type device to make a non-volatile memory cell. [20%]

(b) Explain how a one-transistor one-capacitor (1T/1C) ferroelectric memory cell operates with reference to the partial cross section in Fig. 3. State the function of and the type of material used for the layers A, B, C, D and E in Fig. 3. Draw a circuit diagram showing how a cell can be addressed for a WRITE operation, and include a sketch of the charge vs voltage diagram in your explanation. [50%]

(c) Summarize the performance of current ferroelectric integrated memory devices, and list the main technology challenges which are outstanding. Comment briefly on the performance comparison with competing memory technologies. [30%]

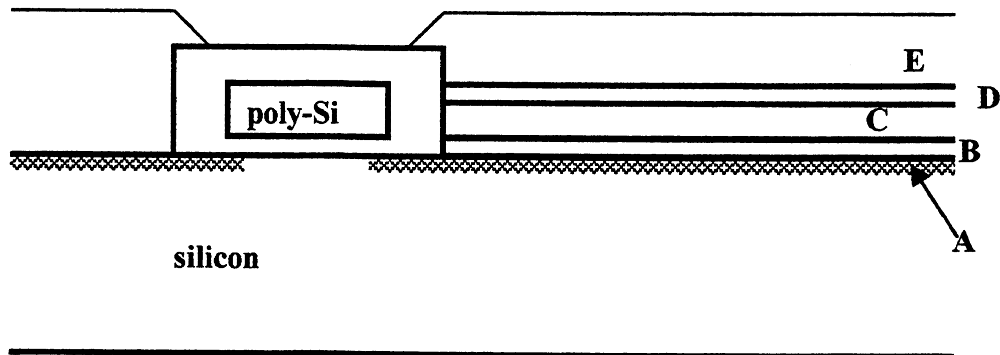

Fig. 3

5 (a) Compare and contrast the technology, performance, cost and range of application of (i) thin film transistor driven liquid crystal displays (LCD), and (ii) digital micromirror displays. [30%]

(b) Describe briefly the construction and mode of operation of an array of micromirrors for display applications. Outline a fabrication process based on a micromachined silicon substrate, including a description of what is meant by surface micromachining. Sketch a typical optical system for a micromirror projection display. Comment on any other possible applications of micromirror array technology. [30%]

(c) Consider an electrostatically driven micromirror display in which each mirror is a torsional element 16 μm x 16 μm x 1 μm. If the electrostatic actuation is across a 3 μm gap, calculate the order of magnitude of the mechanical switching time which is achievable in practice, making reasonable estimates of any unknown quantities. Comment on whether this is fast enough for displaying television images. [40%]

END OF PAPER