UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIB

Monday 3 May 2004 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right hand margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

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1 (a) List the main features of complementary metal-oxide-semiconductor (CMOS) circuit technology and explain why it has displaced other contending technologies for most integrated circuits. [20%]

(b) Describe the function of the CMOS circuit in Fig. 1, where the line D is the power supply V_{dd}, and the line F is the ground V_{ss}. Explain with a sketch which of the four implanted regions are implanted with p-type impurities and which are implanted with n-type impurities. If the circuit is built on an n-type silicon substrate using a p-well where necessary, draw a cross section through the device along the line y=28 from x=0 to x=90. Label all the relevant conductor and insulator layers in the diagram and list their functions. Describe briefly what is meant by self-aligned transistor technology, and explain which lithography step is most important in determining the device switching speed. [30%]

(c) Explain briefly what determines the electrical width of the transistors in Fig. 1. Find the designed ratio of the p-channel transistor width to the n-channel width by taking measurements from the design layout in Fig. 1. In the technology to be used the p-channel mobility is half the n-channel transistor mobility. Calculate the expected ratio of the worst-case rise time to the worst case fall time of the output from the circuit from your measurements on Fig. 1. [20%]

(d) Write out the truth table for the exclusive NOR function between two logic variables. Draw an outline schematic layout for a fully static CMOS circuit to achieve this function. Explain how the relative widths of the transistor channels are designed to achieve equally fast rise and fall times at the output from the exclusive NOR circuit. [30%]

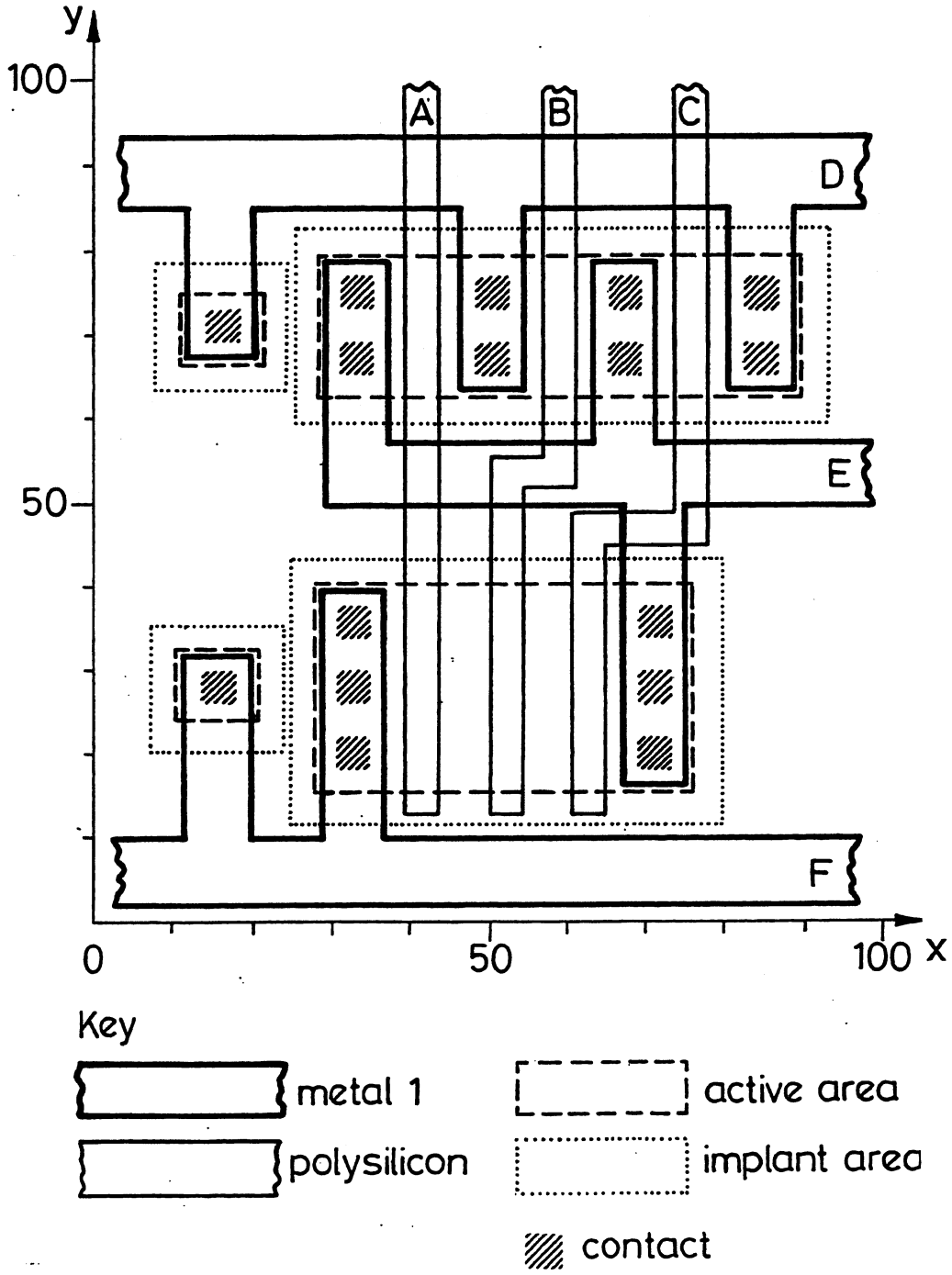
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Figure 1

2. (a) Explain with reference to the data in Fig. 2 what is meant by *device scaling* for silicon integrated circuits. Illustrate your answer with sketch cross sections of devices. Comment on the present state of the technology, making a distinction between the applications in (i) memory devices, and (ii) high-performance microprocessors. What are the approaching physical limits, to what extent can they be avoided, and what is the five year prospect for complementary metal oxide semiconductor (CMOS) technology? [30%]

(b) Describe how ring oscillator circuits are used to measure on-chip performance. Explain what governs the choice of device in the ring, and why an odd number of devices is used. To what extent do ring oscillator data reflect the performance that can be expected from practical circuits? [20%]

(c) Describe the main features of the data in Fig. 3 from a 101 stage ring oscillator. Explain what happens as the power supply voltage V_{dd} is reduced. By graphical means or otherwise, estimate the threshold voltage of the device. [20%]

(d) For one of the devices in the ring, consider a simple device model where the input to the device is a capacitor. The n-channel transistor is 3 μm wide and 100 nm long, and the p-channel transistor is 4 μm wide and 100 nm long. Analysing the data in Fig. 3, taken at $V_{dd} = 0.7$ V when the delay per stage is 55 ps, calculate (i) the effective capacitance of the device, and (ii) the gate oxide thickness, making reasonable estimates of any unknown quantities. State clearly the assumptions made. Comment on whether your result is physically reasonable. [30%]

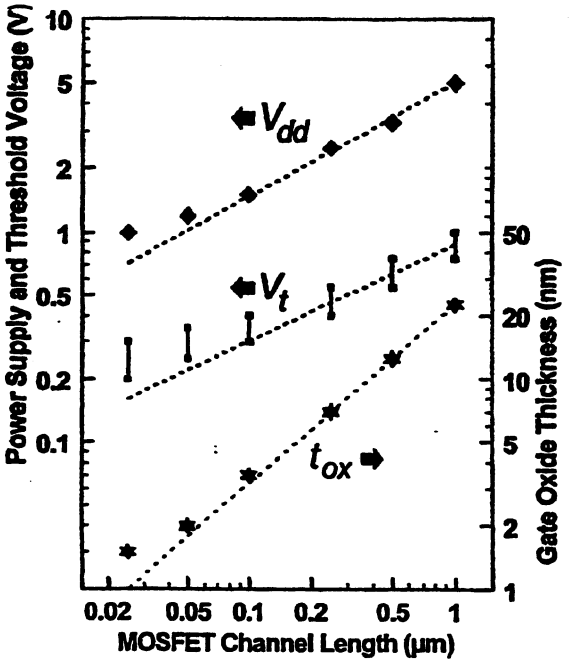

Figure 2

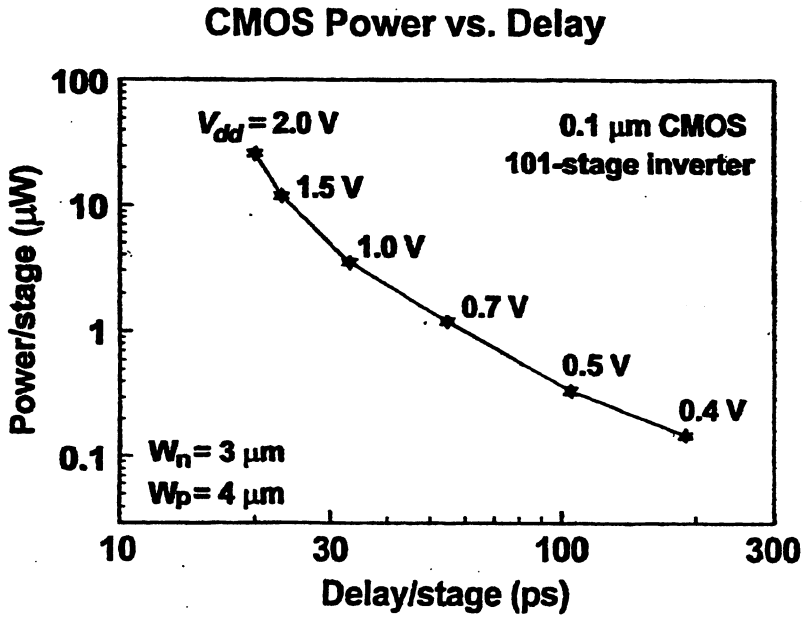

Figure 3

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3 What are the primary requirements of the *output stage* in a linear operational amplifier implemented in CMOS technology, and what challenges does its design pose the IC designer? [15%]

The circuit in Fig. 3 shows a simple Class A amplifier to be used as output stage in a low power integrated operational amplifier. Certain coupling and bias components are not shown. V_{GG} is a fixed bias supply of 3 volts. Fig. 3 also lists device parameters applying to M1 and M2, and the equations for the drain current I_D in a MOS transistor which may be assumed to apply.

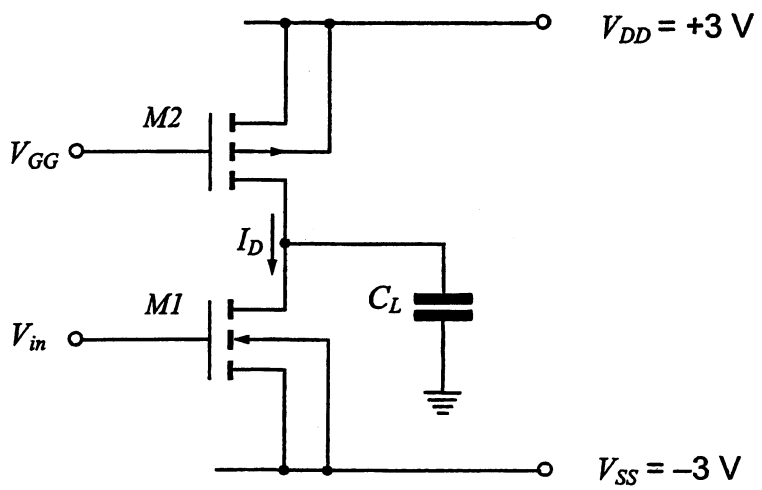
The output stage drives a purely capacitive load C_L of 40 pF, and is required to deliver an output voltage swing of $\pm$ 1 volts relative to ground, with a maximum slew rate of 2×10^7 V s^{-1}. Both devices are to remain in saturation mode under the conditions of operation.

(a) Determine a suitable quiescent operating current I_D for the circuit to meet the slew rate requirement. Hence deduce appropriate channel widths W_1 and W_2, assuming both transistors M1 and M2 have channel lengths of 5 μm,. State any other assumptions made. [20%]

(b) Draw a graph showing the general relationship between the input voltage V_{in} and the output voltage V_{out}, and show the range of conditions over which the saturation requirements are met. [15%]

(c) Estimate the a.c. gain and the small-signal output resistance of the amplifier. [20%]

(d) By consideration of the small-signal equivalent circuit, or otherwise, determine the upper –3dB point for the amplifier under these load conditions. Describe briefly the means available to the IC designer to enhance performance of the amplifier in this and other respects. [30%]



M1: $V_T = +1$ V, $\lambda = 0.01$ V^{-1}, and $\mu_N \varepsilon / t_{OX} = 1.8 \times 10^{-5}$ AV^{-2}

M2: $V_T = -1$ V, $\lambda = 0.02$ V^{-1}, and $\mu_P \varepsilon / t_{OX} = 1 \times 10^{-5}$ AV^{-2}.

$$I_D = \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) (1 + \lambda V_{DS}) \qquad 0 < V_{DS} < V_{GS} - V_T$$

$$I_D = \frac{1}{2} \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \qquad 0 < V_{GS} - V_T < V_{DS}$$

Figure 3

4. (a) Describe the circuit and mode of operation of a transmission gate in complementary MOS technology, and explain clearly how this circuit may provide performance superior to that of a simple pass transistor. [30%]

(b) Give an example of the use of transmission gates in:-

(i) digital circuits

(ii) analogue circuits,

briefly indicating any advantages and disadvantages of the circuit in these applications. [20%]

(c) Describe the circuit structures used in CMOS technology to convey digital signals between input pads and the inputs of logic gates comprising small geometry devices. Discuss the precautions used to protect inputs from the effects of applying excessive voltages and static discharges, and to guard against latchup. [50%]

5 (a) What is the definition of the *threshold voltage* in a MOSFET. What are the major physical and other factors that determine the threshold voltage in a MOSFET? [30%]

(b) The *flash memory* relies for its operation on varying the threshold voltage of a form of MOSFET by electrical means. With the aid of a diagram to show the structure of a flash memory cell, explain how this is accomplished. Hence describe briefly the mode of operation of the flash memory cell, and indicate how data may be written to and read from it. [50%]

What are the main advantages and disadvantages of this approach compared with other MOS implementations of high density memory? [20%]

END OF PAPER