UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIB

Monday 26 April 2004 9 to 10.30

Module 4B8

ELECTRONIC SYSTEM DESIGN

*Answer no more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1 A certain op amp has an open loop dc gain of 120 dB, an output resistance of 150 Ω, and poles in its open-loop frequency at approximately 100 Hz and 200 kHz.

a) Write the equation for the open loop gain. [10%]

b) Sketch a Bode plot of its open loop response. [20%]

c) Describe with the aid of sketches the effect on the frequency response and the step response if the amplifier is operated with feedback so that the overall gain approaches unity. [30%]

d) If the op amp is connected as a non-inverting amplifier with gain 500, for what capacitive load will it be on the verge of instability? [40%]

It is recommended that you answer part (c) graphically, using the log graph paper provided.

2 A Sample-and-Hold circuit is made using the circuit in Fig 1. The following parameters of the Analogue Switch and Op Amp are as follows:

Analogue Switch		Op Amp	
Charge injection	20 pC	Input bias current	50 nA
"on" resistance	40 Ω	Slew rate	8 V/μs
Leakage current	30 nA		

The control line of the analogue switch is connected to a pulse stream. Each pulse has a fixed duration of 10 μs, during which time the switch is closed ("on").

a) Draw a timing diagram of the circuit in Fig 1 and explain hold step and droop rate. [20%]

b) Select a capacitor value so that an input voltage step is acquired to an accuracy of 0.05% or better, the output droop rate is less than 5 mV/ms, and the hold step is less than 1 mV. [50%]

c) What maximum input step is permissible, if slew-rate limiting is not to take place in the op amp? [30%]

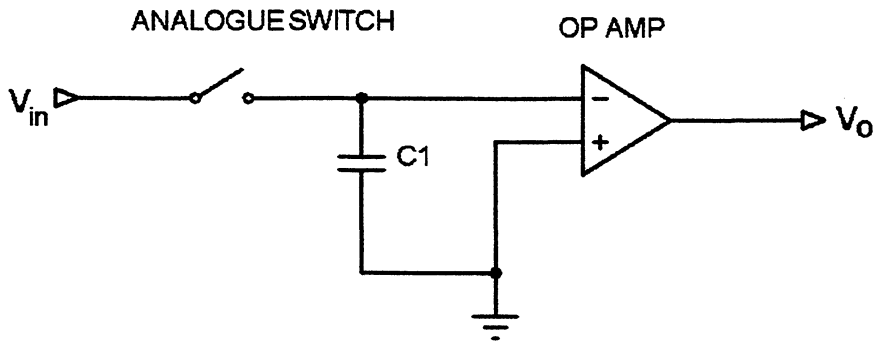

Fig 1

3 a) A filter circuit is to have a *Bandpass* response between the input voltage v_1 and the output voltage v_2 of the form:

$$v_2 / v_1 = A\, s\, \omega_0 / (s^2 + \alpha\, \omega_0\, s + \omega_0^2) \quad \text{where } s = j\,\omega .$$

Sketch the main features of the voltage gain against frequency ω characteristic showing particularly the gain at frequency ω_0 and the half power bandwidth, $\alpha\omega_0$ on your sketch. [15%]

b) The usual inverting multiple feedback filter circuit for a Bandpass response filter is shown in Fig 2 and is known to have a voltage gain given in terms of the conductances of the five passive components, Y_1 to Y_5 as:

$$v_2 / v_1 = -Y_1 Y_3 / \{ Y_5 (Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4 \}.$$

If the passive component connected to the input is a resistor so $Y_1 = 1 / R_1$, what type of components are the other four to get the desired response type?
Hence find expressions for ω_0^2, $A\omega_0$ and $\alpha\omega_0$. [35%]

c) If two equal capacitors of value 100nF are used in the circuit of part (b) determine values for all the components whose conductances are Y_1 to Y_5 if a peak voltage gain of 10 is needed at a frequency of 200Hz and the half power bandwidth is to be 20 Hz.

Describe briefly any precautions needed in selecting the op-amp type suitable for this design. [30%]

d) Explain *one* important use for such a circuit. [20%]

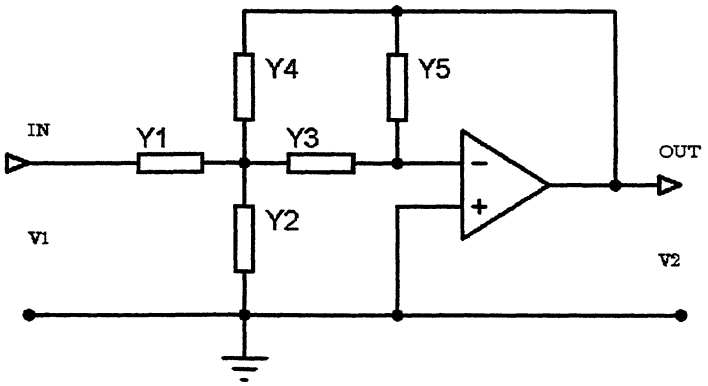

Fig 2

4 a) An instrumentation *full wave* rectifier is wanted which will give a +10V peak output when the input is a sine wave of 1V peak value. The circuit input resistance is to be 50kΩ and errors of no more than 0.1% of the expected peak value should be allowed.

Draw a suitable circuit diagram that uses two op-amps. Explain clearly its action and how errors arise. [40%]

b) Specify the values for the components of your circuit in part(a) as fully as possible including any specification needed on the diode leakage current for the devices used. [30%]

c) The peak output voltage of your instrumentation amplifier is to be maintained on a capacitor with a *droop* of less than 0.1% at a signal frequency of 50Hz. Redraw the circuit. What value capacitor is needed if the output voltage is measured on a *DVM* of 500kΩ input resistance? [30%]

5 a) Define an ideal transmission line. [10%]

b) The coaxial measuring cable from an oscilloscope has a inductance per unit of length L = 267.7 nHm^{-1} and capacitance C = 102.3 pFm^{-1}. Prove that characteristic impedance Z_0 for the coaxial cable is defined as follows:

$Z_0 = (L / C)^{1/2} = 50\ \Omega$

where:
L = inductance per unit of length
C = capacitance per unit of length. [40%]

c) Two terminating resistors R_A and R_B are mounted next to each other on the thick epoxy FR–4 PCB (printed circuit board). The resistor $R_A = 50\ \Omega$ is terminating a signal source with a pulse of amplitude 2.7V and 800 ps rise time. In order to measure mutual inductance of two resistors, the second resistor, $R_B = 50\ \Omega$, is connected to the input of the oscilloscope with a coaxial cable of part (a) terminated by a 50 Ω resistor at the oscilloscope input.

i) Define a mutual inductance. [10%]

ii) If measured voltage amplitude on the resistor R_B is $V_B = 80$ mV at the rising transition of the pulse what is the mutual inductance between the two resistors? [40%]

Note: Assume that signal source is back terminated and that both coaxial cables are orthogonal reducing the direct feed-through.

END OF PAPER