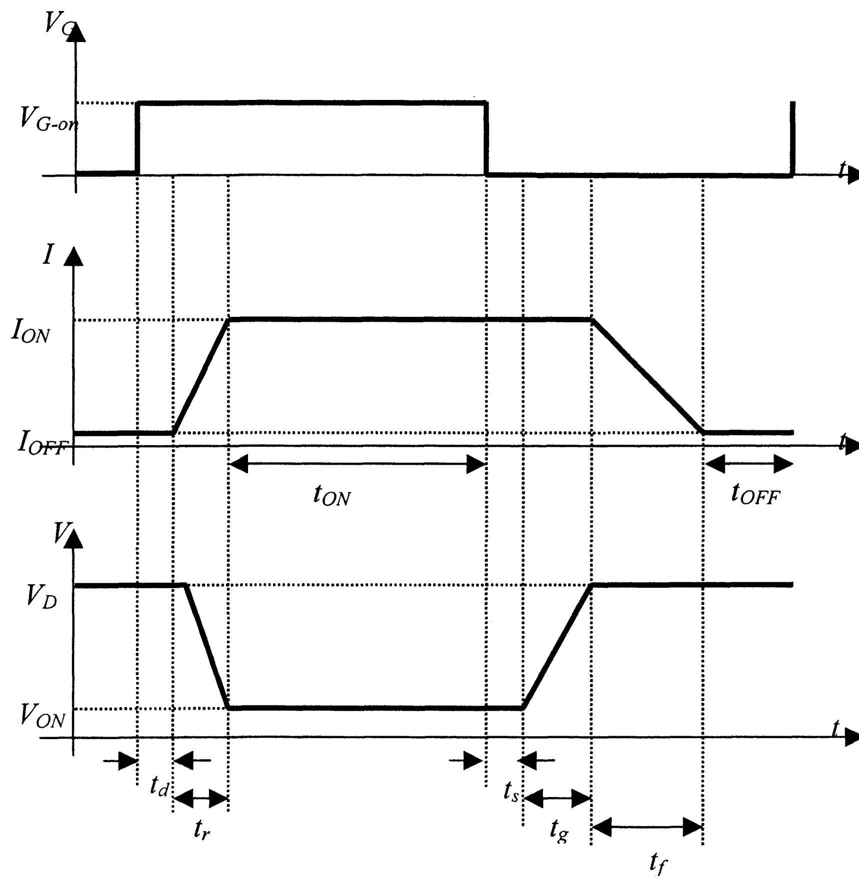
1.

(a) The signal provided by the utility supply is first rectified and filtered to obtain a high DC voltage v_d. The DC voltage is then converted back into an AC form by switching the IGBT ON/OFF at high frequencies. The ac voltage at the secondary is then rectified by the output diodes and a low-pass filter is used to extract its average DC component. A feedback is provided from the output voltage to the gate of the transistors via a controller. This ensures that no matter what the load is, the output voltage remains unchanged. This can be done by finely adjusting the ON to OFF time ratio of the transistor. Initially when the switch is ON, D1 is forward biased and D2 is reverse biased. When the switch is OFF the inductor current i_L circulates through D2. The results is a DC voltage V_0 across the load:

$V_0 = \frac{N_2}{N_1} V_d \frac{t_{on}}{T_S}$ where $\frac{t_{on}}{T_S}$ is the duty cycle D and $\frac{N_2}{N_1}$ is the transformer turns ratio. With the values given Vo = (1/35)·350·0.5 = 5V. [30%]

(b)



(i) $T = \frac{1}{f_s} = \frac{1}{100\,kHz} = 10\mu s$ $\qquad D = 50\% \Rightarrow DT = 5\mu s$

- $DT = t_{ON} + t_d + t_r = 5\mu s \Rightarrow t_{ON} = 5 - 0.2 - 0.1 = 4.7\mu s$
- $(1-D)T = t_{OFF} + t_s + t_g + t_f \Rightarrow t_{OFF} = 5 - 0.1 - 0.3 - 0.6 = 4\mu s$

ON - STATE LOSSES

$$P_{on} = \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON}\,dt = V_{ON} I_{ON} \cdot \frac{t_{ON}}{T} = V_{ON} I_{ON} \cdot t_{ON} \cdot f_s =$$

$$= \frac{4.7}{10} \cdot 1.2 = 0.94\,W$$

OFF - STATE LOSSES

$$P_{off} = \frac{1}{T}\int_0^{t_{OFF}} V_D \cdot I_{OFF} = V_D \cdot I_{OFF} \cdot \frac{t_{OFF}}{T} = \frac{350 \cdot 0.1 \cdot 10^{-3} \cdot 4}{10}$$

$$= 0.014\,W$$

TURN - ON

- delay time : $P_d = \frac{1}{T}\int_0^{t_d} I_{OFF} \cdot V_D = \frac{V_D I_{OFF}\, t_d}{T} = 0.35 \cdot 10^{-3}\,W$ negligible
- rise time : $V(t) = V_D + (V_{ON} - V_D)\frac{t}{t_r}$

$$I(t) = I_{OFF} + \frac{(I_{ON} - I_{OFF})\,t}{t_r} \simeq \frac{I_{ON} \cdot t}{t_r}$$

$$P_r = \frac{1}{T}\int_0^{t_r} I_{ON} \frac{t}{t_r}\left[V_D + (V_{ON} - V_D)\frac{t}{t_r}\right]dt =$$

$$= \frac{t_r I_{ON}}{T}\left[\frac{V_D}{6} + \frac{V_{ON}}{3}\right] = \frac{0.2 \cdot 1}{10}\left[\frac{350}{6} + \frac{2}{3}\right] = 1.18\,W$$

TURN - OFF

- delay time $P = V_{ON} \cdot I_{ON} \cdot \frac{t_s}{T} = 0.02\,W$
- voltage growth time,

$$V(t) = V_{ON} + \frac{V_D - V_{ON}}{t_g} \cdot t \qquad I(t) = I_{ON}$$

$$\Rightarrow P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_D - V_{ON}}{t_g} \cdot t\right) =$$

$$= \frac{t_g}{T} I_{ON}\left[\frac{V_D}{2} + V_{ON}\right] = \frac{1 \cdot 0.3}{10} \cdot 177 = 5.31\,W$$

- current fall time

$$I(t) = I_{ON} - \frac{I_{ON} - I_{OFF}}{t_f} \cdot t \;, \quad V(t) = V_D$$

$$P_f = \frac{1}{T}\int_0^{t_f} I(t) \cdot V(t)\,dt = \frac{t_f}{T} \cdot \frac{V_D \cdot I_{ON}}{2} = \frac{0.6}{10} \cdot \frac{350 \cdot 1}{2} =$$

$$= 10.5\,W$$

ON - STATE LOSSES = 0.94 W

OFF - STATE LOSSES = 0.014 W

TURN-ON LOSSES = $P_d + P_r \simeq P_r = 1.18\,W$

TURN - OFF LOSSES = $P_s + P_f + P_j = 0.02 + 5.31 + 10.5 = 15.83\,W$

TOTAL LOSSES = $0.94 + 0.014 + 1.18 + 15.83 = 17.96\,W$

[50%]

(ii) Transient losses are too high.
It means that frequency of operation is too high. We should lower the frequency so that the transient losses are comparable with the on-state losses.

$$P_{ON} = V_{ON} \cdot I_{ON} \cdot \frac{t_{ON}}{T} = V_{ON} \cdot I_{ON} \cdot \frac{DT - t_d - t_r}{T}$$

$$DT \gg t_d + t_r \Rightarrow \boxed{P_{ON} \simeq V_{ON} \cdot I_{ON} \cdot D}$$

$$P_{turn-off} = \frac{I_{ON} \cdot V_D}{2T} (t_f + t_j)$$

$$P_{turn-on} = \frac{I_{ON} \cdot V_D}{6T} \cdot t_r$$

$$\Rightarrow P_{ON} \simeq P_{turn-on} + P_{turn-off}$$

$$\Rightarrow f_{OPT} \simeq \frac{D \cdot \frac{V_{ON}}{V_D}}{\frac{t_j + t_f}{2} + \frac{t_r}{6}} = 5.95\,kHz$$

$\Rightarrow$ efficient operation around 6 kHz !

[30%]

2.

(a)

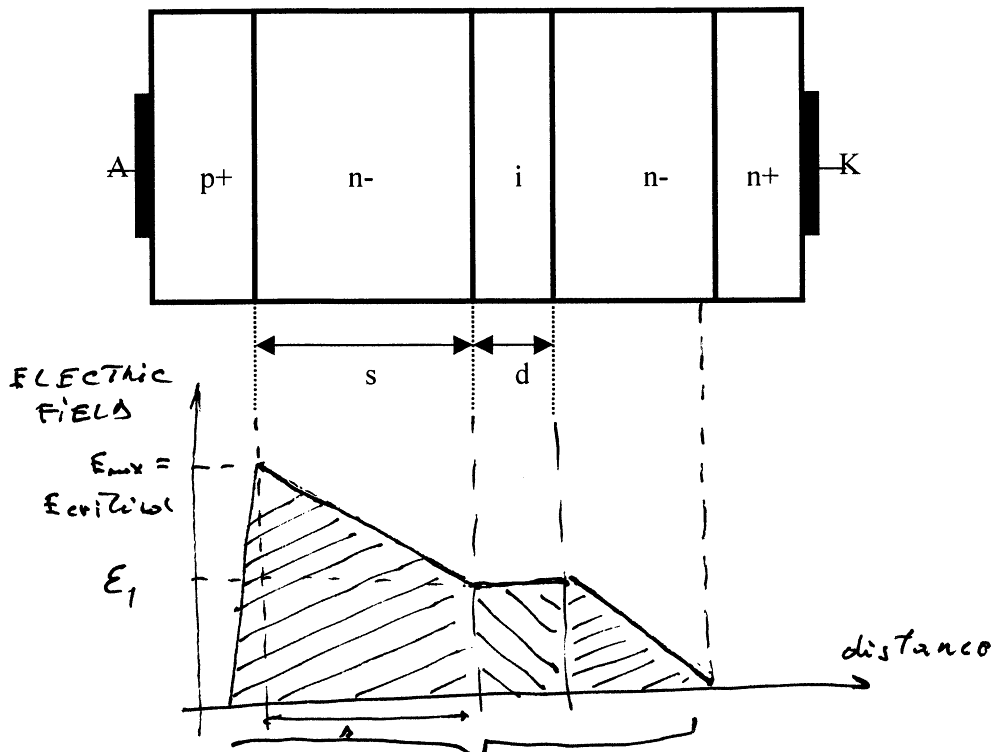
- The NPT high voltage junction is a PIN junction where the thickness (width) of the lowly doped layer (n- or p-) is larger than the depletion region thickness (width) at breakdown. The breakdown voltage of the NPT diode is dictated solely by the doping of the lowly doped region (n- or p-) and the critical electric field but is independent on the thickness (width) of the drift region. The electric field has a triangular shape given by the 1D Poisson equation.

- The PT high voltage junction is a PIN junction where the thickness (width) of the lowly doped layer (n- or p-) is smaller than the depletion region thickness (width) at breakdown. The breakdown voltage of punch-through diode is dependent now on both the doping of the lowly doped layer (drift region) and the thickness (width) of the drift region. The electric field has a trapezoidal shape at breakdown. The doping of the drift layer in the PT junction is significantly smaller than that used in the NPT junction.

- For bipolar devices, the PT design is more favourable because the on-state resistance is dictated by high level plasma and therefore independent of the doping. For unipolar devices the on-state resistance of the drift region is proportional with the width of the drift region and inverse proportional with the doping. However for the same breakdown for PT and NPT the ratio between the doping concentrations of the drift regions in PT and NPT is smaller than the ratio between widths of the drift regions in the PT and NPT design. , Therefore for power MOSFETs the NPT design is more favourable because the on-state resistance is smaller for the same breakdown!

[30%]

(b)

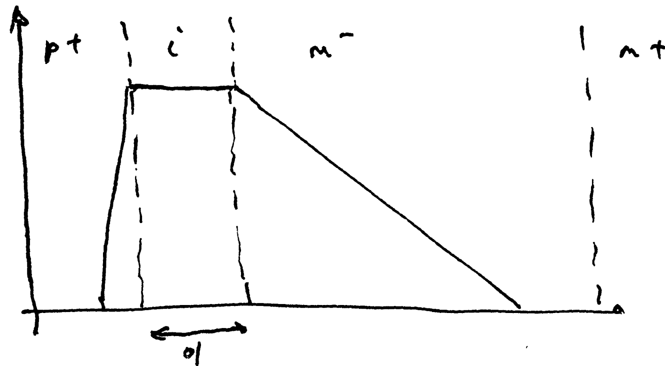


area under the graph is V_{BR}

max of electric field is produced at the p+/n- physical junction

optimum position is when $s = 0$ ⇒ maximum area

⇒ V_{BR} = maximum



[20%]

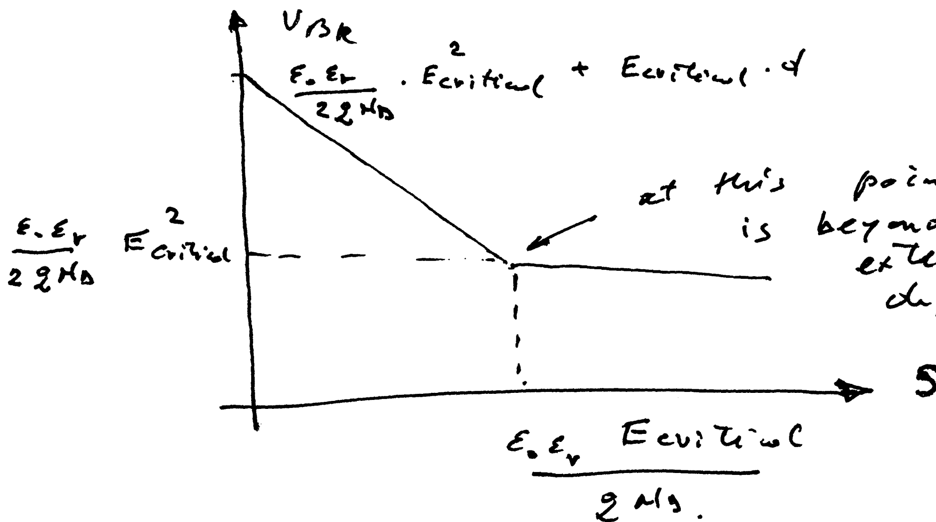
V_{BR} is the area under the graph.

$$V_{BR} = \frac{\varepsilon_0 \varepsilon_r E_{critical}^2}{2 q N_A} + \mathcal{E}_1 \cdot d.$$

$$\mathcal{E}_1 = \mathcal{E}_{critical} - \frac{q N_A}{\varepsilon_0 \varepsilon_r} \cdot s$$

$$\Rightarrow V_{BR} = \frac{\varepsilon_0 \varepsilon_r E_{critical}^2}{2 q N_A} + E_{critical} \cdot d - \frac{q N_A}{\varepsilon_0 \varepsilon_r} s$$

[30%]

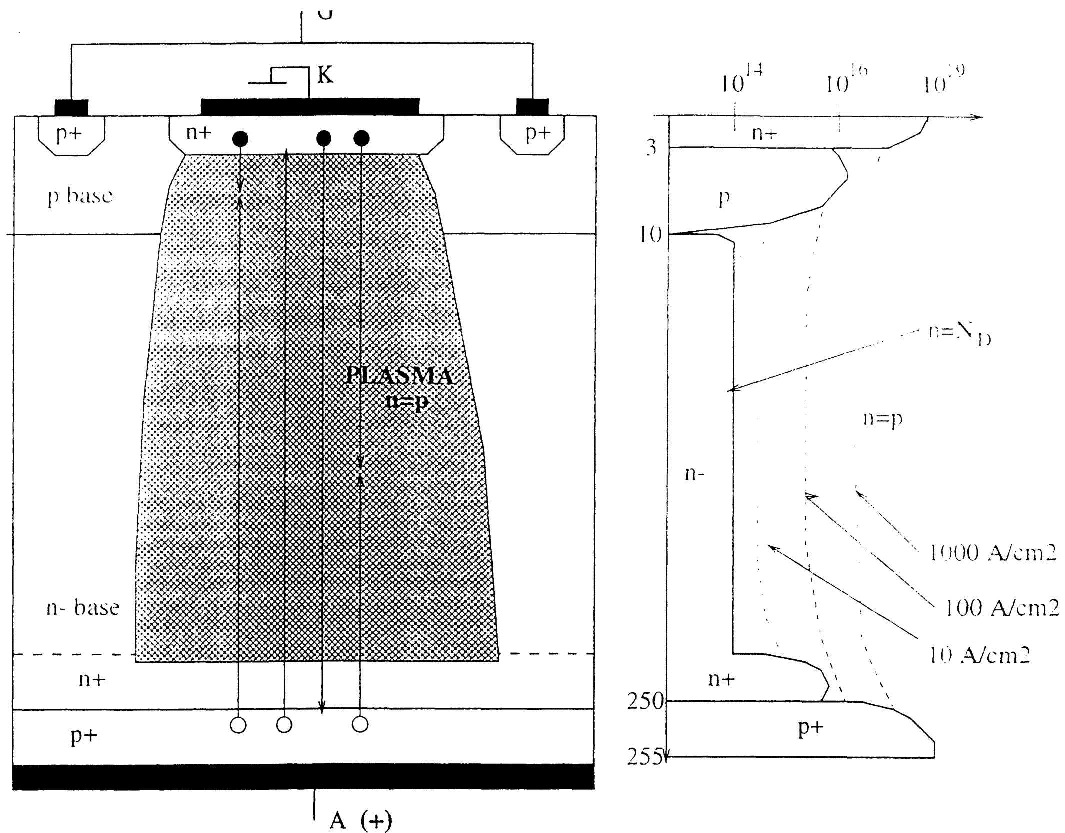


[20%]

3. In the on-state the GTO is under high level injection and plasma is present in the n-base and p- base. The thyristor is self-sustained by the positive feedback established between the two bipolar transistors. There is no gate current flowing in this state. All the junctions are forward biased and the two bipolar transistors (npn and pnp) are both in hard saturation. The thyristor plasma distribution resembles that of a PIN diode with double injection of electrons from the cathode and holes from the anode. The on-state voltage drop across the device is given by:

$$V_{AK(on)} \approx 0.7 + V_d$$

This is similarly to the diode case. The anode junction voltage drop is approximately 0.7 V while V_D depends on the breakdown voltage capability (thickness of the n-base) and the plasma level which in turn depends on the current level. V_D can be orders of few tenth of a volt to maximum of few volts.



- During the turn-off a significant current made of holes is extracted for a short period of time through the p+ gates. This effectively cuts the positive feedback of the thyristor. First the current through the npn transistor will be lowered (as its base current is reduced) which means that the base current supplied to the pnp transistor is reduced too. The injection of the two transistors is lowered and is not high enough to maintain saturation and the regenerative action leads eventually to full turn-off. The plasma is squeezed to the centre of the cathode cell and a depletion region (formed between the p-base and n- base) advances from the edges towards the centre. [40%]

(b)

- Increasing the p-well doping leads to a reduced latch-up effect. This is because the hole current flows through this region because is collected effectively by the cathode short.
- An enhanced p-well doping increases the threshold voltage and therefore increases the on-state resistance.
- Reducing the p-well reduces the threshold voltage but under a certain level the device becomes affected by noise.
- Reducing the p-well doping can lead to punch-through (in the off-state blocking mode) which in turn results in premature breakdown. This is because at low p-well doping levels, the electric field developed across the p-well/n-drift region junction can reach the cathode junction. [30%]

(c) The latch-up occurs when the cathode junction becomes forward-biased and the npn transistor turns on. Since now both the npn and the pnp transistors are ON, they form a thyristor and the gate control is lost. The current no longer flows through the channel but straight through the cathode junction. To prevent the latch-up several methods can be employed (i) increase the density of shorts (ii) reduce the doping of the p-well. To preserve the threshold voltage, one should increase the doping locally in the proximity of the shorts and not under the channel (use of a p+ sinker). (iii) reduce the length of the n+ emitter and (iv) reduce the operating temperature by employing a more efficient heat sink– the latch-up is more prominent at high temperatures.

The static latch-up occurs when the voltage drop developed by the hole current across the lateral resistance in the p-well becomes 0.6 V. Therefore the static latch-up occurs when $I_{hole} = 0.6/20$ Thus the total latch-up current is given by $I_{latch} = 0.6/(0.3 \cdot 20) = 0.1$ A. This is a very low value for any IGBTs indicating a poor design ! [30%]

4.

SOI technology in high voltage ICs:

Advantages

• vertical isolation is achieved via a buried insulated layer
• medium breakdown voltage (limited by the insulating layer thickness) - 700 V is challenging
• very low interference between adjacent devices
• high speed (for bipolar devices such as LIGBT)
• low area consumption

Drabacks

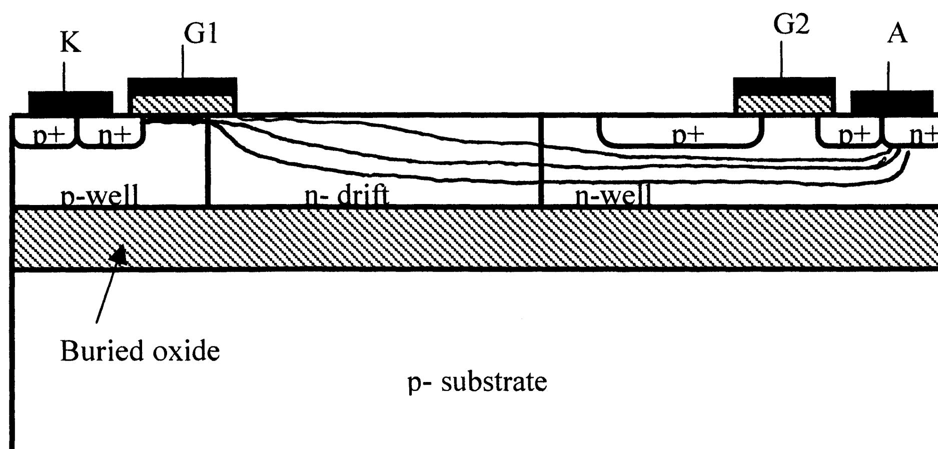
•self-heating
•The Resurf effect is not as effective as in bulk Junction-Isolation technology
•the substrate is relatively expensive

[20%]

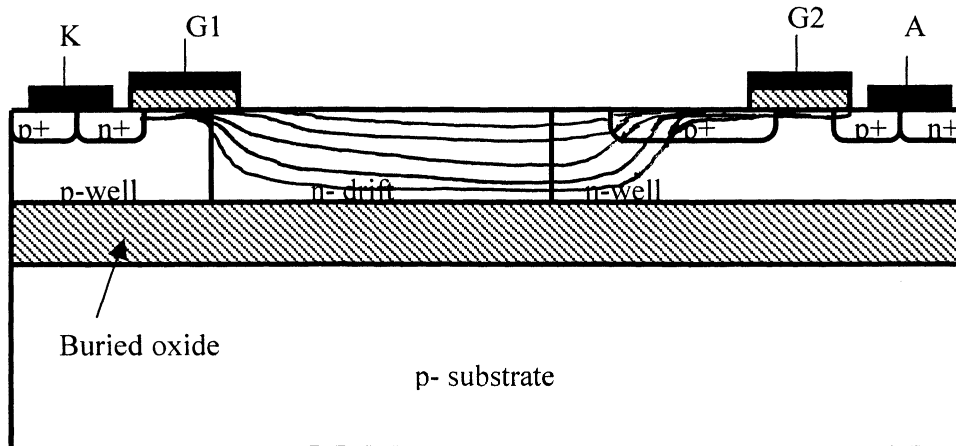
(b)

Off-state. Both gates inactive ($V_{G1-K}=0$ and $V_{G2-A}=0$) The voltage is supported laterally across the n- drift layer and vertically across the buried oxide. The p-well/n-drift layer junction is reverse-biased. There is virtually no potential drop in the silicon substrate, under the buried oxide. The n-well helps to prevent punch-through and thus a PT junction design can be employed.

Turn-on. Both gates are turned on at the same time. ($V_{G1-K}=0 \rightarrow 5V$ and $V_{G2-A}= 0 \rightarrow -5V$). An electron inversion layer is formed in the p-well and a hole inversion layer is formed in the n-well. Initially when the current is small, the device turns on like a MOSFET. The electron current flows through the channel formed in p-well, n-drift layer, n-well to the n+ anode short .



Once a forward voltage drop of 0.6V develops across the long p+ (with the length Lp1) /n-well junction the transistor switches from a MOSFET to a LIGBT. This is followed by plasma injection and thus conductivity modulation of the n- drift region.



On-state: Both MOS gates are active. (V_{G1-K}= 5V and V_{G2-A}= -5V). An electron inversion layer is formed in the p-well and a hole inversion layer is formed in the n-well. The current flows like in anode-shorted LIGBT. Most of the anode current is supplied in the form of holes which travel through the hole inversion layer to the long p+ layer from where they are injected across the junction in the n- base. A small part of the anode current is formed of electrons which flow through the n+ short.

Turn-off : Both gates can be turned off simultaneously(V_{G1-K}= 5V $\rightarrow$ 0V and V_{G2-A}= -5V $\rightarrow$ 0V). The plasma removal is enhanced by the presence of the n+ short on the anode side. Holes are removed to the cathode short and some electrons are removed to the anode short. The rest of plasma is removed by recombination.

Smart operation. It is possible to operate the device in a very efficient way, with minimal power losses, function of the switching frequency. At very high frequencies, the gate2 can be made inactive (no inversion layer formed) and the device operates in a unipolar mode allowing very fast turn-off and low transient losses. At low frequencies the gate G2 can be made fully on, and thus the device operates in a IGBT mode with low on-state losses. At medium frequencies the gate 2 can be operated with a V_{GA} only slightly above the threshold voltage and thus a weak injection is established –this is a good compromise between on-state and switching losses. [50%]

(c) the long p+ is the active emitter of the pnp. To turn the device on from a unipolar mode (MOSFET) to a bipolar mode (IGBT) the long p+/n-well junction must be forward-biased. Thus a long p+ (large Lp1) facilitates the rapid switch from unipolar to bipolar (minimises the snapback effect). However, unless full injection is desirable, the p+ cathode junction should not be forward-biased. This would help the more rapid turn-off. This means that the length of the anode p+ layer (Lp2) should be kept small.
The n-well layer is there to prevent punch-through breakdown and eventually to reduce the anode emitter efficiency (for fast turn-off). The doping of the n-well also determines the threshold voltage of the p-channel transistor. [30%]