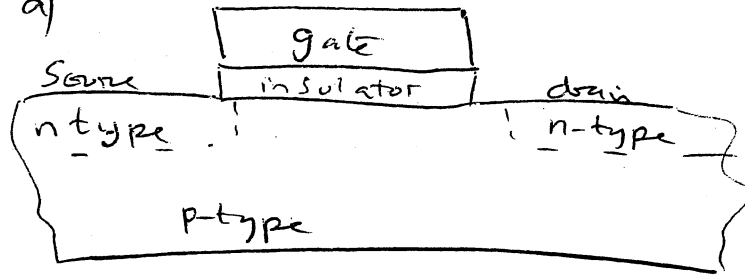


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4B6 Q1 a)

FET
Cross
Section

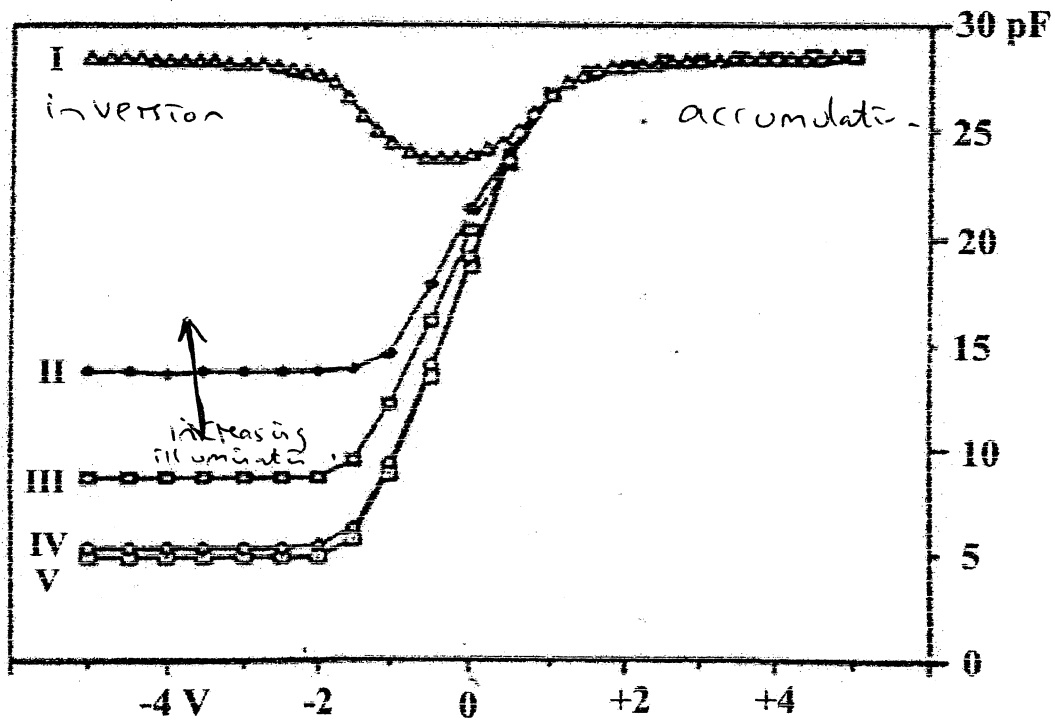


Dfm 13.2.2005

Transistor operation is achieved by applying positive voltage to the gate to invert the channel above threshold and switch on conduction of electrons from the source to the drain

The switch is fast when the source drain separation is made as small as the fabrication technology allows

b) To take the data a small ac signal, eg 0.5 volt peak to peak, is applied on top of a dc signal which is varied from -5 to +5 Volt in this case. The size of the ac determines the minimum voltage range of the C-V structure that can be resolved. In this case small would be ≤ 0.5 Vpp.



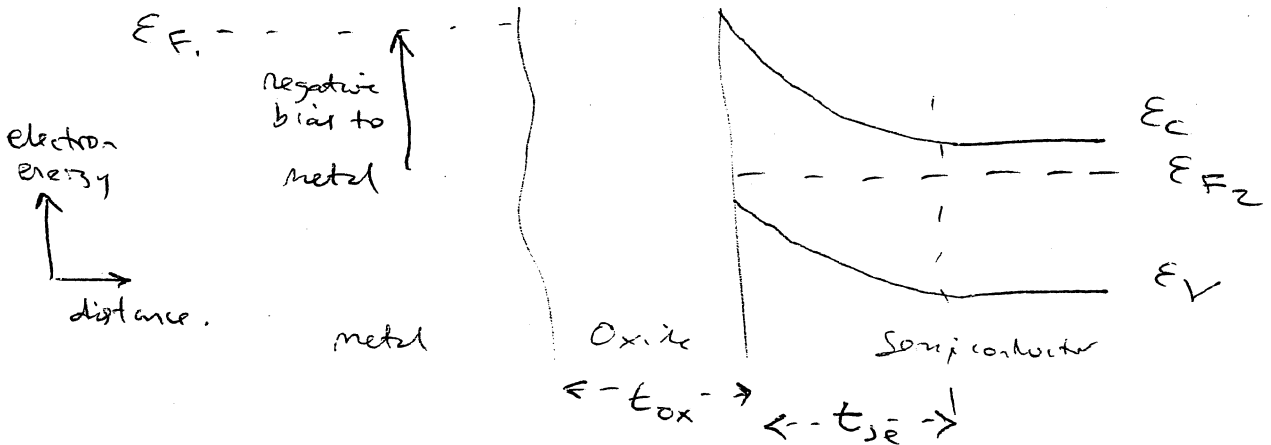
gate with respect to the channel

The semiconductor is n-type because applying a negative gate voltage results in inversion and holes at the surface of the semiconductor.



4B6 Q1 (continual)

DFM 13.2.2005



When the semiconductor is inverted the semiconductor is depleted to a depth t_{se} at the effective capacitor plate separation is $t_{ox} + t_{se}$ for high frequency ac measurements.

However light absorbed in the depletion region produces electron hole pairs which separate in the electric field and produce an inversion charge which stays near to the equilibrium charge at each point in the applied ac cycle.

Hence the capacitor plates are effectively separated by t_{ox} , the capacitance is large under illumination compared with in the dark.

Using a reduced ac frequency in moderate light will also result in an increased capacitance being measured.

c) In accumulation $C_{ox} = \frac{A \epsilon_0 \epsilon_r}{t_{ox}}$

$$t_{oxide} = \frac{A \epsilon_0 \epsilon_r}{C_{ox}} = \frac{2 \times 10^{-8} \times 8.9 \times 10^{-12} \times 5}{28 \times 10^{-12}}$$

$$= \frac{8.9 \times 10^{-19}}{28 \times 10^{-12}} = 3.2 \times 10^{-8} \text{ m}$$

In inversion $\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_{semi}}$

$$\frac{1}{4 \times 10^{-12}} = \frac{1}{28 \times 10^{-12}} + \frac{1}{C_{semi}}$$

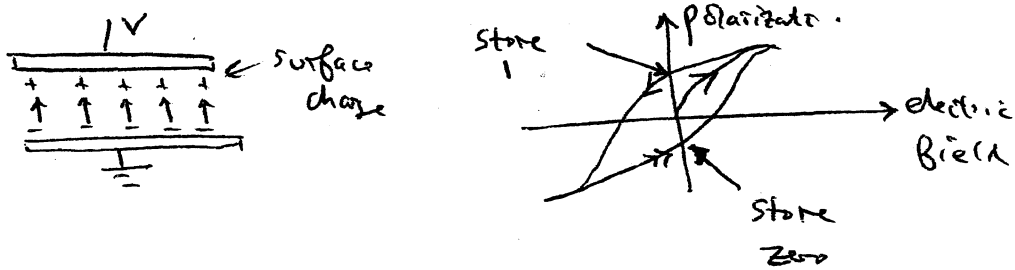
$\therefore C_{semi} = 4.7 \times 10^{-12} \text{ F}$

As above $C_{semi} = \frac{A \epsilon_0 \epsilon_r}{t_{semi}}$

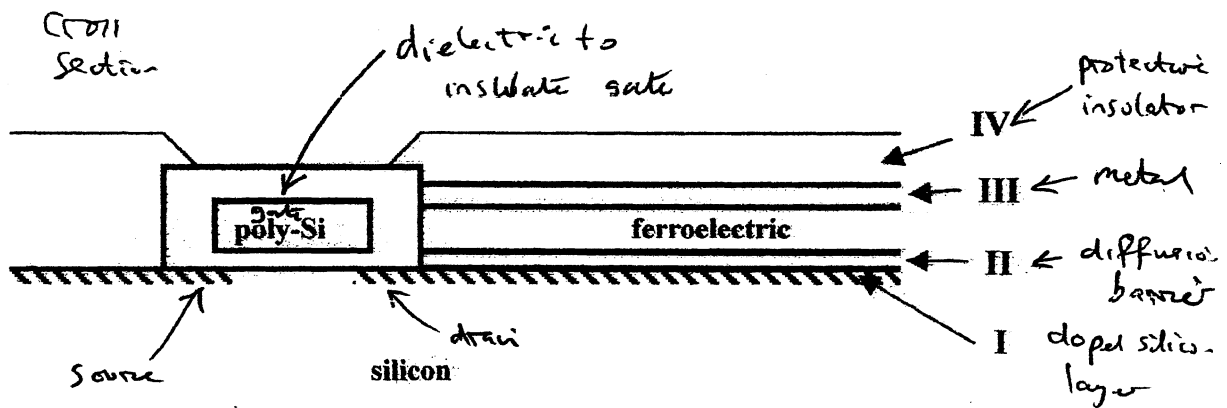
$$t_{semi} = \frac{A \epsilon_0 \epsilon_r}{C_{semi}} = \frac{2 \times 10^{-8} \times 8.9 \times 10^{-12} \times 10}{4.7 \times 10^{-12}} = 1.9 \times 10^{-7} \text{ m}$$

Yell, With short pulse dc measurement the deep depletion region can be probed,

456 Q2 a) The electric dipoles in ferroelectric materials can be aligned to polarize the material by application of an external field. This is the basis of a non-volatile memory device. Dhm 13.2.2005



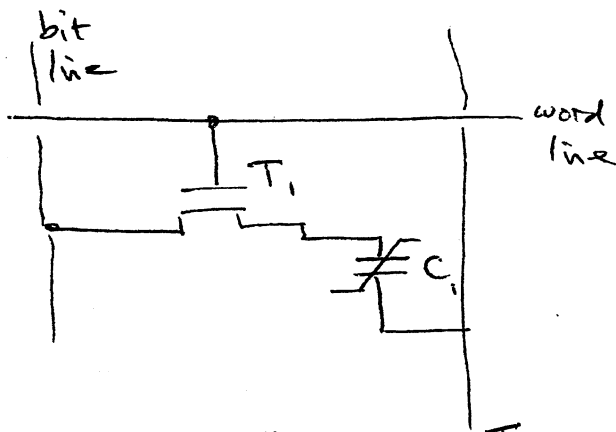
b)



data is stored by applying a high positive or negative voltage

to polarize the ferroelectric.

eg. the word line is high to turn on the transistor T_1 and then a voltage is applied to the bit line to bias the cell C_1



Readout

In the charge approach the cell's address is the charge $\Delta Q = A \Delta P$ corresponding to a change in polarization is detected.

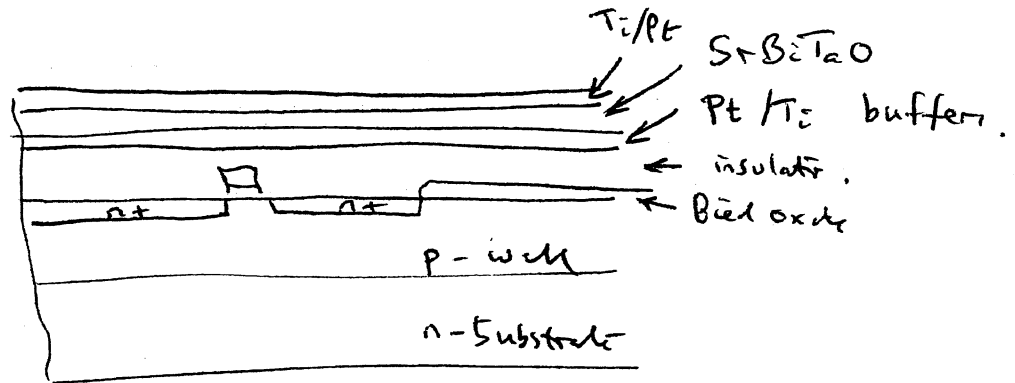
In the field approach $E \propto P$ and the potential on the device is detected.

456 Q2 (continued)

DFM 13.2.2005

The most critical fabrication steps are the deposition of the ferroelectric layer and the diffusion barrier.

eg. cross SECTION



Subsequent steps to etch patterns in the ferroelectric layer and make contacts to the source and drain regions are less critical.

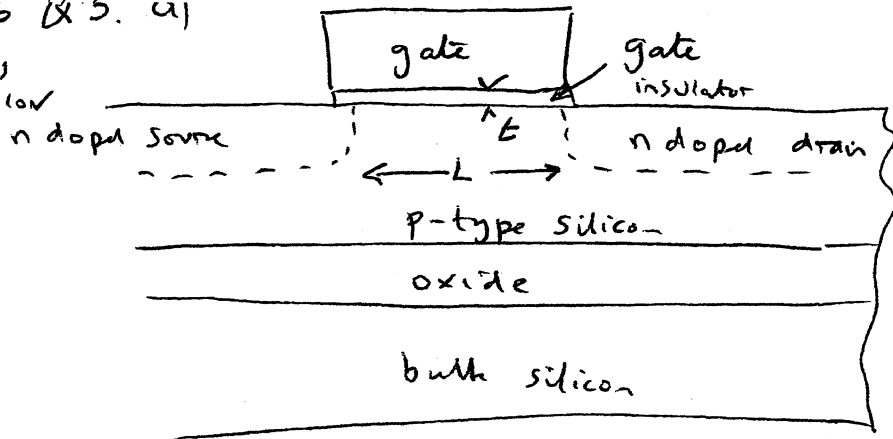
c) Ferroelectric memory is becoming widespread for low power portable applications.

In 2003 ferroelectric memory was available with a stacked geometry at 0.18 μm minimum litho technology.

The prospects are good for further technology improvement for thinner ferroelectric layers to give lower voltage operation.

4B6 & 3. a)

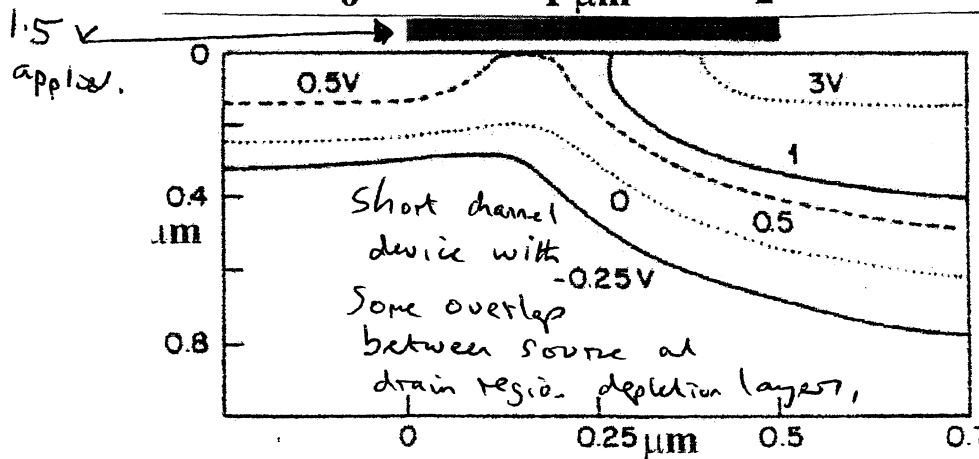
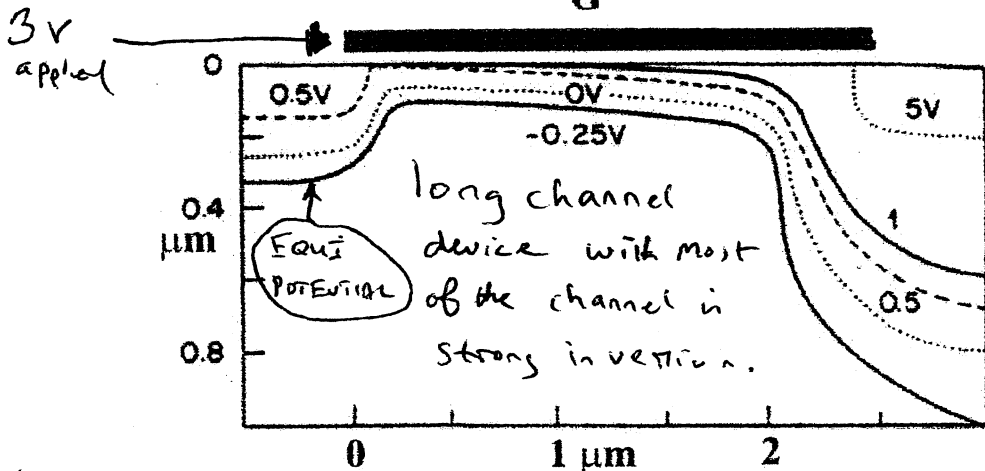
Cross Section



Dfm 13.12.2005

Scaling MOSFET device, taking the example of Silicon on insulator SOI technology consists of reducing L or t as the fabrication technology improves. Reducing the electrical length L gives a faster device because ultimately the transistor performance is determined by the carrier transit time. However the source or drain doping depth or the thickness of the silicon device layer above the oxide must also be reduced to maintain good electrical on/off characteristics.

b)



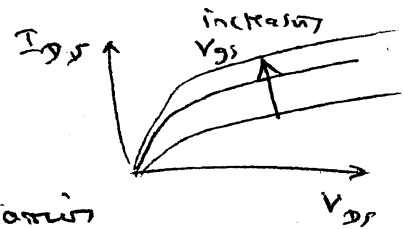
4B6 Q3 (continued)

13.2.2005

In the long channel device at 3V gate there is a clear pinch off region near the drain, across which the transit electrons flow near the gate insulator and are accelerated towards the drain i.e. the device has a well-defined I_{sat} .

The equipotential for the short channel device show that the carriers are no longer confined to the layer near the oxide interface - under these conditions

the current I_{DS} increases with increasing V_{DS} .



The parasitic bipolar effect is that carriers accelerated in the pinch off region produce electron-hole pairs by impact ionization. The carriers separate in the electric field, and there is a hole current towards the source, then the body-source junction becomes forward biased and bipolar transistor action occurs in very short channel length devices, (n-p-n bipolar)

c) One physical limitation to scaling is that tunnelling through very thin gate insulators results in mixing of the controlling fluid (charge to the gate electrode) and the controlled fluid (charge flowing along the channel) degrading the transistor action.

One technology limitation is the lithography requirement to print lines for very short channel length devices (high cost of UV laser systems) and the technology for making very shallow source and drain doped regions.

4B6 Q4 a) A projection display for business presentation must be bright and have good resolution. The speed of the display is less important than for television or video applications.

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Dfm 13.2.2005

LCD.

Liquid crystal based display technologies are widespread, low power and cheap for projection displays but the liquid crystal acts as a light shutter and the proportion of light transmitted is relatively low eg. 50% and the response time for liquid crystal technologies has until recently been long eg 20 msec making high speed video applications difficult.

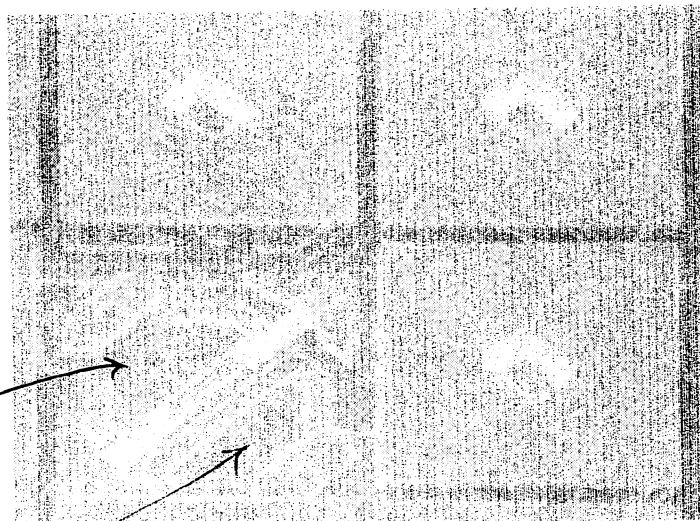
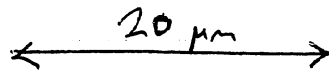
DMD

Digital micromirror displays have been introduced in the past decade for projection displays.

The metallized micromirrors reflect light well ~90% and the displays are bright and efficient compared with LCD technology.

At present the technology is still relatively expensive so market penetration has been limited.

b) In standard mirror display chips the repeat distance is ~20µm



transistor circuitry under the mirrors

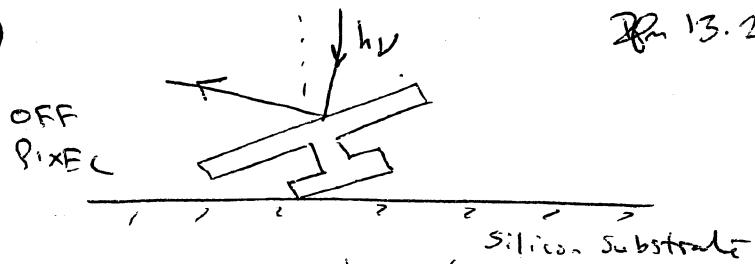
the output provides a voltage on an electrostatic attractor pad used to deflect the mirror

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13.2.2005

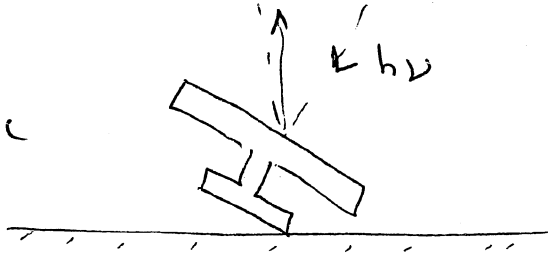
4B6 Q4 (continued)

Cross section of pixel element.



ON PIXEL

Light reflected along the optic axis of the projection system.



An x-y addressing system is used to address and control the individual mirrors which tilt $\pm 10^\circ$ from their mechanical rest position.

The mechanical act. is electrostatic with typically 5 V applied across a $3 \mu\text{m}$ gap.

Mechanical switching times of order 10 μs are achieved since the mirror layer is relatively thin.

eg. Mass of $16 \mu\text{m} \times 16 \mu\text{m} \times 1 \mu\text{m}$ mirror density 2000 kg m^{-3}
 is $16 \times 10^{-6} \times 16 \times 10^{-6} \times 10^{-6} \times 2000 = 5 \times 10^{-13} \text{ kg}$.

eg. Attractor over $16 \mu\text{m} \times 16 \mu\text{m}$ with 5 V across a $3 \mu\text{m}$ gap.

$$\begin{aligned} \text{Force} &= \frac{1}{2} QE = \frac{1}{2} CV \frac{V}{d} = \frac{1}{2} C \frac{V^2}{d} = \frac{1}{2} \epsilon_0 \epsilon_r \frac{V^2}{d^2} \\ &= \frac{1}{2} \times 16 \times 10^{-6} \times 4 \times 10^{-6} \times 8.9 \times 10^{12} \times \frac{5 \times 5}{3 \times 10^{-6} \times 3 \times 10^{-6}} \\ &= 8 \times 10^{-10} \text{ N} \end{aligned}$$

To order of magnitude acceleration: $a = \frac{\text{Force}}{\text{Mass}}$
 $= \frac{8 \times 10^{-10}}{5 \times 10^{-13}} = 1600 \text{ ms}^{-2}$

Approximating to linear motion

$$s = \frac{1}{2} at^2 \quad \therefore t = \sqrt{\frac{2s}{a}} = \sqrt{\frac{2 \times 3 \times 10^{-6}}{1600}} = 6 \times 10^{-5} \text{ sec}$$

The main factors contributing to this fast switching speed are the small mass of the mirror and the small electrode separation.

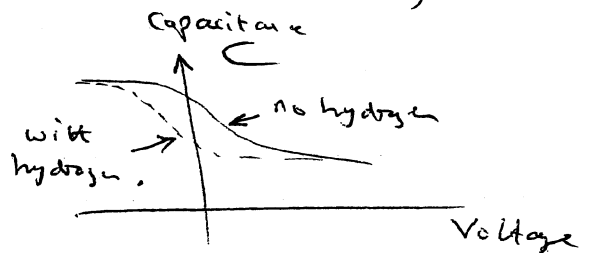
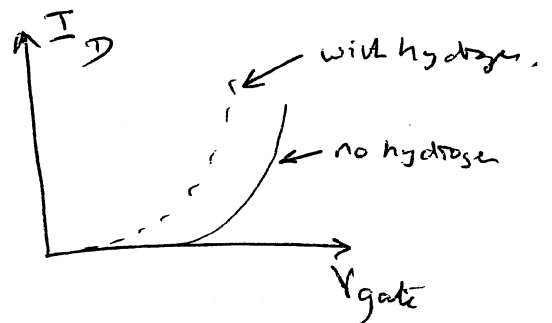
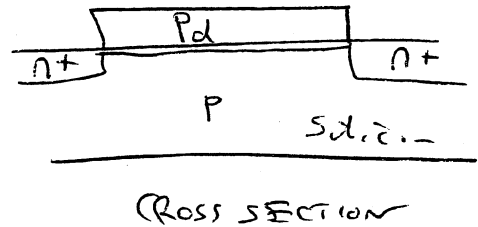
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28/13.2.2005

4B6 Q5 a) A palladium gate

on a metal oxide semiconductor structure is sensitive to hydrogen because it can diffuse into the electrode and change the threshold by changing the metal work function.

Other gases which can be detected using this principle include H_2S , NH_3 , CO etc.

The hydrogen is adsorbed at the interface and generates a +ve charge resulting in the formation of a dipole layer.



b) Hydrogen ion concentration is expressed in terms of pH on a log scale of moles per litre (1 mole is 6×10^{23} ions)

$$pH = -\log_{10} [H^+]$$

$pH \leq 7$ acidic

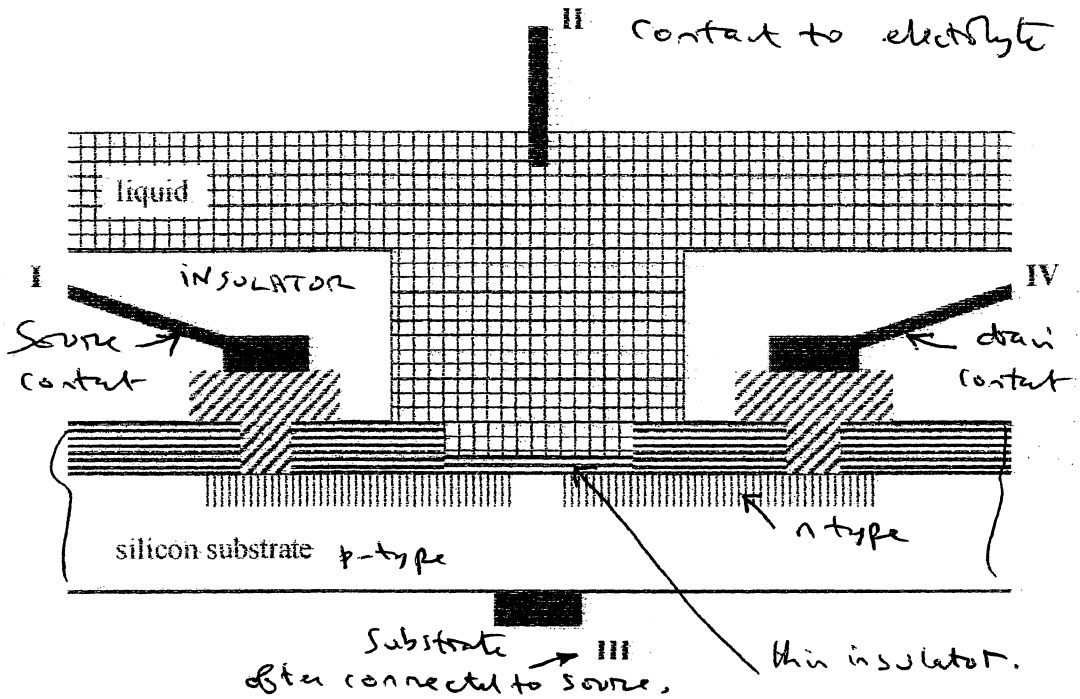
$pH \geq 7$ basic solution

In a biosensor a bioreceptor is immobilized on the surface of a compatible transducer

Eg. glucose oxidase promotes the reaction of glucose with oxygen, one of the byproducts is hydrogen peroxide and gluconic acid is also formed \rightarrow pH change.

4B6 Q5 (continued) ISFET structure

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Dm 13.2.2005



The ISFET serves to sense and amplify changes in the double layer potential due to changes in the pH of the liquid.

By functionalizing the gate insulator surface, organic or biological compounds of interest can be detected.

The detection method is usually to monitor the current as a function of time for a given source drain voltage which reflects variations in the threshold (pH)