4B8 - 2005

Question 1

a) When switch is in position 1, the currents at the inverting input of the integrating amplifier are as follows:

$i_{in} + i_{int} - I_c = 0$

$i_{int} = I_c - i_{in}$

$i_{int} = C_{int} * dV_{int} / dt$

$dV_{int} / dt = i_{int} / C_{int}$

$dV_{int} / dt = (I_c - i_{in}) / C_{int}$

Voltage at the output of the integrator is defined as follows:

$V_{int} = 1/C_{int} * \int (I_c - i_{in}) * dt$

$V_{int} = 1/C_{int} * (I_c - i_{in}) * t \,|_0^{T1}$

At the end of the reset period, T_1, $t = T_1$ and voltage at the output of the integrator V_{int} is defined as follows:

$V_{int} = \Delta V = 1/C_{int} * (I_c - i_{in}) * T_1$

When switch is in position 2, the currents at the amplifier outputs are defined as follows:

$i_{amp} + i_{int} - I_c = 0$

$i_{amp} = I_c - i_{int}$

As amplifier is ideal it is possible to conclude following:

$i_{in} = i_{int}$

$i_{in} = C_{int} * dV_{int} / dt$

$dV_{int} / dt = i_{in} / C_{int}$

$V_{int} = 1/C_{int} * i_{in} * t \,|_0^{T2}$

$V_{int} = 1/C_{int} * i_{in} * T_2$

As integrating capacitor was charged at the start of the period T2 voltage at the output of the amplifier is defined as difference of the charged voltage at the stage T1 and discharge caused by charging integrating capacitor with i_{in}:

$V_i = \Delta V - V_{int}$

When V_i reaches zero, the comparator will change output sign to positive, trigger monostable, which will switch current generator to position T_1 and charge integrating capacitor, repeating cycle.
$V_i = 0$

$\Delta V = V_{int}$

$1/C_{int} * (I_c - i_{in}) * T_1 = 1/C_{int} * i_{in} * T_2$

$(I_c - i_{in}) * T_1 = i_{in} * T_2$

$T_2 = (I_c - i_{in}) * T_1 / i_{in}$

Total period of the cycle is sum of the T_1 and T_2 so it is possible to write:

$T = T_1 + T_2$

$T = T_1 + (I_c - i_{in}) * T_1 / i_{in}$

$T = T_1 + I_c * T_1 / i_{in} - T_1$

$T = I_c * T_1 / i_{in}$

or frequency :
$f_0 = i_{in} / (I_c * T_1)$

Input current to the inverting input of the amplifier is defined as follows:

$i_{in} = V_{in} / R_{in}$

$f_0 = V_{in} / (R_{in} * I_c * T_1)$

b)

i) Assuming that integrating amplifier is not ideal and that at the inverting input amplifier has bias current i_b at the period T1, charging period, sum of the current at the inverting input is defined as follows:

$i_{in} + i_{int} - I_c - i_b = 0$

$i_{int} = I_c + i_b - i_{in}$

$V_{int} = \Delta V = 1/C_{int} * (I_c + i_b - i_{in}) * T_1$

During the period T2 the integrating current through the capacitor is defined with the following equation:

$i_{in} - i_{int} - i_b = 0$

$i_{int} = i_{in} - i_b$

$V_{int} = 1/C_{int} * (i_{in} - i_b) * T_2$

$V_i = \Delta V - V_{int}$

$V_i = 0$

$\Delta V = V_{int}$

$1/C_{int} * (I_c + i_b - i_{in}) * T_1 = 1/C_{int} * (i_{in} - i_b) * T_2$

$T_2 = (I_c + i_b - i_{in}) * T_1 / (i_{in} - i_b)$

$T_2 = I_c * T_1 / (i_{in} - i_b) - T_1$

$T = T_1 + T_2$

$T = T_1 + I_c * T_1 / (i_{in} - i_b) - T_1$

$T = I_c * T_1 / (i_{in} - i_b)$

$f_0 = 1 / T = (i_{in} - i_b) / (I_c * T_1)$

$f_0 = i_{in} / (I_c * T_1) - i_b / (I_c * T_1)$

Error caused by bias current is defined as follows:

$Error_{ibias} = i_b / (I_c * T_1)$

ii) If comparator has fixed offset error, all other components ideal, there is no output error. The threshold level is just moved up or down.

c) Charge of the integrator will occur at the end of the T1 with the maximum voltage defined as:

$\Delta V = 1 / C_{int} * (I_c - i_{in}) * T_1$

If input voltage is equal zero i.e:

$i_{in} = 0$

$\Delta V = 1 / C_{int} * I_c * T_1$

Maximum charge of the integrated capacitor at the end of T1 is 4V

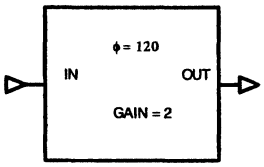
$T_1 = \Delta V * C_{int} / I_c$

$T1 = 4 * 2200 * 10^{-12} * 1 * 10^3 = 8.8 * 10^3 * 10^{-9}$

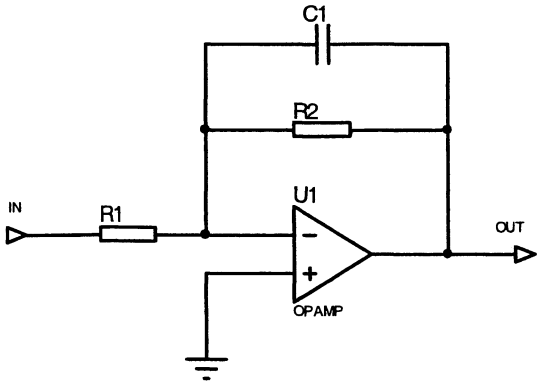
$T_1 = 8.8 * 10^{-6}$ s

Question 2

a) From the given equations for the input and output signals it is possible to conclude that Gain of that circuit should be 2 and phase delay is 120^0.



The possible solution can be, using two resistors, one capacitor and ideal amplifier as follows:



b) In proposed solution relation between Output and Input is defined as follows:

$Out = -(R_2 \parallel C_1) / R_1 * In$

The Gain is defined as follows:

$Out / In = -(R_2 \parallel C_1) / R_1$

Assuming that $j\omega = s$

$Out / In = -[(R_2 / s*C_1) / (R_2 + 1 / s*C_1)] / R_1$

$Out / In = -R_2 / R_1 * \{ 1 / [s*C_1 * (R_2 + 1 / s*C_1)]\}$

$Out / In = -R_2 / R_1 * 1 / (1 + s*C_1*R_2)$

$Gain = G = |-R_2 / R_1 * 1 / (1 + s*C_1*R_2)|$

$G = R_2 / R_1 * 1 / (1 + \omega^2 * C_1^2 * R_2^2)^{1/2}$

$\tan \phi = -\omega * C_1 * R_2$

$R_2 = - \tan \phi / \omega * C_1$

$R_2 = - [\tan\{120) / (2 * \pi * 10^3 * C_1)]$

Select $\mathbf{C_1 = 20\ nF}$

$R_2 = - [\tan\{120) / (2 * \pi * 10^3 * 20 * 10^{-9})]$

$R_2 = -[-1.732 / \{40 * \pi * 10^{-6})]$

$R_2 = 1.732 / \{40 * \pi * 10^{-6})$

$\mathbf{R_2 = 13789\ \Omega}$

$G = R_2 / R_1 * \ 1 / \ (1 + \omega^2 * C_1^2 * R_2^2)^{1/2}$

$G = R_2 / R_1 * \ 1 / \ [1 + (\tan \phi)^2]^{1/2}$

$2 = 13789\ \Omega / R1 * 1 / \ [1 + (-1.732)^2]^{1/2}$

$R1 = 13789\ \Omega / 2 * 1 / \ [1 + (-1.732)^2]^{1/2}$

$R1 = 13789\ \Omega / 2 * 1 / \ [1 + 2.999]^{1/2}$

$R1 = 13789\ \Omega / 2 * 1 / 1.999$

$\mathbf{R1 = 3448.9\ \Omega}$

c) For the frequencies above 1 kHz the gain G defined as:

$\mathbf{G = R_2 / R_1 * \ 1 / \ (1 + \omega^2 * C_1^2 * R_2^2)^{1/2}}$

The gain will be less than 2 as frequency rises and bigger than 2 as frequency is lower. When frequency is equal zero (DC case) the gain G of the circuit is defined as:

$\mathbf{G = R_2 / R_1}$

The phase of the circuit is defined as:

$\mathbf{\tan \phi = -\omega * C_1 * R_2}$

For the frequencies above 1 kHz the phase will be close to 90^0 and at DC case the phase will be zero.

Question 3

a) At a gain of 40, and at 250 Hz, the Gain X Bandwidth product is 10^4. This is a factor of 10 under the limiting figure for the op-Amp. So performance will be close to design figures.

At 250 Hz, for a sine wave of peak amplitude A, differentiating A*sin (ω*t) gives A * ω as the max rate of change of the speed.

With a 15 V supply, A of 12 is the limit approx, when

$A * \omega = 12 * 2 * \pi * 250$

$A * \omega = 1.8840 * 10^4$

which is a factor of **5** under amp limit – so again fine.

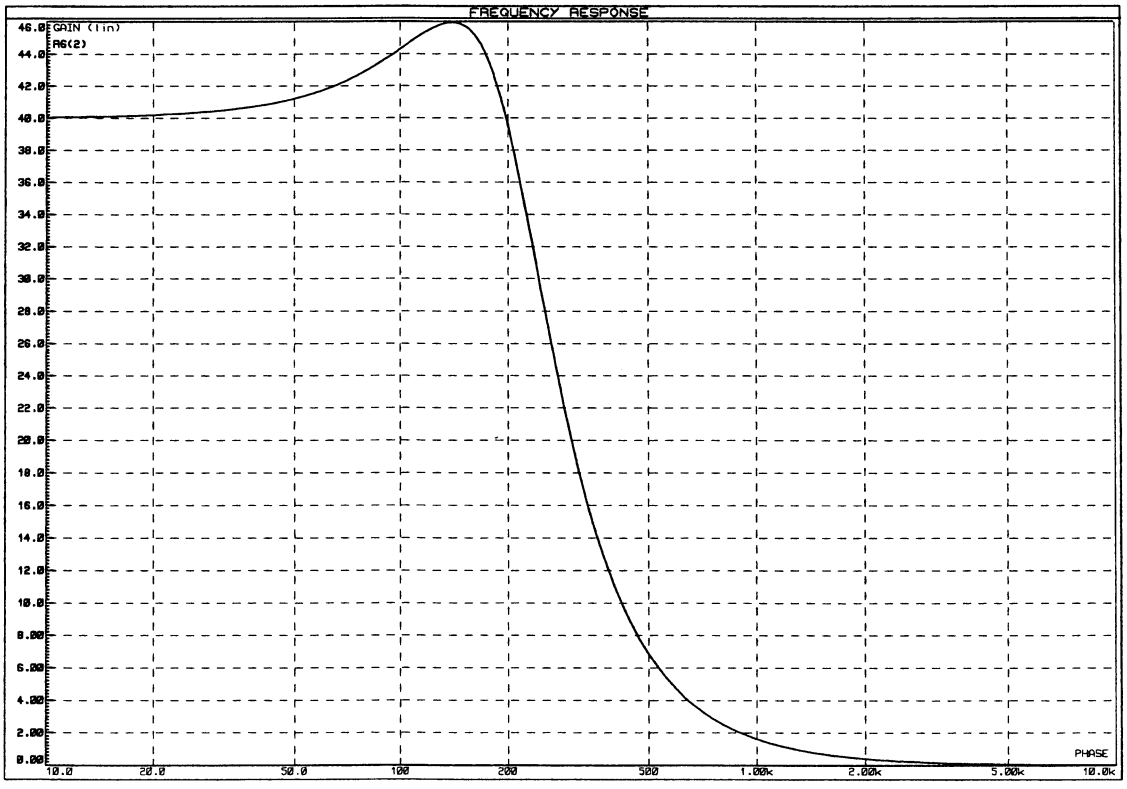
b) Chebichev filter, with 2dB ripple so:

2 dB = $20*\log G_{2dB}$

Gain = $20*\log Gain_{DC}$ +2 dB = $20*\log Gain_{DC}+20*\log G_{2dB} = 20 *\log(Gain_{DC}*G_{2dB})$

Gain max = $Gain_{DC} * Gain_{2dB} = 40 * 10^{2/20} = 40 * 10^{0.1} = 40 * 1.258 = 50.32$

an than drops as shown at 250 Hz.



c) As final stage of circuit is a unity gain inverter, so signal at Output of middle op-amp is $-V_2$.

For middle op-amp, if input voltage is V', say, KCL at (-) input gives:

$V'/R_3 + (-V_2) * s * C = 0$ where $s = j\omega$

$V' = V_2 * s * R_3 * C$ [1]

KCL at input to left hand op-amp gives:

$V_1 / R_1 + V_2 / R_5 + V' / R_2 + V' * s * C = 0$

$V_1 / R_1 = -V_2 / R_5 - V' * (1/ R_2 + s * C)$

Using equation [1]

$V_1 / R_1 = -V_2 / R_5 - V_2 * s * R_3 * C * (1/ R_2 + s * C)$

$V_1 / R_1 = -V_2 * (1 / R_5 + s * C * R_3 / R_2 + s^2 * C^2 * R_3)$

$V_2 / V_1 = \text{Gain} = -1 / (R_1 / R_5 + s * C * R_3 * R_1 / R_2 + s^2 * C^2 * R_1 * R_3)$ [2]

$V_2 / V_1 = \text{Gain} = - [1/ (C^2 * R_1 * R_3)] / [s^2 + 1/(R_2 * C) * s + 1 / (C^2 * R_3 * R_5)]$ [3]

By dividing all terms by $C^2 * R_1 * R_3$ in denominator and comparing this with original function it follows:

$A * \omega^2_0 = 1 / (C^2 * R_1 * R_3)$ [4]

$0.804 * \omega_0 = 1/(R_2 * C)$ [5]

$0.637 * \omega^2_0 = 1 / (C^2 * R_3 * R_5)$ [6]

At very low frequency, the original polynomial nill s and the gain reduces to:

$\text{Gain}_{LF} = A * \omega^2_0 / (0.637 * \omega^2_0)$ [7]

Gain = A / 0.637

Dividing equations [4] and [6] it follows:

$A / 0.637 = (C^2 * R_3 * R_5) / (C^2 * R_1 * R_3)$

$A / 0.637 = R_5 / R_1$ **[8]**

(*gain at low frequency as expected – ratio of feedback resistor/ input resistor*)

Also equation [6] shows R_3 & R_5 define frequency; if R_5 set already by the Gain, than)

R_3 defines frequency.

d) As input resistance of 10 kΩ needed, min, R_1 = 10 kΩ chosen.

For LF Gain of 40, equation [8] gives:

$R_5 = \text{Gain} * R_1 / 0.637$

$R_5 = 40 * 10 * 10^3 / 0.637$

R_5 = 400 kΩ

From equation [5] it follows:

$R_2 = 1 / (0.804 * \omega_0 * C)$

$R_2 = 10^9 / (0.804 * 2 * \pi * 250 * 22)$

$R_2 = 10^9 / 27770.16$

R_2 = 36.009 kΩ

From equation [6] it follows:

$R_3 = 1 / (0.637 * \omega^2_0 * C^2 * R_5)$

$R_3 = 10^{18} / (0.637 * 4 * 3.14^2 * 250^2 * 22^2 * 400 * 10^3)$

$R_3 = 10^{18} / (0.637 * 4 * 9.86 + 625 * 10^2 * 484 * 4 * 10^5)$

$R_3 = 10^{18} / (0.637 * 4 * 9.86 + 625 * 484 * 4 * 10^7)$

R_3 = 3289.56 Ω

If R_4 = 10 kΩ, for a 10 V peak output signal, 1mA of op-amp output is "wasted" – acceptable, they give 20 mA normally. Power dissipation then = 10 mW peak – so OK. (5mW mean)

Question 4

a) Transistors are available as closely matched pairs, in h_{FE} and leakage current and mounted close together so that they track each other in temperature. Diodes are not so made. So the leakage current error of are can hopefully be offset by the other (largely).

The current V_{in} / R_1 from the input is actually the Collector Current, I_C of Q1.
But $I_E = I_C + I_B = I_C + I_C / h_{FE}$ so in equations, we can write $I_E = V_{in} / R_1$ with only 0.33% error when $h_{FE} = 300$ (or more).

R, Q, A use the non-linear diode like, Base-Emitter junction of the transistor so A op-amp output is a logarithmic relation to V_{in} (nearly).

As the transistor leakage current is proportional to temperature, this can be nulled by a second transistor Q_2 fed with a settable constant current I.

The op-AmpA2 will have a high input resistance, so now loading Q_2, and with a non inverting gain of:

$$\text{Gain} = (R_5 + R_6 + R_7) / R_5 = (10^3 + 15 * 10^3 + 0.709 * 10^3) / 10^3 = 16.709$$

b) To get low errors, under 0.5%, the $\exp(V_{BE}/0.026)$ term needs to be 200 (or more) in the "diode" equation:

$$V_{BE} / 0.026 = \ln(200) = 5.3$$

$$V_{BE} = 5.3 * 0.026 = 0.137 \text{ V}$$

So circuit output = -16.709 * 0.137 = -2.29V (for low errors, minimum)

c) To get a circuit input resistance of 3.3 kΩ, min, then $R_1 = 3.3$ kΩ.
Taking the maximum conditions, $I_E = 1$ mA, $I_S = 0.2$ nA it follows:
$\exp(V_{BE} / 0.026) - 1 = I_E / I_S$
$I_E / I_S = 10^{-3} / (2 * 10^{-10}) = 5 * 10^6$
$\exp(V_{BE} / 0.026) - 1 = 5 * 10^6$

$V_{BE} / 0.026 = \ln(5 * 10^6)$
$V_{BE} = 0.026 * \ln(5 * 10^6)$
$V_{BE} = 0.026 * 15.425$
$V_{BE} = 0.401$
$V_{omax} = - 0.401 * 16.709$
$V_{omax} = - 6.7$ V

For $I_E = 1$ mA it follows:
$I_C = V_{in} / R_1$
$V_{in} = R_1 * I_C$
$V_{in} = 3.3 * 10^3 * 10^{-3}$
$V_{in} = 3.3$ V

Rewriting Emitter current equation it follows:
$I_E / I_S = \exp(V_{BE} / 0.026) - 1$
$V_{BE} / 0.026 = \ln (I_E) - \ln (I_S)$
$V_{BE} = 0.026 * [\ln (I_E) - \ln (I_S)]$
The term $\ln (I_S)]$ is nulled by Q_2 then it follows:
$V_{BE} = 0.026 * \ln (I_E)$
or
$V_{BE} = 0.026 * \log (e) * \log (I_E)$
$V_{BE} = 0.026 * 2.302 * \log (I_E)$

$V_0 = - 16.709 * V_{BE}$
$V_0 = - 16.709 * 0.026 * 2.302 * \log (I_E)$
$V_0 = - 1.0006 * \log (V_{in} / R_1)$

Ie, there is 1V change of output for each decade change of input. So Input/Output relation is shown in Fig – Log Scale.

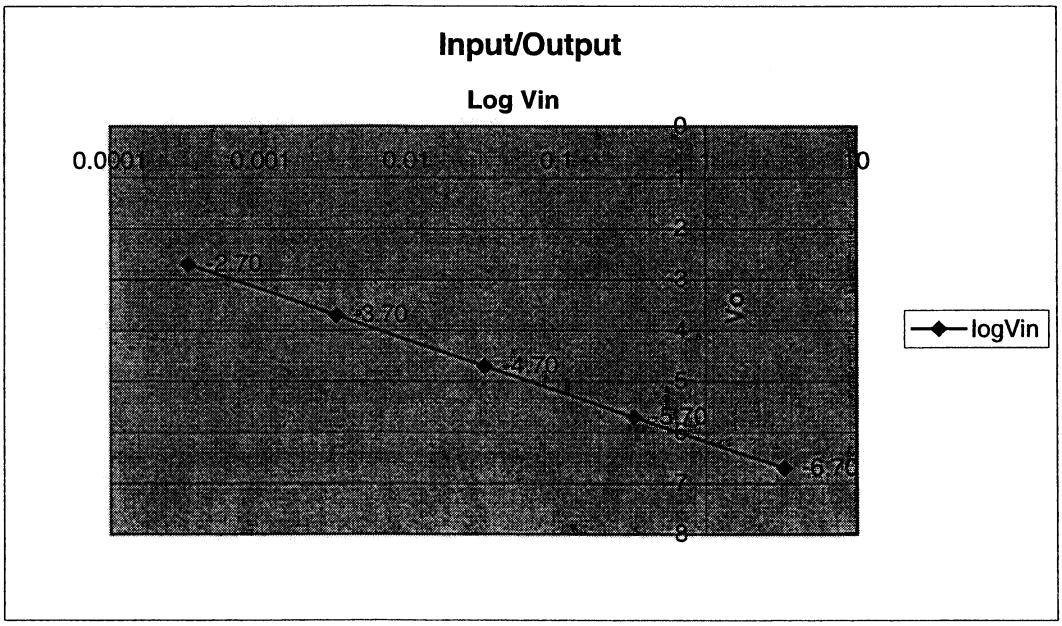
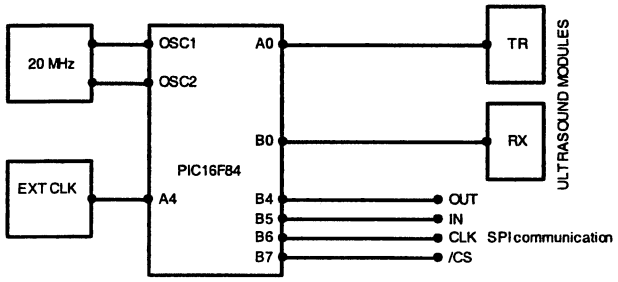


Fig - Log Scale

Question 5

a) One of the possible solution is as follows:



b)

i) The transmit pulse will trigger TR (ultrasound transmitter) from pin A0 and detect receiving pulse from RX (ultrasound receiver) on pin B0 (configured as external interrupt). At the moment of sending command to the transmitter, internal timer will be enabled and start counting from zero with the frequency of the EXTCLK pin A4. (*Possible solution is that local PIC timer can be incremented by internal oscillator using instruction cycle clock).* When receiver interrupts controller on B0, local timer will be disabled, and measured number of clocks will be stored into register for transmission over SPI. This is solution for single distance measure. The local timer is eight bit counter, so every overflow of the timer will generate peripheral interrupt, incrementing counter register. Both, counter register and local timer will represent distance measured by using EXT CLK.

ii) The EXTCLK will be calculated on the basis of the speed of air and required resolution. The speed of the sound in air is 0.34 mm /μs. To measure distance with required resolution, 1mm, EXTCLK should have following frequency:

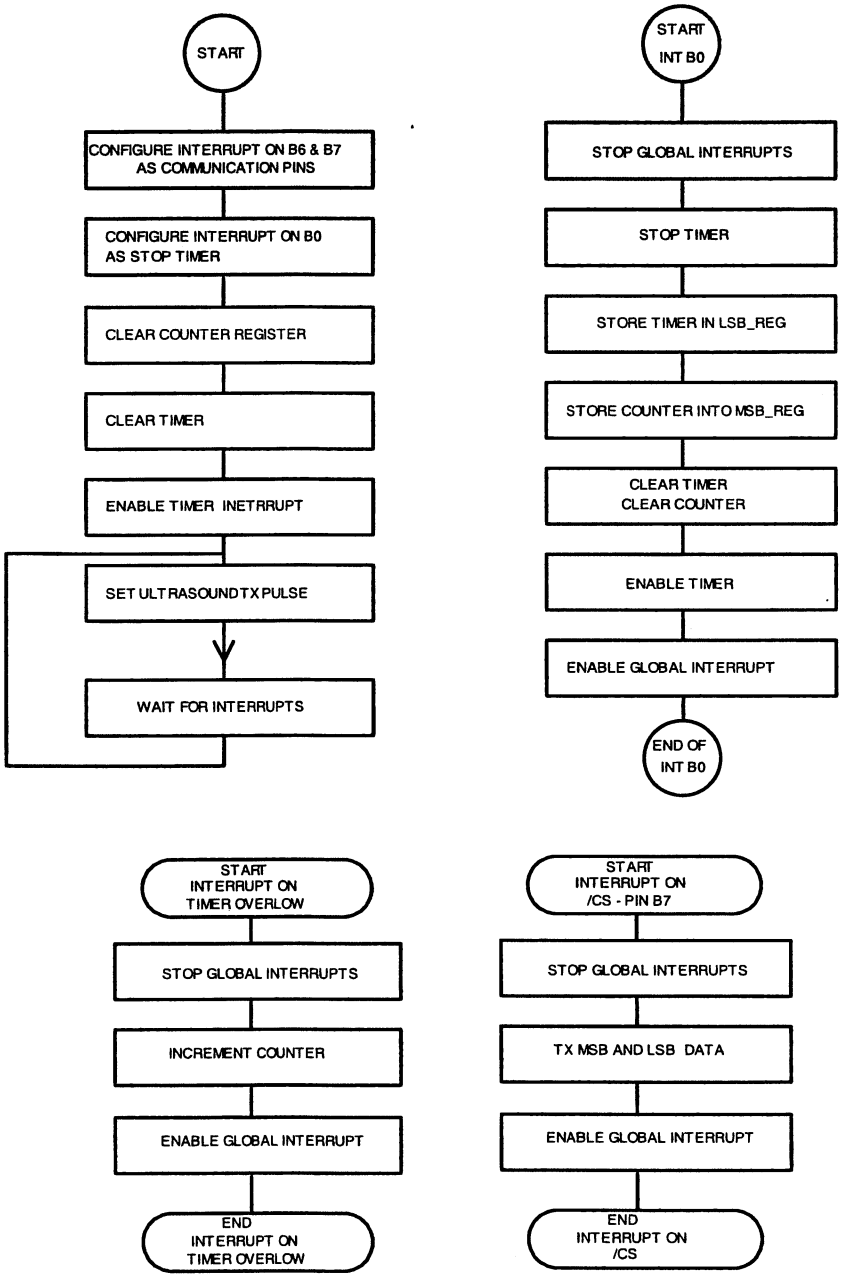
Time_travel_2m = 2000 / 0.34 = 5.88 ms
Time_per_1mm = 1 / 0.34 = 2.94 μs
EXTCLK = 1 / 2.94 * 10^6 = 340 kHz

As measured distance is doubled – transmit + receive path. The EXTCLK must be half of the calculated frequency as follows:

EXTCLK = 170 kHz

The micro-controller instruction clock for 20 MHz oscillator is 5 MHz or 200 ns. If interrupt code can be realized with 14 instruction clocks it will be possible to measure distance with the required resolution.

iii) Software flow diagram



c) Serial communication protocols are divided into synchronous and asynchronous. Synchronous protocols are Microwire or SPI (Simple Peripheral Interface) and I^2C (Inter-integrated circuit protocol). Examples of the Asynchronous protocols are RS232 and CAN protocol. Synchronous protocols have clock controlled by master unit. Asynchronous protocols have transmit and receive line which will trigger receiver on signal change. Advanced protocols as CAN will use commands over transmission line using tokens in order to transfer command and data between units in the network.

d) For the SPI protocol unit will require four dedicated lines: Chip select, Data lines (IN & OUT) and Clock line. The lines Chip select and Clock can be connected for the PORT B of the micro-controller and using interrupt on change to realize synchronization with the remote unit. The Data Lines can be dedicated to the any of the pins of the PORT A or PORT B. One of the possible solution can be as follows:

Chip Select -	pin 13 - B7	(interrupt on change)
Clock -	pin 12 - B6	(interrupt on change)
Data line IN -	pin 11 - B5	(data input)
Data line OUT-	pin 10 - B4	(data out)