ENGINEERING TRIPOS PART IIB

Wednesday 27 April 2005 9am – 10.30am

Module 4B2

POWER ELECTRONICS AND APPLICATIONS

Answer not more than ***three*** *questions*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

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1. (a) The circuit in Fig. 1 shows a typical power electronics AC-DC converter. Explain briefly the operation of the circuit and demonstrate that the output voltage is proportional to the power device duty cycle. If the rectified voltage V_d = 350 V and turns-ratio of the transformer N_2/N_1= 1/35 find the output voltage for a duty cycle, D = 50%. [30%]

(b) The waveforms of an Insulated Gate Bipolar Transistor (IGBT) are shown in Fig. 2. The IGBT operates at a switching frequency of 100 kHz with a duty cycle D = 50%. The other parameters are: V_d = 350 V, the off-state leakage current I_{OFF} = 0.1 mA, the on-state current I_{ON} = 1 A, the on-state voltage V_{ON} = 2 V, the turn-on delay time t_d = 0.1 μs, the rise time t_r = 0.2 μs, the turn-off delay time t_s = 0.1 μs, the turn-off voltage growth time t_g = 0.3 μs and the current fall time t_f = 0.6 μs. Note that the turn-on is specific to resistive loads while turn-off switching is specific to inductive conditions.

(i) Estimate the static, switching and total power losses in the IGBT. [50%]

(ii) Given the answer above, what would be a more appropriate switching frequency to balance the losses in the system. [20%]

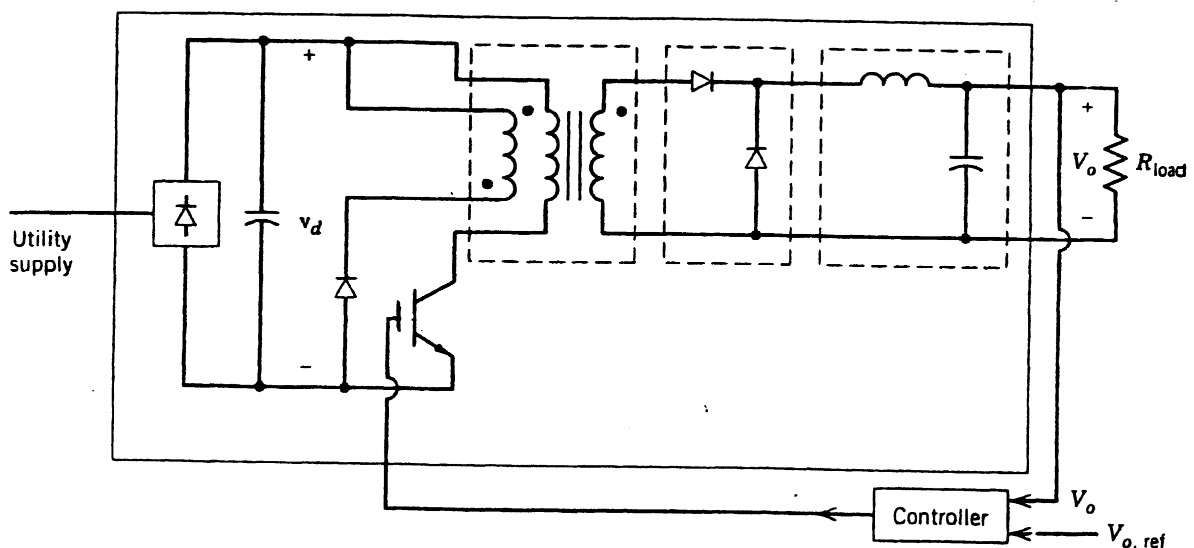

Fig. 1

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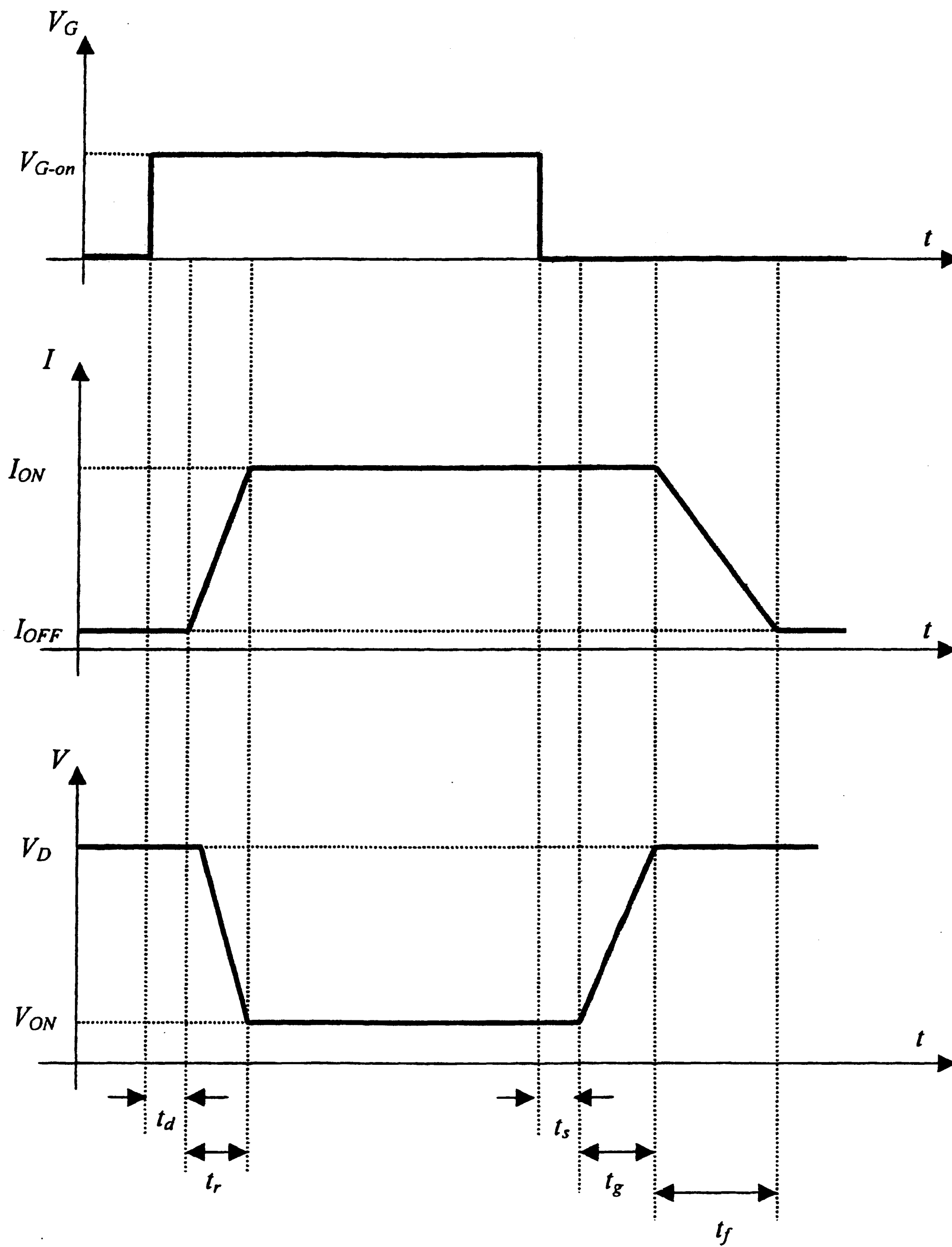

Fig. 2

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2. (a) Explain briefly what are the structural and operational differences between Punch-Through (PT) and Non-Punch Through (NPT) power junctions. For a power MOSFET what is a more appropriate design to use and why ? [30%]

(b) The NPT power diode shown in Fig. 3 incorporates an intrinsic region of a fixed width *d*, placed within the drift region n- at a certain distance *s* from the *p+/n-* physical junction. The doping of the n- drift layer N_D is considerably lower than that of the *p+* layer N_A and considerably larger than that of the intrinsic region N_i.

(i) Sketch the electric field distribution as a function of the distance, across the diode. Where is the maximum electric field located and what is the optimal position of the intrinsic region within the n- drift region ? [25%]

(ii) Calculate the breakdown voltage of the diode as a function of the thickness of the intrinsic region *d*, its position *s*, the doping of the layers and the critical electric field. [25%]

(iii) Draw a graph showing the breakdown voltage as a function of the position of the intrinsic region with all the other parameters being constant. [20%]

Assume that the width of the n- region is in all cases much larger than the maximum depletion region at breakdown. State any other assumptions made.

You may also assume the following equation in an abrupt p+/n- junction :

$$w = \left[\frac{2\varepsilon_r\varepsilon_0 V}{q}\frac{1}{N_D}\right]^{\frac{1}{2}}$$

where *w* is the depletion region width; *V* is the reverse voltage and the other symbols have their usual meaning.

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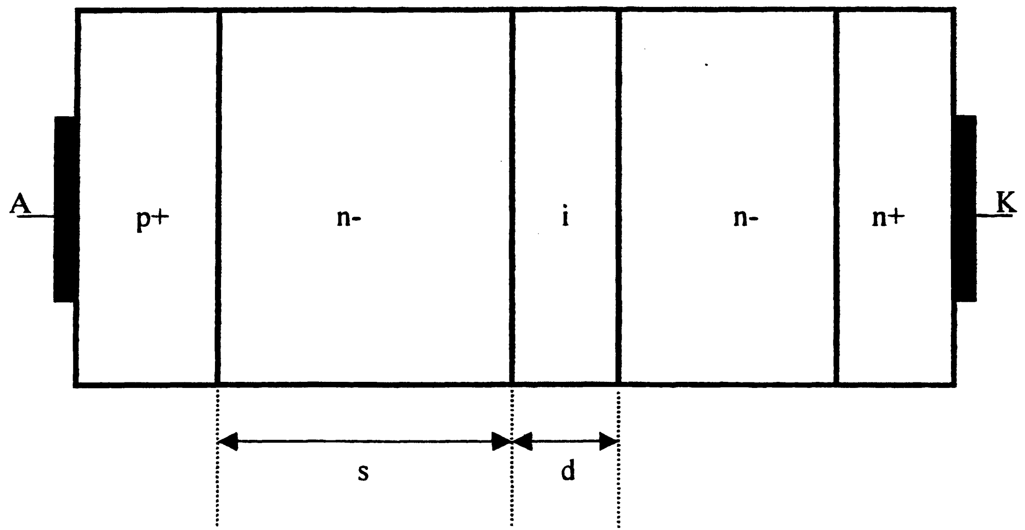

Fig. 3

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3. (a) Describe the on-state operation of a Gate Turn-off thyristor (GTO) showing a cross-section and an equivalent circuit indicating the build-up of mobile charge (plasma) for different current densities. Explain the turn-off behaviour and the distribution of plasma in this regime. [40%]

(b) Explain all the operational consequences (and the associated trade-offs) of increasing or reducing the p-well doping in a vertical Insulated Gate Bipolar Transistor (IGBT). [30%]

(c) An IGBT is found to operate incorrectly in the on-state due to latch-up. Explain the latch-up phenomenon and briefly discuss how you would redesign the structure to prevent the latch-up. Considering that the lateral resistance in the p-well under the n+ cathode of the IGBT is 20 Ω and the current gain (α_{pnp}) of the pnp bipolar transistor is 0.3 what is the approximate anode current at which static latch-up occurs ? [30%]

4. (a) State the advantages and disadvantages of SOI technology in high voltage ICs. [20%]

(b) Fig. 4 shows a novel four terminal high voltage device. Explain the operation of the device in off-state and on-state. Also explain the turn-on and turn-off phenomena function of the action of the two gates. What are the advantages and disadvantages of such a device compared to a classical Lateral Insulated Gate Bipolar Transistor (LIGBT) ? [50%]

Explain what is the influence of the L_{p1} and L_{p2} parameters shown in Fig. 4 on the operation of the device. What is the purpose of the n-well and what are the considerations in choosing the doping of this layer ? [30%]

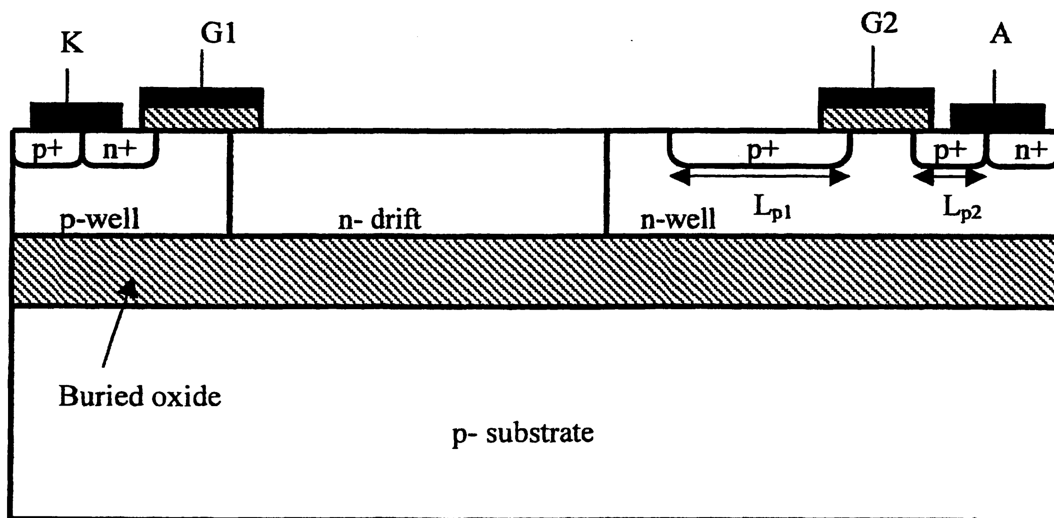

Fig. 4

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Answers 4B2 – 2005 – Power Electronics

1.

(a) Vout=5V

(b)

- On-state losses: 0.94W
- Off-state losses:0.014W
- Turn-on losses: 1.18 W
- Turn-off losses: 15.83W
- TOTAL losses: 17.96W

(c) fopt is approx 6kHz

2.

(a) s=0

(b) $V_{BR} = \frac{\varepsilon_0 \varepsilon_r E_{critical}}{2qN_D} + E_{critical} d - \frac{qN_D s}{\varepsilon_0 \varepsilon_r}$

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(c) I_{latch} =0.1 A (considering that the cathode junction opens at 0.6 V)