UNIVERSITY OF CAMBRIDGE

ENGINEERING TRIPOS PART IIB

Tuesday 10 May 2005 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

Answer not more than three questions.

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right hand margin.*

Supplementary page:
Extra copy of Fig. 1 (Question 1).

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

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1 (a) Outline briefly the advantages and disadvantages of complementary metal oxide semiconductor (CMOS) technology, and explain why silicon-based technology dominates over other semiconductors. [20%]

(b) Figure 1 shows layouts of two different CMOS gates using n-well technology and a p-type substrate, with power supply V_{DD} labelled *A* and power supply V_{SS} labelled *B*.

(i) Explain the operation of each gate and the logic functions of the connections *P*, *Q*, *R*, *S*, *T* and *U*. [15%]

(ii) On the supplementary copy of Fig. 1, label which regions are implanted with p-type impurities and which regions are implanted n-type. Draw on that copy a possible location for the n-type well, and shade in the active regions of all of the n-channel transistors. [15%]

(iii) Taking measurements from Fig. 1, calculate the ratio r_{NP} of the widths of the n-channel to the p-channel transistors in each of the logic gates in Fig. 1. [10%]

(c) Taking the electron mobility in silicon to be twice as large as the hole mobility, comment on the switching performance of each of the logic gates in Figure 1. For incorporation into a general purpose logic circuit, calculate the optimum design value ratio for r_{NP} to maximize the switching speed. [20%]

(d) Outline why the performance of CMOS circuits improves when the minimum lithographic linewidth is reduced. With reference to Fig. 1, explain which dimensions are most important in determining circuit performance. Comment briefly on possible limitations in CMOS circuit performance as the available fabrication technology is projected to improve over the next decade. [20%]

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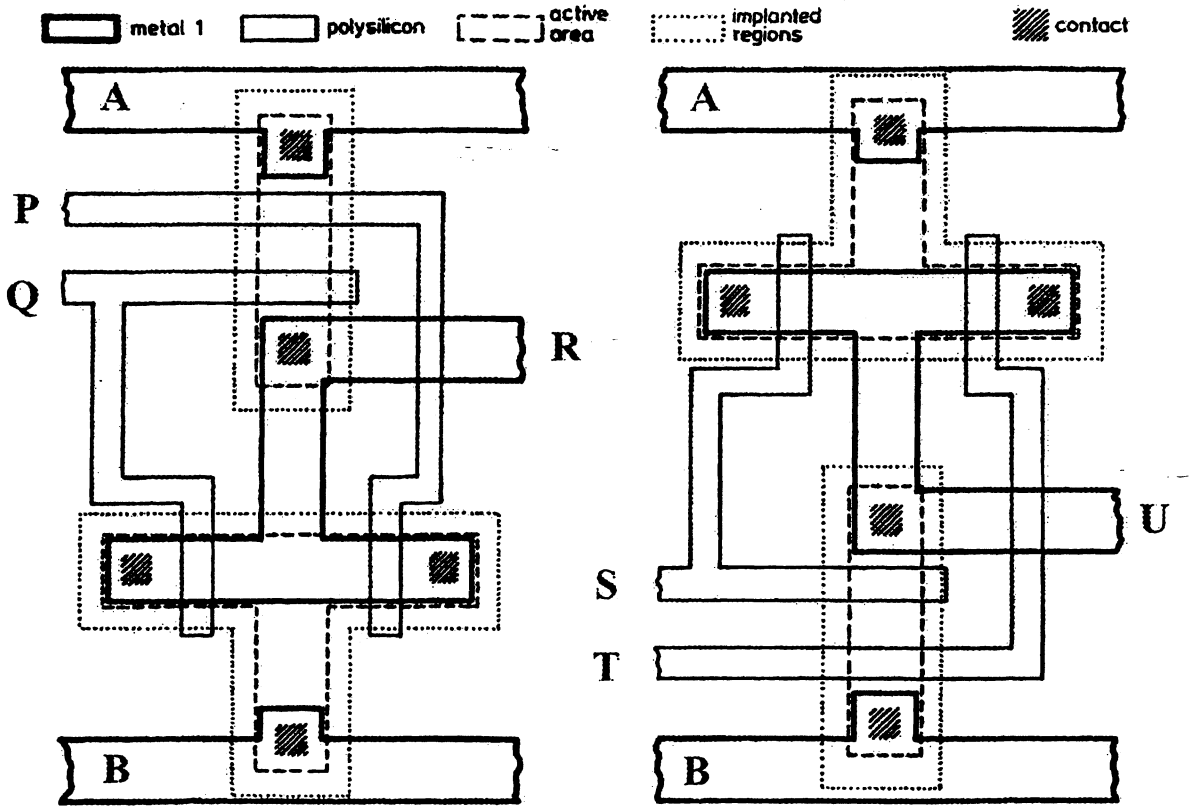
metal 1
polysilicon
active area
implanted regions
contact
A
P
Q
R
B
A
U
S
T
B

Fig. 1

2 (a) Discuss how the switching performance of integrated silicon transistor circuits is measured, and the limitations of accessing small devices through relatively large input and output contact pads. Taking the example of a CMOS inverter, explain the main factors which are important in determining the device switching speed. [20%]

Figure 2 shows partially labelled experimental data from 113-element ring oscillators with the ring oscillator frequency displayed as a function of power supply voltage, for two different chips, at 77 K and 300 K.

(b) Discuss the main features in Fig. 2. State which traces correspond to each temperature, and comment on the comparative characteristics of the two chips. [20%]

(c) Explain how you would expect the total current drawn by the ring to vary with power supply voltage. [10%]

(d) Describe what you would expect to observe as a chip is cooled down from room temperature with the power supply at:

(i) 3 V;

(ii) 1.5 V. [20%]

(e) Outline why the data in Fig. 2, derived entirely from simple inverter circuits, give a misleadingly optimistic impression of the performance of logic circuits. Explain how the ring oscillator design could be adapted to provide a more realistic model of typical logic circuit behaviour. [20%]

(f) The data in Fig. 2 are based on 2 μm minimum line-width technology from the last millennium. Explain how the ring oscillator frequency is expected to scale with this minimum line-width, and comment on how closely present commercial device technology is approaching any theoretical limits to this performance scaling. [10%]

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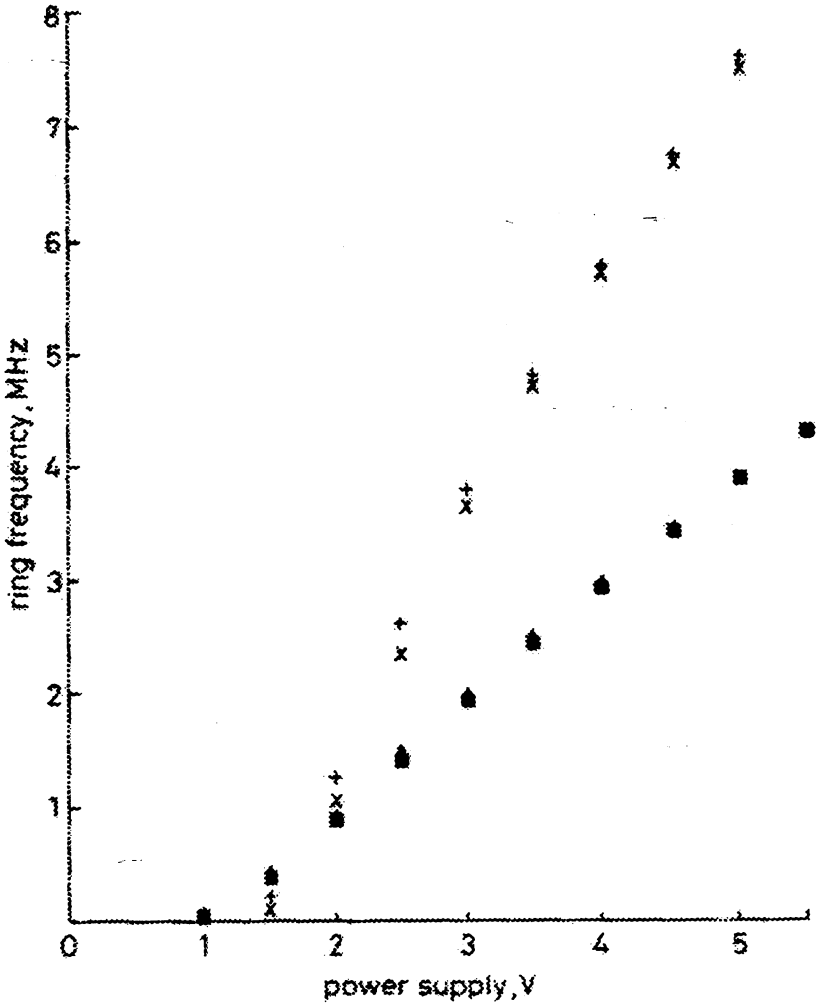

Fig. 2

3 Consider the circuit of Fig. 3, in which an NMOS transistor *M1* is connected in a circuit designed to provide a reference voltage V_{REF}.

(a) Derive an expression relating V_{REF} with the drain current I, transistor parameters and other circuit constants. [20%]

(b) The transistor dimensions W and L are chosen as 80 μm and 4 μm respectively, V_{DD} and V_{SS} are 12 V and 0 V respectively, and other transistor parameters are given below. Deduce a suitable value for R if V_{REF} is to be 2 V, and determine the drain current I. [20%]

(c) What is meant by the following terms in the context of the performance of voltage references, and why are they important?

(i) Power supply sensitivity

(ii) Fractional temperature coefficient [20%]

(d) Write a short account of the approaches available to the CMOS IC designer for generating stable reference voltages for use in integrated circuit designs. Your account should mention power consumption, stability, area occupied, and any other factors you consider to be important. [40%]

For *M1*, $V_T = +1$ V, and $\mu_N \varepsilon / t_{OX} = 20 \times 10^{-6}$ AV^{-2}.

You may assume the following expressions for the drain current I_D in a MOS transistor.

$$I_D = \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \qquad 0 < V_{DS} < V_{GS} - V_T$$

$$I_D = \frac{1}{2} \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} (V_{GS} - V_T)^2 \qquad 0 < V_{GS} - V_T < V_{DS}$$

(cont.

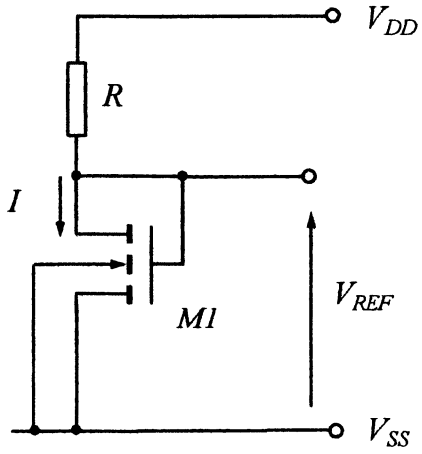

Fig. 3

(TURN OVER

4 (a) Describe the circuit structures required in CMOS IC design to convey signals between logic gates comprising small geometry MOSFETs and the output pads. [30%]

(b) Discuss the precautions that are necessary:

(i) to minimise the area occupied by the pad driver;
(ii) to prevent latchup. [10%]

(c) A non-inverting CMOS output pad driver consists of four appropriately designed inverters connected in cascade. It is required to transmit the signal from the output of a minimum geometry gate to an output pad. The pad and external circuitry impose a purely capacitive load of 90 pF. The capacitance to substrate measured at the input to the first inverter is 150 fF, and the channel dimensions W and L for the n-channel transistor used in its construction are 1 μm and 0.5 μm respectively.

(i) Show how to specify the channel dimensions of the transistors used in the remaining three stages of the pad driver so as to minimise the delay imposed on the transmitted signal, and determine the dimensions and the minimum delay. All stages are to have propagation delays equalised for rising and falling edges. [40%]

(ii) Discuss whether it is possible to devise an alternative design that would be expected to result in a smaller delay, if the driver is required to provide a non-inverted output. [20%]

You may assume that the delay τ imposed on a signal by a CMOS inverter driving a capacitive load C is given by:-

$$\tau = \frac{3C}{\mu C_{OX} V_{DD} (W/L)}$$

where μ is the mobility of the carriers concerned, C_{OX} is the specific capacitance of the gate electrode, V_{DD} is the power supply voltage, and W/L is the channel aspect ratio. Take $\mu_N/\mu_P = 2$, $\mu_N C_{OX} = 2.5 \times 10^{-4}$ AV^{-2}, and $V_{DD} = 3$ V.

5 (a) The constant field model of MOS scaling applies a dimensionless factor k to manufacturing dimensions (length, width and thickness), voltages and doping densities, so that electric fields remain unchanged. For example, with $k = 1$, the dimensions are unchanged; with $k = 1.1$, they would be slightly reduced. Based on the method of dimensions, derive appropriate expressions for the consequent scaling of the following parameters:

(i) gate area
(ii) gate delay
(iii) parasitic capacitance
(iv) current
(v) static power consumption (per inverter gate)
(vi) power density (per unit area)
(vii) current density (in wires)
(viii) signal delay due to interconnect [50%]

(b) Discuss the main implications of the effects listed in (a) for size, speed and power consumption in digital CMOS designs. [20%]

(c) What further factors make this model inappropriate as device sizes continue to decrease? [30%]

END OF PAPER

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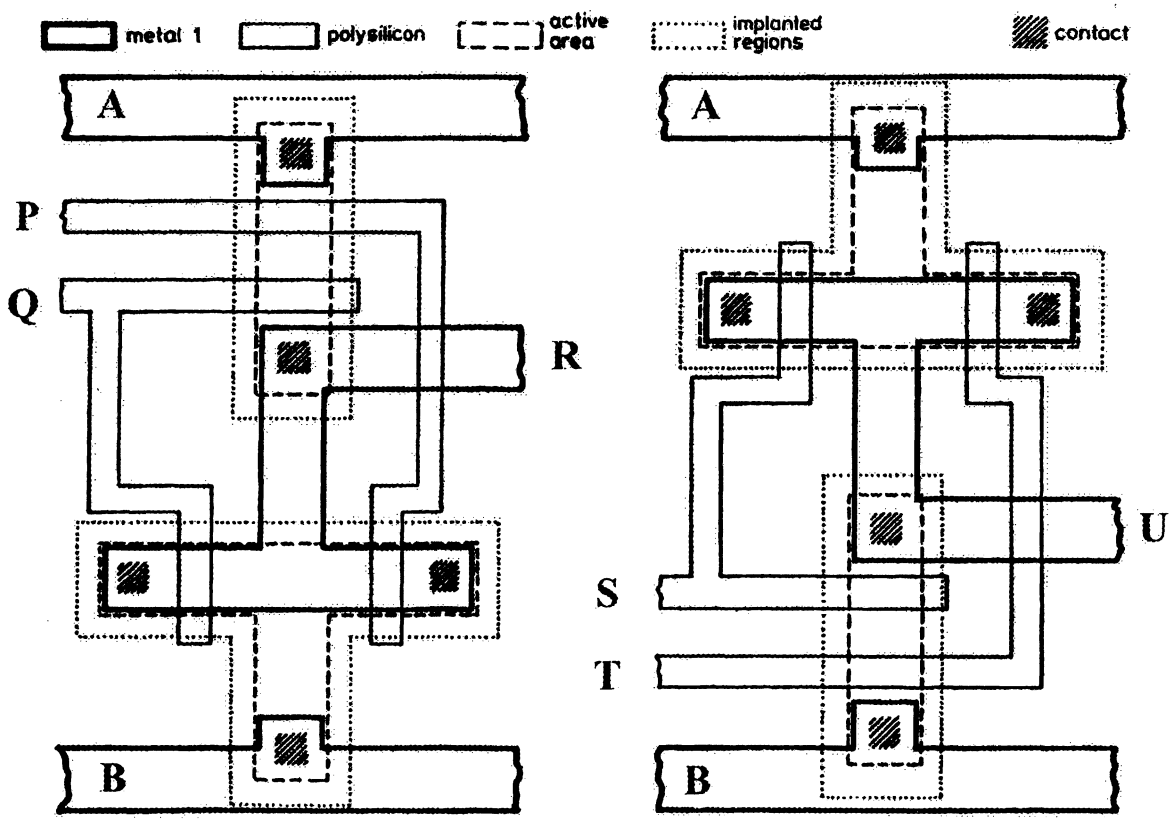

Additional copy of Fig. 1
(may be handed in with your script)