ENGINEERING TRIPOS PART IIB

Monday 2 May 2005 9:00 to 10:30

Module 4B8

ELECTRONIC SYSTEM DESIGN

*Answer no more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachments:
PIC16F84 data sheet (6 pages)

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

(TURN OVER

1. Figure 1 shows the block diagram of a charge-balance type voltage to frequency converter. The monostable is positive edge triggered, and its output pulse is positive-going. When the pulse is high, the switch that it controls is switched to position 1, i.e. connection is made to the op amp input.

a) If all circuit elements are ideal, show that the output frequency, f_0, is given by:

$$f_0 = V_{in} / (R_{in} I_c T_1)$$

where T_1 is the output pulse duration of the monostable. [40%]

b) Derive an expression for the error in output:
   (i) If the op amp used for the integrator has an input bias current of I_b, all other components being ideal; [20%]
   (ii) If the comparator has an input offset voltage of V_{io}, all other components being ideal. [20%]

c) Determine the maximum value for the T_1 under the following conditions:

The range of V_{in} is 0 V to +2 V
V_{int} can swing between –4 V and + 4 V
C_{int} is 2200 pF
I_c is 1 mA. [20%]

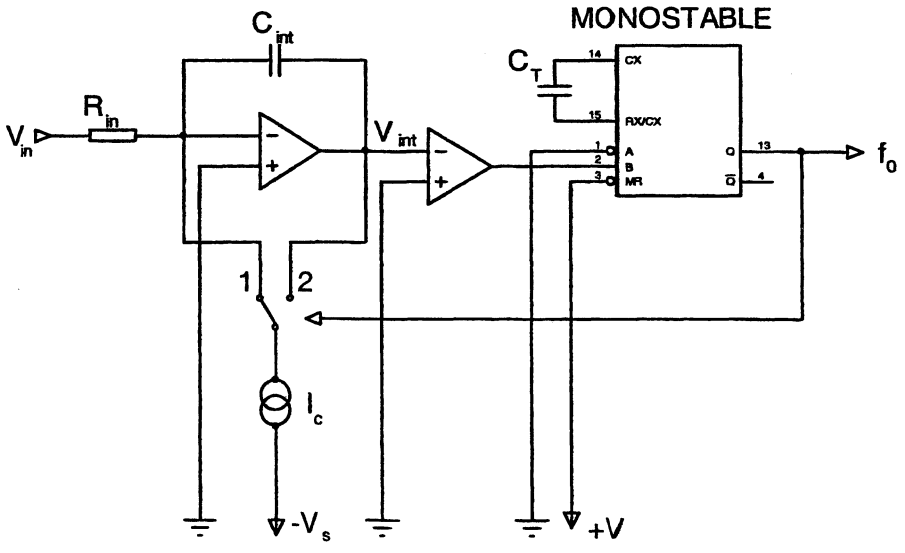


Fig 1.

2. Figure 2 shows two sinusoidal voltages, one labeled as input and the other labeled as output. The input and output sinusoidal signal have same frequency, f = 1000 Hz, but different amplitudes.

a) Draw a proposed circuit which will produce the required relations between the input and output sinusoidal signals using no more than four components including an op-amp. [30%]

b) Calculate component values for the circuit assuming an ideal amplifier. [50%]

c) Explain what changes you expect with the change of the frequency. [20%]

Note: $V_{in}(t) = \sin(2\pi f\ t)$ V and $V_{out}(t) = 2\sin(2\pi f\ t + 120^0)$ V

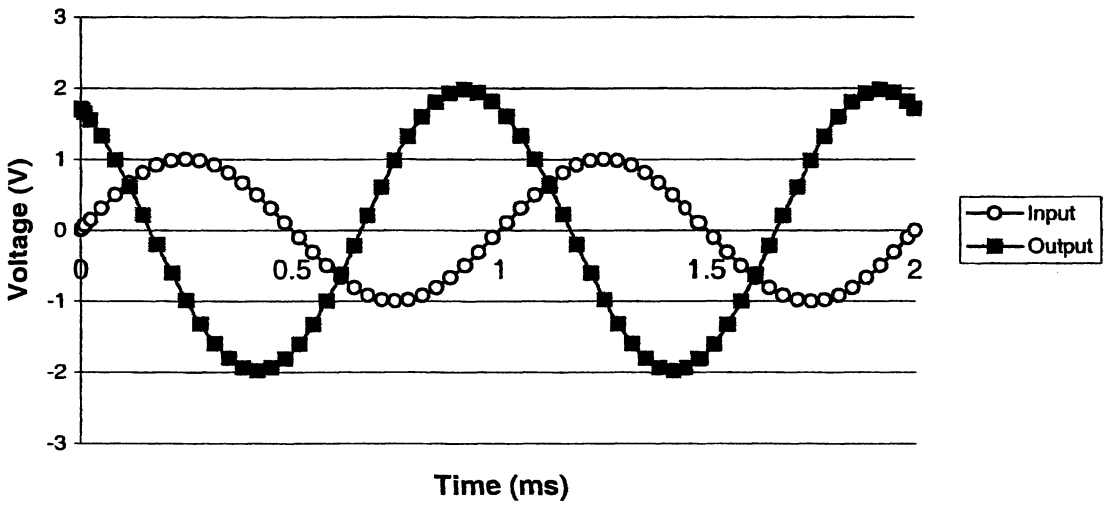


Fig 2

3. a) A second order low pass filter with a –3dB point at 250 Hz is to have a numerical gain of 40 in its passband. An op-amp with a gain-bandwidth product of 10^5 is to be used. Explain clearly if this type of op-amp is satisfactory. The op-amp has a nominal slewing rate of 0.6V / μs; would this limit the filter performance? [30%]

b) This same filter circuit is to have a *Chebychev* response between the input voltage V_1 and the output voltage V_2 of the form:

$$V_2 / V_1 = A\,\omega_0^2 / (s^2 + 0.804\,\omega_0\,s + 0.637\,\omega_0^2) \quad \text{where } s = j\,\omega.$$

How would this response look on a voltage gain against frequency, ω, plot? [10%]

c) This filter is to use the circuit shown in Fig 3. Obtain an equation for the gain of the circuit relating V_2 / V_1 to the values of the two equal capacitors of value *C* and to the values of the resistors R_1, R_2, R_3 *and* R_5 and using $s = j\omega$. Determine values for ω_0^2 and $A\omega_0$. Consider the given equation for gain at *very low* frequencies: what function will the voltage then become in terms of *A* and any of the given constants? Determine which resistors set this gain. Which resistors set the turnover frequency ω_0 for a given value of C and which sets the circuit's input resistance? [35%]

d) If C = 22nF, determine values for all the components needed for the filter if its minimum input resistance is to be 10 kΩ. Why might one choose a value in the region of 10 kΩ for the two equal resistors R_4? [25%]

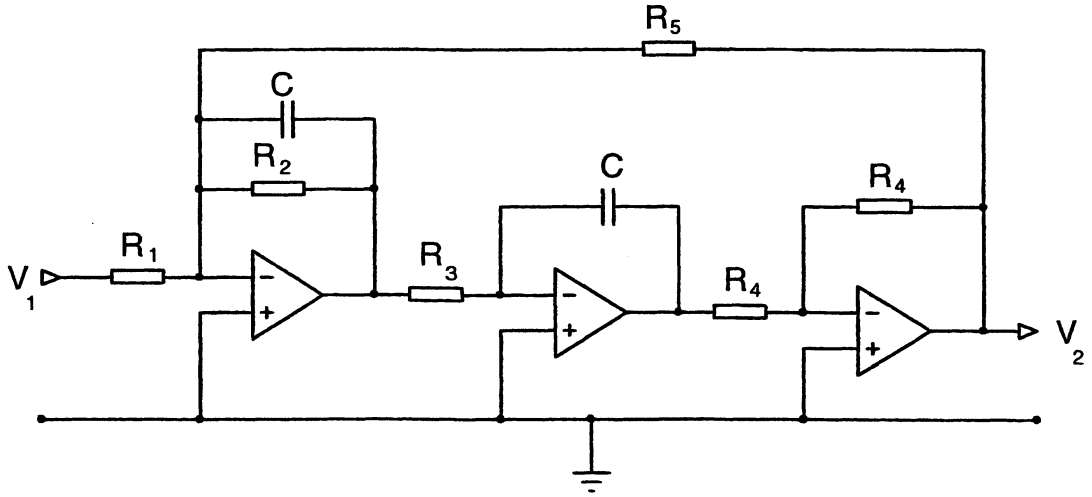


Fig 3

4. a) In the "logarithmic amplifier" shown in Fig 4, why is a pair of transistors Q_1 and Q_2 used rather than diodes? Why is a transistor with a current gain of 300 or more desirable? Write brief notes about the main features of the arrangement of the circuit. [35%]

b) The emitter current I_E of the transistor Q_1 is given by:

$$I_E = I_S (exp (V_{BE} / 0.026) - 1)$$

where I_S = 0.2 nA is the reverse saturation current of the junction, and V_{BE} is the base-emitter voltage. Determine the *minimum* output voltage of the circuit, V_0 for the errors to be under 0.5% of the expected logarithmic relation. [20%]

c) If a circuit of input resistance of 3.3 kΩ is needed, what is the maximum output voltage V_0 for an emitter current in Q_1 of 1 mA? What input V_{IN} does this correspond to? Sketch *carefully* salient features of the output versus input voltage relation for the circuit. [45%]

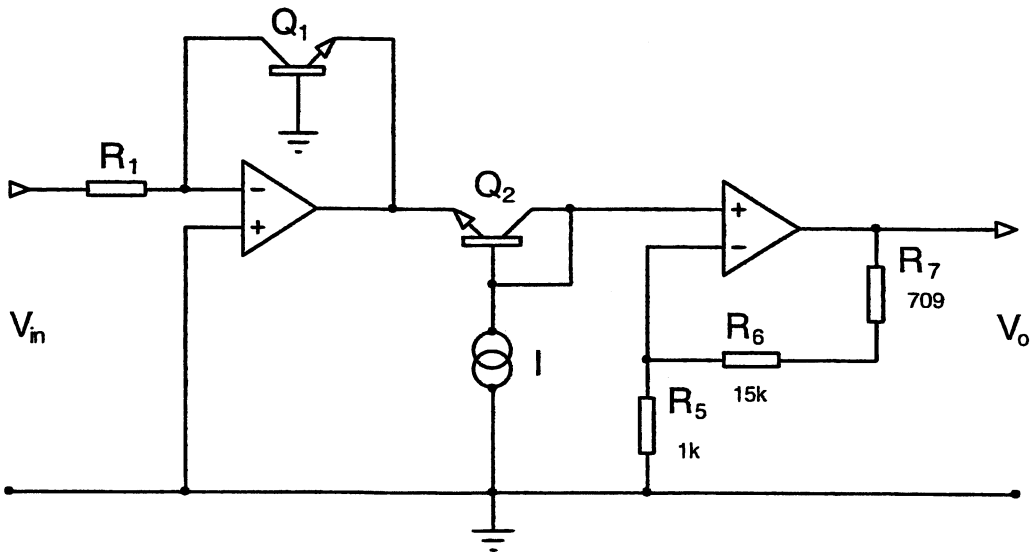


Fig 4.

5. An ultrasound distance-measuring device measures the time between a generated pulse and the reflected pulse from a solid object. You are required to design such a device using a PIC16F84 micro-controller. The ultrasound distance-measuring device will be controlled remotely using serial communication. The frequency of the micro-controller clock is 20 MHz.

a) Draw a block diagram using the micro-controller data from data sheets attached. * [20%]

b) The measuring range of the device should be 1 m and the resolution 1mm.**

(i) Describe how you will measure distance based on the suggested micro-controller. [10%]

(ii) Calculate the minimum distance that you will be able to measure and explain what parameters determine this value. [10%]

(iii) Draw a software flow diagram for the proposed design presenting all steps during the measurement cycle and remote communication. [20%]

c) Define serial communications protocols and describe their features. [20%]

d) Briefly explain how SPI (Simple Peripheral Protocol) can be realised within your design annotating relevant pins of the micro-controller and define the functionality of the pin(s). [20%]

* Note: The ultrasound transmitter and receiver are ideal and with TTL input /output respectively.

** Note: The speed of the sound in air is 340 m/s.

END OF PAPER

MICROCHIP

PIC16F84A

18-pin *Enhanced* FLASH/EEPROM 8-Bit Microcontroller

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single-cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of Data RAM
- 64 bytes of Data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 Special Function Hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt-on-change
  - Data EEPROM write complete

Peripheral Features:

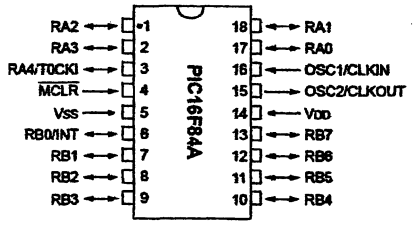
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

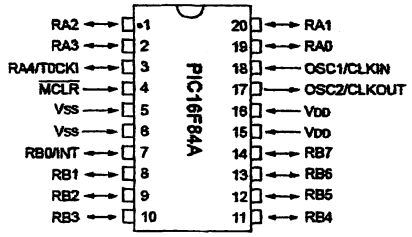
- 10,000 erase/write cycles *Enhanced* FLASH Program memory typical
- 10,000,000 typical erase/write cycles EEPROM Data memory typical
- EEPROM Data Retention > 40 years
- In-Circuit Serial Programming™ (ICSP™) - via two pins
- Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own On-Chip RC Oscillator for reliable operation
- Code protection
- Power saving SLEEP mode
- Selectable oscillator options

Pin Diagrams

PDIP, SOIC



SSOP



CMOS Enhanced FLASH/EEPROM Technology:

- Low power, high speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 5.5V
  - Industrial: 2.0V to 5.5V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 0.5 µA typical standby current @ 2V

TABLE 1-1: PIC16F84A PINOUT DESCRIPTION

Pin Name	PDIP No.	SOIC No.	SSOP No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	18	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	19	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$	4	4	4	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0	17	17	19	I/O	TTL	
RA1	18	18	20	I/O	TTL	
RA2	1	1	1	I/O	TTL	
RA3	2	2	2	I/O	TTL	
RA4/T0CKI	3	3	3	I/O	ST	Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.
						PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	6	6	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	7	7	8	I/O	TTL	
RB2	8	8	9	I/O	TTL	
RB3	9	9	10	I/O	TTL	
RB4	10	10	11	I/O	TTL	Interrupt-on-change pin.
RB5	11	11	12	I/O	TTL	Interrupt-on-change pin.
RB6	12	12	13	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming clock.
RB7	13	13	14	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming data.
VSS	5	5	5,6	P	—	Ground reference for logic and I/O pins.
VDD	14	14	15,16	P	—	Positive supply for logic and I/O pins.

Legend: I= input O = Output I/O = Input/Output P = Power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

TABLE 4-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0	bit0	TTL	Input/output
RA1	bit1	TTL	Input/output
RA2	bit2	TTL	Input/output
RA3	bit3	TTL	Input/output
RA4/T0CKI	bit4	ST	Input/output or external clock input for TMR0. Output is open drain type.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 4-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
05h	PORTA				RA4/T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
85h	TRISA				TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	---1 1111	---1 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are unimplemented, read as '0'.

TABLE 4-3: PORTB FUNCTIONS

Name	Bit	Buffer Type	I/O Consistency Function
RB0/INT	bit0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3	bit3	TTL	Input/output pin. Internal software programmable weak pull-up.
RB4	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6	bit6	TTL/ST(2)	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7	bit7	TTL/ST(2)	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger.
Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other RESETS
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0/INT	xxxx xxxx	uuuu uuuu
86h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
0Bh,8Bh	INTCON	GIE	EEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

9.3.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 9-6: EXTERNAL CLOCK TIMING

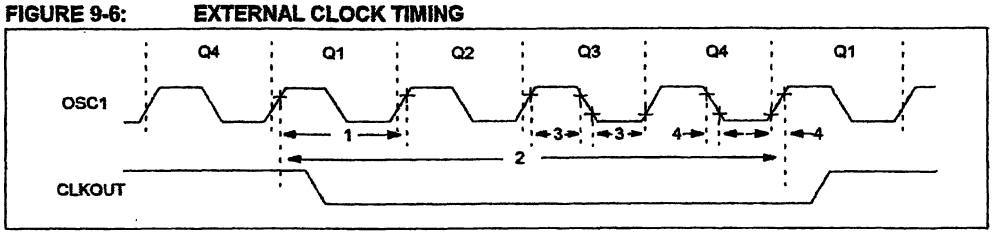


TABLE 9-2: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
	FOSC	**External CLKIN Frequency(1)**	DC	—	2	MHz	XT, RC osc	(-04, LF)
			DC	—	4	MHz	XT, RC osc	(-04)
			DC	—	20	MHz	HS osc	(-20)
			DC	—	200	kHz	LP osc	(-04, LF)
		Oscillator Frequency(1)	DC	—	2	MHz	RC osc	(-04, LF)
			DC	—	4	MHz	RC osc	(-04)
			0.1	—	2	MHz	XT osc	(-04, LF)
			0.1	—	4	MHz	XT osc	(-04)
			1.0	—	20	MHz	HS osc	(-20)
			DC	—	200	kHz	LP osc	(-04, LF)
1	TOSC	**External CLKIN Period(1)**	500	—	—	ns	XT, RC osc	(-04, LF)
			250	—	—	ns	XT, RC osc	(-04)
			50	—	—	ns	HS osc	(-20)
			5.0	—	—	µs	LP osc	(-04, LF)
		Oscillator Period(1)	500	—	—	ns	RC osc	(-04, LF)
			250	—	—	ns	RC osc	(-04)
			500	—	10,000	ns	XT osc	(-04, LF)
			250	—	10,000	ns	XT osc	(-04)
			50	—	1,000	ns	HS osc	(-20)
			5.0	—	—	µs	LP osc	(-04, LF)
2	TCY	**Instruction Cycle Time(1)**	0.2	4/FOSC	DC	µs		
3	TOSL, TOSH	**Clock in (OSC1) High or Low Time**	60	—	—	ns	XT osc	(-04, LF)
			50	—	—	ns	XT osc	(-04)
			2.0	—	—	µs	LP osc	(-04, LF)
			17.5	—	—	ns	HS osc	(-20)
4	TOSR, TOSF	**Clock in (OSC1) Rise or Fall Time**	25	—	—	ns	XT osc	(-04)
			50	—	—	ns	LP osc	(-04, LF)
			7.5	—	—	ns	HS osc	(-20)

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Min." values with an external clock applied to the OSC1 pin.
When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 9-9: TIMER0 CLOCK TIMINGS

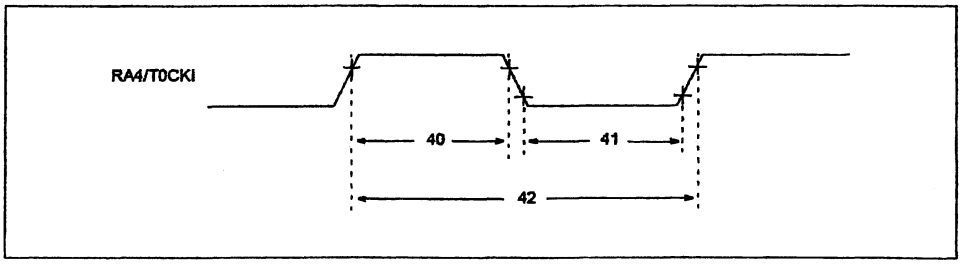


TABLE 9-5: TIMER0 CLOCK REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	50	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				30	—	—	ns	3.0V ≤ VDD ≤ 6.0V
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	50	—	—	ns	2.0V ≤ VDD ≤ 3.0V
				20	—	—	ns	3.0V ≤ VDD ≤ 6.0V
42	Tt0P	T0CKI Period		$\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (2, 4, ..., 256)

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.