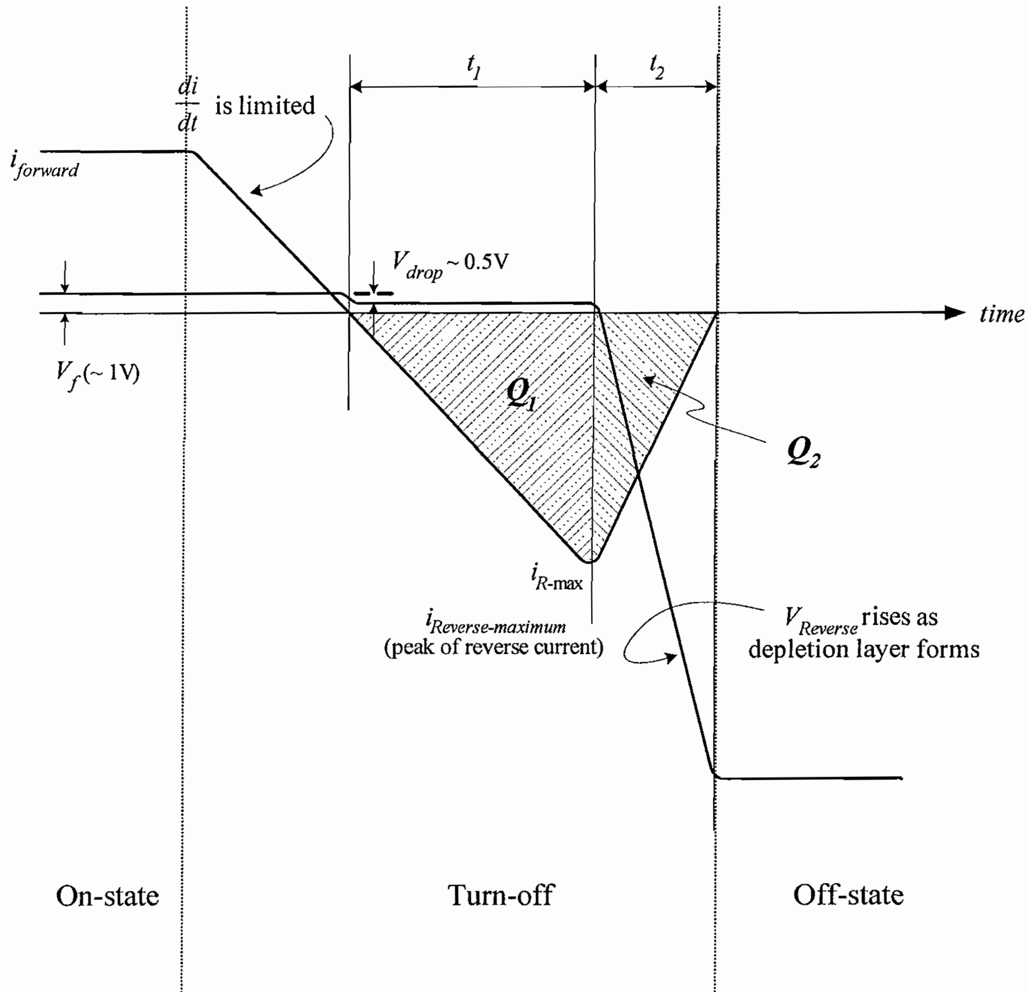
1. (a)



Turn-off

- di/dt is limited by the external circuit. As an attempt is made to reverse-bias the diode, the current starts decreasing and flows in the opposite direction as plasma is still present.
- Q1 is associated with the plasma in the drift region and t1 is the time taken to remove it.
- Once plasma is removed at the end of t1, a depletion region starts to grow and the reverse voltage across the diode can increase. At the end of this region the device can block the voltage and the current decreases to a leackage level. [30%]
-

(b). The device is an IGBT. The turn-off is shown to be comprised of a first fall, associated with the drop in the electron current (as the channel (MOS inversion layer) is suppressed) and the second drop is usually associated with the hole sweep out and recombination of plasma. This takes a longer time to remove. I*h* is approximately equal to the original hole current at the cathode side (as the electron current drops very fast when the channel is 'killed'). [20%]

(b) (ii) $T = \frac{1}{f_s} = \frac{1}{100\,kHz} = 10\,\mu s$ $\quad D = 50\% \Rightarrow DT = 5\,\mu s$

$DT = t_{ON} + t_r + t_d = 5\,\mu s \Rightarrow t_{on} = 5 - 0.1 - 0.2 = 4.7\,\mu s$

$(1-D)T = t_{off} + t_s + t_g + t_{f1} + t_{f2} \Rightarrow t_{off} = 5 - 0.1 - 0.3 - 0.5 - 0.1 = 4\,\mu s$

- $P_{ON} = \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON}\,dt = V_{ON} \cdot I_{ON} \cdot \frac{t_{ON}}{T} = 3 \cdot 1 \cdot \frac{4.7}{10} = 1.41\,W$

- TURN-ON

$P_r = \frac{1}{T}\int_0^{t_r} V_{dc} \frac{I_{on} \cdot t}{t_r} \cdot dt = \frac{V_{dc}\, I_{on} \cdot t_r}{2T} = 2\,W$

- $P_d = \frac{1}{T}\int_0^{t_d} I_{ON} V(t)\,dt = \frac{1}{T}\int_0^{t_d} I_{ON}\left[V_{dc} + (V_{ON} - V_{dc})\frac{t}{t_d}\right]dt =$

$= \frac{I_{ON} \cdot t_d}{2T}(V_{dc} + V_{ON}) = \frac{1 \cdot 0.2}{2 \cdot 10} \cdot 403 = 4.03\,W$

- TURN-OFF

$P_s = V_{ON} \cdot I_{ON} \cdot \frac{t_s}{T} = 3 \cdot 1 \cdot \frac{0.1}{10} = 0.03\,W$ (negligible)

$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left[V_{ON} + \frac{V_{dc} - V_{ON}}{t_g} t\right] dt =$

$= \frac{1}{2T} I_{ON} \cdot t_g (V_{ON} + V_{dc}) = \frac{1}{2 \cdot 10} 1 \cdot 0.3 \cdot 403 = 6.05\,W$

$P_{f1} = \frac{1}{T}\int_0^{t_{f1}} V_{dc}\left[I_{ON} + (I_h - I_{ON})\frac{t}{t_{f1}}\right] dt =$

$= \frac{1}{2T} V_{dc}\, t_{f1}\left[I_{ON} + I_h\right] = \frac{1}{2 \cdot 10} \cdot 400 \cdot 0.1 \cdot 1.3 = 2.6\,W$

$P_{f2} = \frac{1}{T} V_{dc} \cdot t_{f2} \cdot \frac{I_h}{2} = \frac{1}{2 \cdot 10} \cdot 400 \cdot 0.5 \cdot 0.3 = 3\,W$

ON-STATE LOSSES = 1.41 W

OFF-STATE LOSSES = 0 W

TURN-ON LOSSES = 2 W + 4.03 W = 6.03 W

TURN-OFF LOSSES = 0.03 + 6.05 + 2.6 + 3 = 11.68 W

TOTAL LOSSES = 1.41 + 6.03 + 11.68 = **19.12 W**

[50%]

2.

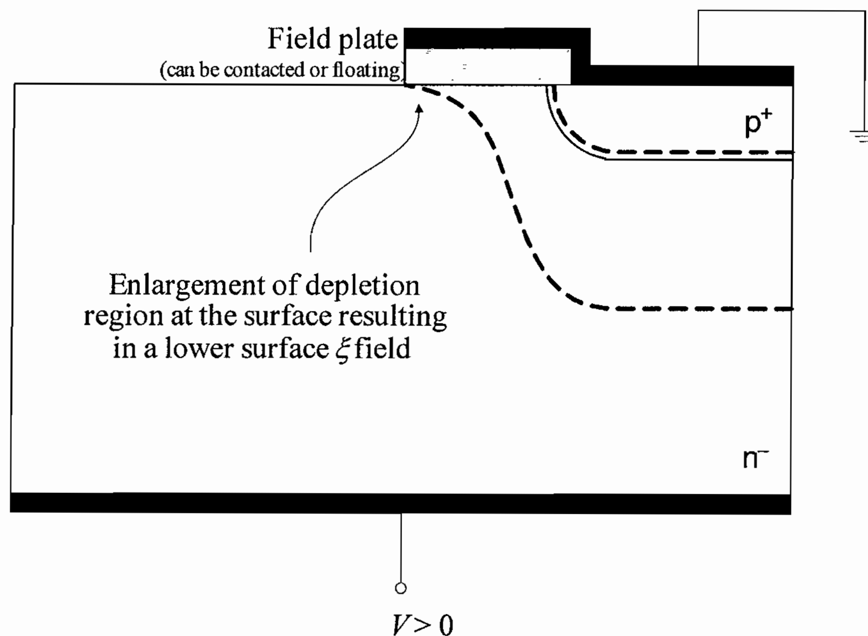
Curvature effect

The shape of the junction which supports the voltage plays an important role in 'field crowding'. The higher the radius of a cylindrical or spherical junction the closer the breakdown is to that of an ideal parallel-plane junction. However, in most microelectronics processes the junction depth is limited to a couple of microns up to maximum 10-15 microns. The curvature effect can be reduced in multiple cell power devices such as MOSFETs or IGBTs by placing the cells (with multiple junctions) close together to simulate almost a 'continuous junction'. By solving Poisson equation for a cylindrical junction one can show that the maximum electric field for the same reverse voltage applied increases significantly compared to that in a planar junction.

Edge breakdown

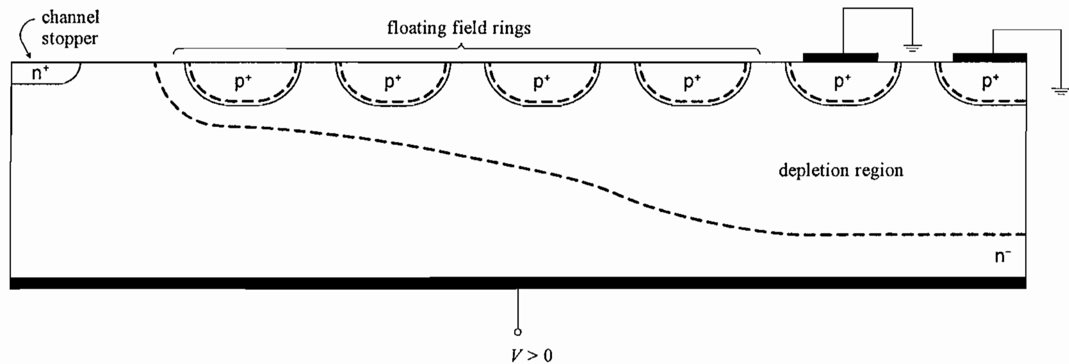
Placing cells very close together has only limited value because at the edge there is always a last cell left 'unprotected'. Premature edge breakdown is a very common effect in power devices. For this special techniques can be used

The field plate technique uses a metal layer as shown below. This results in enhancing the effective radius of the junction.

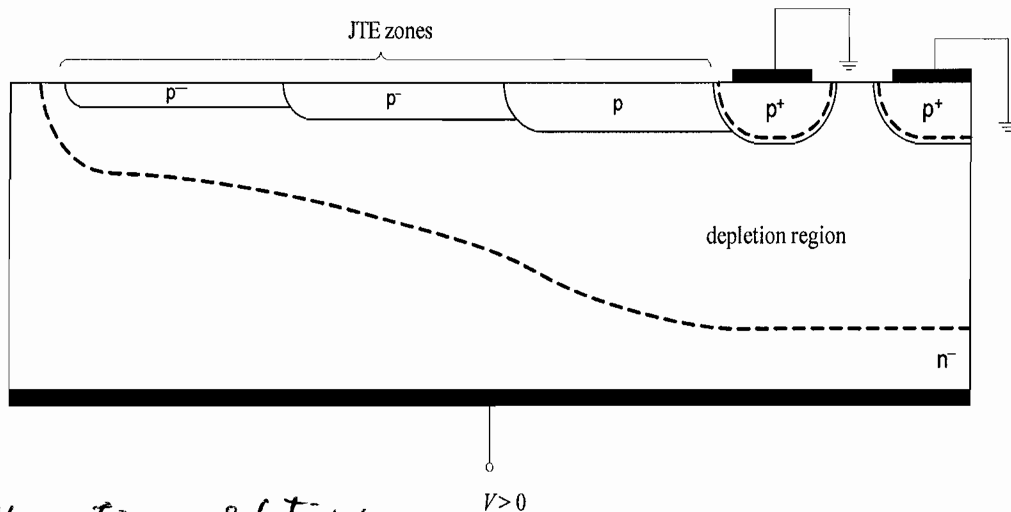


[30%]

An alternative solution is the floating field ring technique. This is based on distributing the field between highly doped p+ floating field rings to alleviate the edge effect.



A similar result can be obtained with the junction termination extension. This is based on having regions of lowly doped p- layers to spread out uniformly the electric field at the edge of the device. The p- layers have to be depleted at breakdown.

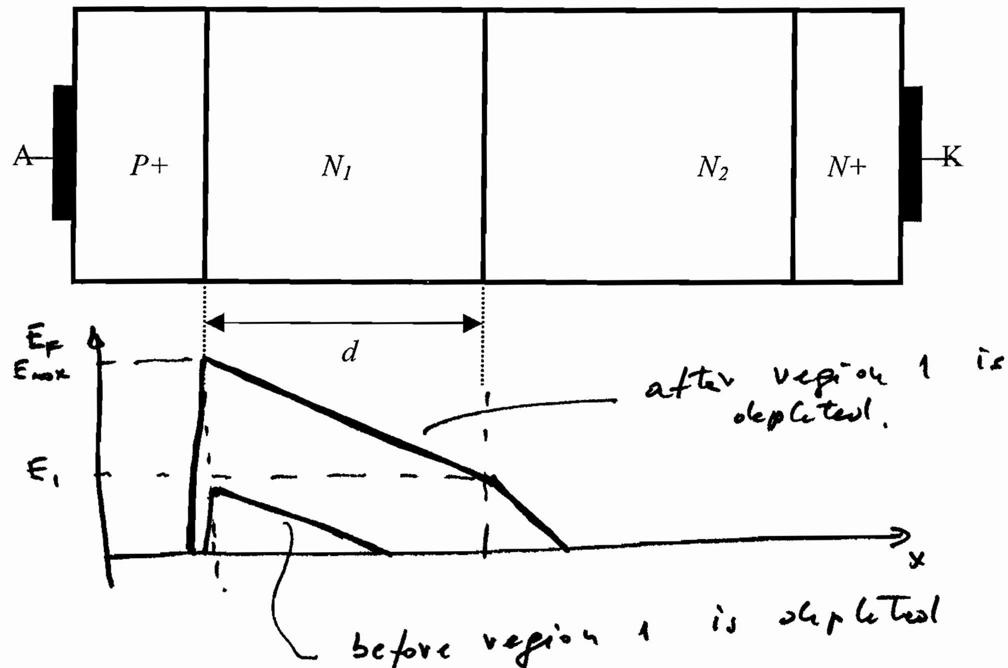


* alternative solutions

The field rings that are closer to the active area have a smaller equivalent radius of a spherical (or cylindrical) junction when compared to the field rings that are farther away from the active area. Therefore to avoid high electric fields next to the active area, the inner rings should have a smaller distance between them. Hence they absorb a smaller voltage between them compared to the outer rings. A good optimisation is when all the electric field peaks between the rings are equal at breakdown so the device theoretically breaks in all points at the same time. This would lead to the maximum efficiency of breakdown per unit area. For this the distance between the rings should be increased gradually from the first ring (the closes to the active cell) to the last ring (the farthest from the active cell).

[20%]

(b).



breakdown occurs when $E_{max} = E_{cr}$

$V_{BR} = V_{PT\ region\ 1} + V_{NPT\ region\ 2}$ (assuming that region 1 gets depleted before breakdown of the diode)

$$V_{BR} = \frac{1}{2}(E_{cr} + E_1)\, d + \frac{\varepsilon_0 \varepsilon_r E_1^2}{2 q N_2}$$

$$E_1 = E_{cr} - \frac{q N_1}{\varepsilon_0 \varepsilon_r} d$$

$$\Rightarrow V_{BR} = E_{cr}\, d - \frac{q N_1}{2 \varepsilon_0 \varepsilon_r} d^2 + \left(E_{cr} - \frac{q N_1 d}{\varepsilon_0 \varepsilon_r}\right)^2 \frac{\varepsilon_0 \varepsilon_r}{2 q N_2}$$

$$V_{BR} = \underbrace{\frac{E_{cr}^2 \varepsilon_0 \varepsilon_r}{2 q N_2}}_{①} + \underbrace{d\left(1 - \frac{N_1}{N_2}\right)\left(E_{cr} - \frac{q N_1}{2 \varepsilon_0 \varepsilon_r} d\right)}_{②}$$

[30%]

(ii) if $N_1 = N_2$ ② $= 0$ $\Rightarrow$

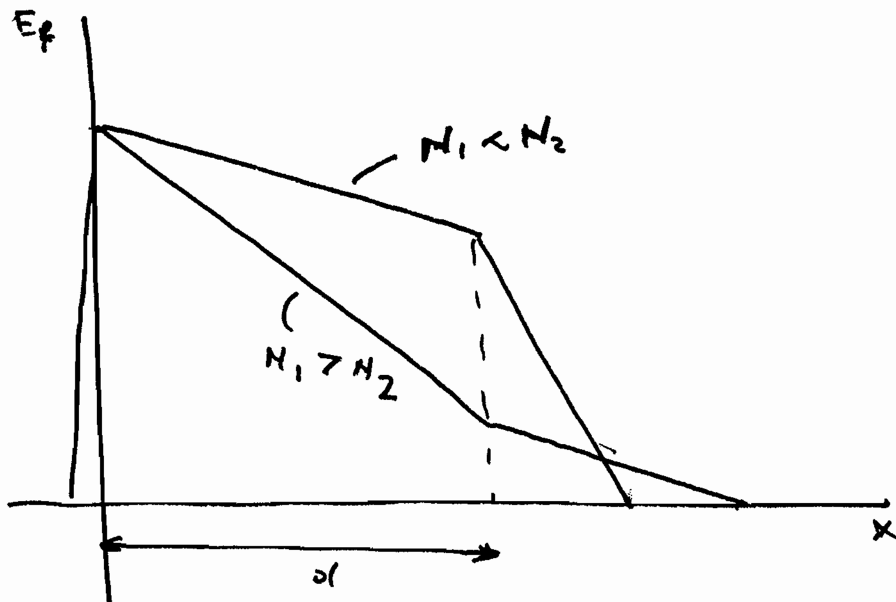
$$\Rightarrow V_{BR} = \frac{E_{cv}^2 \varepsilon_0 \varepsilon_r}{2 q N_2}$$ (just as in 1-D NPT diodes)

if $N_1 > N_2$

$\Rightarrow$ ② is negative $\Rightarrow$ V_{BR} decreases

if $N_1 < N_2$

② is positive ⇒ V_{BR} increases

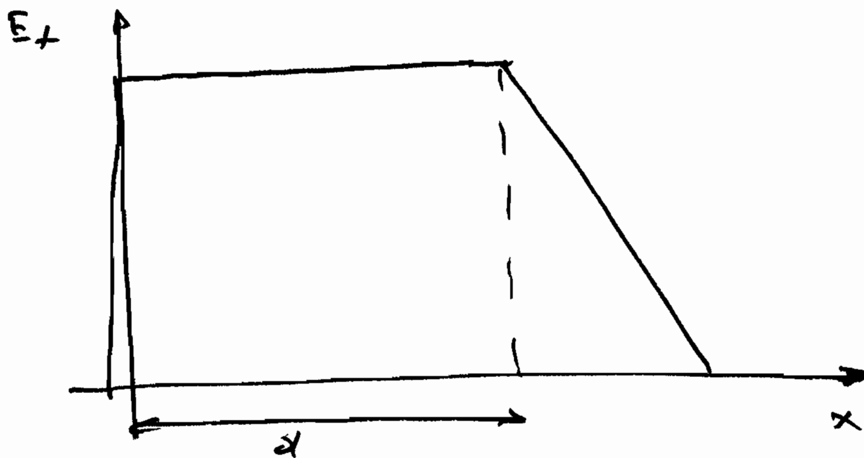


[10%]

(iii) ② is maximum when $N_1 = 0$

In reality N_1 is equal to $n_i \simeq 10^{10}\ cm^{-3}$

for this $E_{AR} = E_{cr}\, d + \dfrac{E_{cr}^2\, \varepsilon_0 \varepsilon_r}{2 q N_2}$



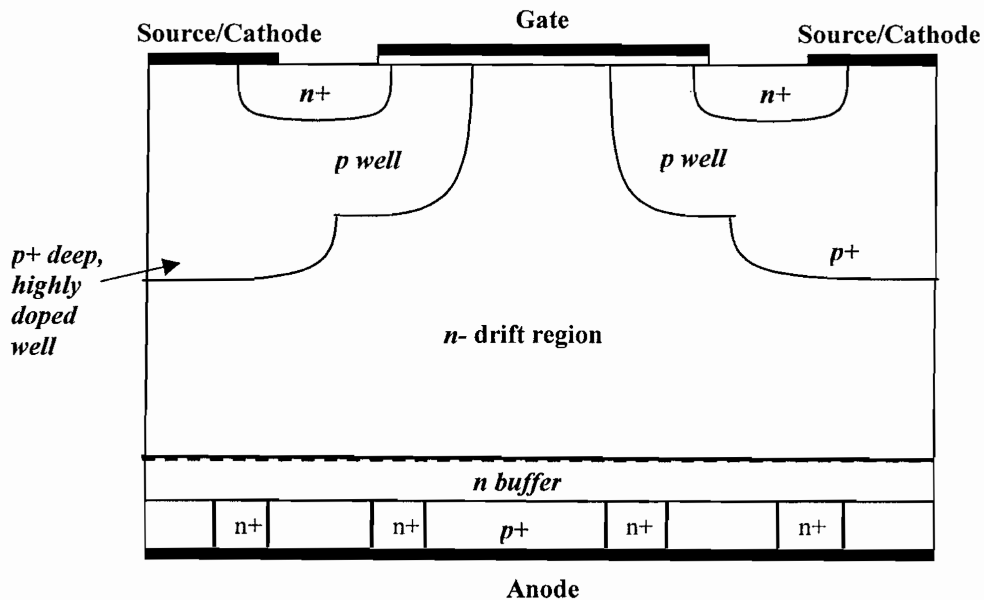
[10%]

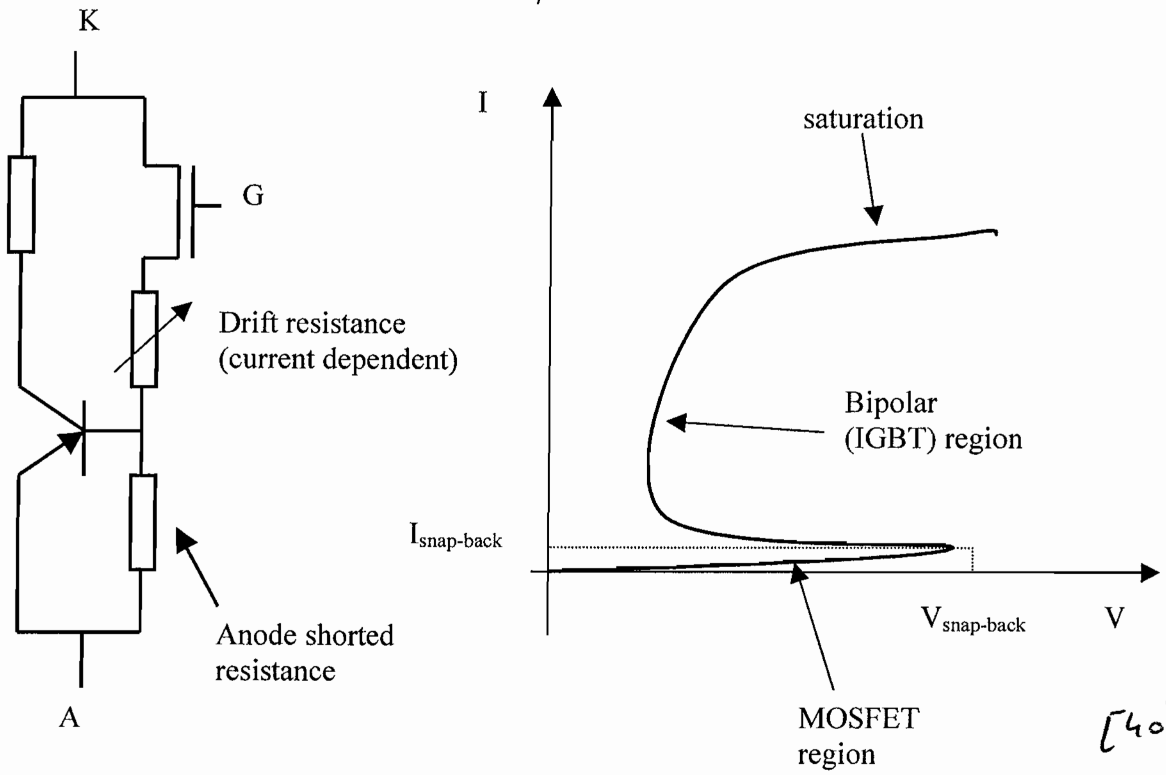
3. The bipolar transistor in saturation has both the base-emitter and base-collector junctions forward-biased. For a power BJT, the collector is wide and in saturation is completely filled with plasma. Hard saturation occurs when the plasma reaches the n+ contact of the collector and deep saturation happens when the plasma level at the n+ side of the collector region raises well above the doping level. In bipolar devices we speak about voltage saturation !

In MOSFET we speak about current saturation. This is due to the pinch-off of the MOS channel and as a result the electron velocity saturates in the channel resulting in a flat current. Therefore the meaning of saturation in MOSFETs and Bipolar is completely different. In switch mode electronics, the bipolar devices are operated in saturation while the MOSFETs are operated in the linear region.

[30%]

(b)





[40%]

(ii) Initially the current is formed of electrons only and flows solely through the channel - drift region and the anod shorted resistance.

The condition for transition from unipolar (MOSFET type conduction) to bipolar conduction is

$$I_{snapback} \cdot R_S = 0.7\,V$$

$$\Rightarrow \underline{I_{snapback}} = \frac{0.7}{10} = \underline{70\,mA}$$

$$\underline{V_{snapback}} = (\underbrace{R_{ch} + R_{acc}}_{50\,\Omega} + \underbrace{R_d + R_{spr}}_{20\,\Omega})\, I_{snapback} + 0.7\,V =$$

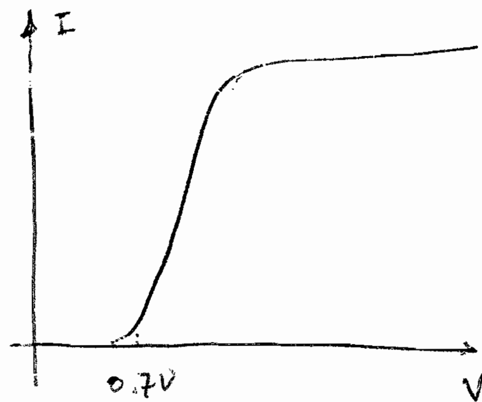
$$= 70 \cdot 0.07 + 0.7 = \underline{5.6\,V}$$

* The voltage drop on the MOS channel at the snapback current is $1.4\,V \ll V_G - V_T = 10\,V$ which justify that the MOS channel is in the linear region.

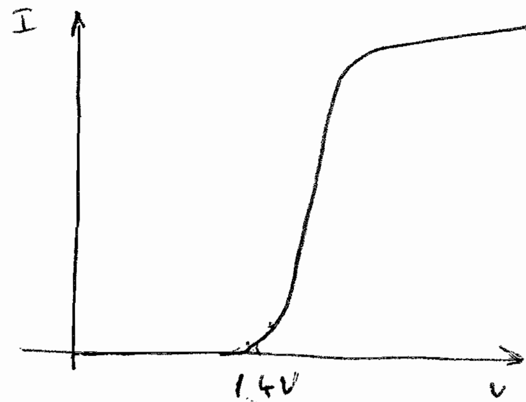
[30%]

4. (a) Reducing the buffer layer doping can potentially lead to punch-through breakdown as this layer is relatively thin. The buffer layer should still be at least one order or in many cases two orders of magnitude greater than the drift region doping. Also reducing the buffer layer leads to higher injection efficiency (approaching 1) which leads to heavy injection of holes and as a result high level of plasma in the drift region, with a pronounced peak at the anode side of the drift region. This leads to better on-state but very low speed and high switching losses. Modern PT IGBTs are made with a moderately doped buffer layer to stop the punch-through and at the same time lower slightly the injection efficiency to obtain a favourable trade-off between on-state performance and switching losses. [20%]

(b) These are two LIGBT type structures. The structure (a) is based on two pnp transistors in parallel (one with wide collector and one with wide base). The MOSFET serves as the base current for both transistors. In general the wide collector (narrow base) transistor has a higher gain and could take more current than the wide base transistor. This structure is quite common in junction-isolation technology where the drift region plays the role of the wide base in one of the transistors and the p-substrate plays the role of the wide collector in the other transistor. The structure (b) is based on a electron MOS current driving the base of a Darlington pair of pnp transistors. The gain of the pnp transistor is slightly enhanced by the Darlington configuration but the effective base-emitter voltage is double compared to a single device. For this reason the on-state losses are quite high without offering any significant advantage. The I-V characteristics are shown below (not the differences in the shift voltage in the on-state)

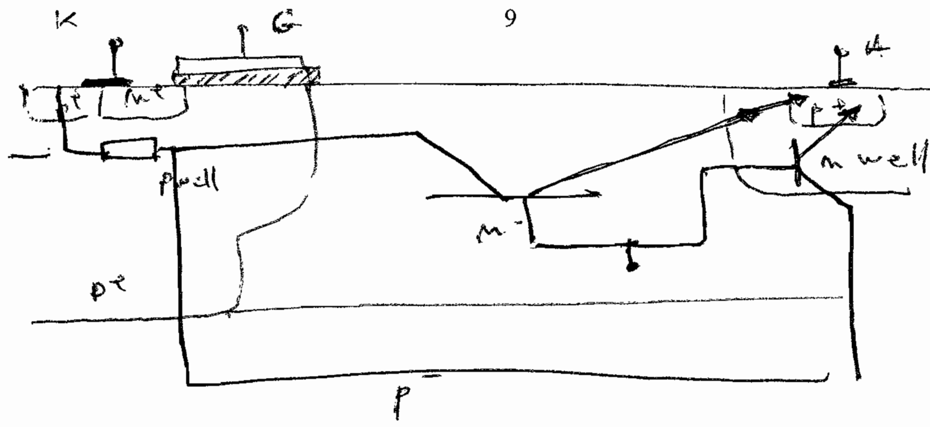


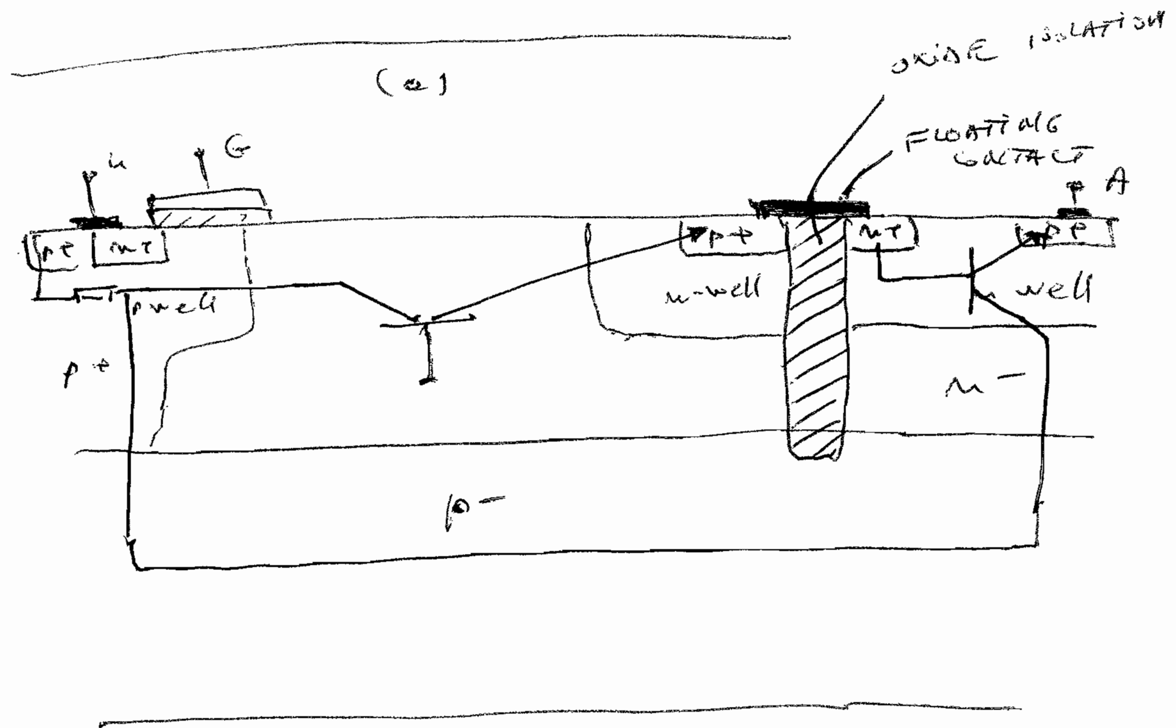
(a)



(b)

[30%]



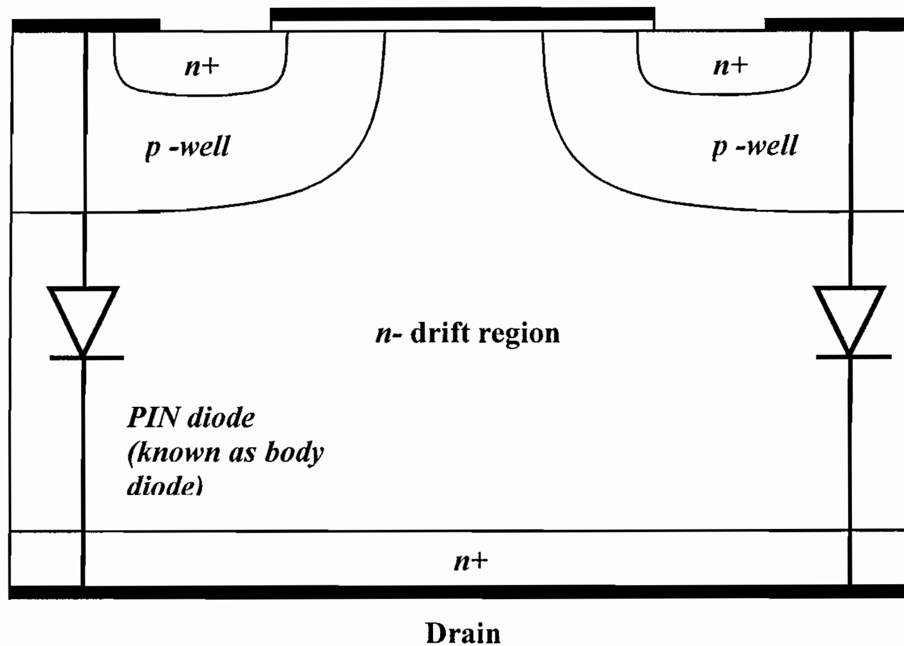


[30%]

The SOI LIGBT has only one wide base transistor (as the buried insulator stops an injection of plasma into the substrate). As result the SOI LIGBT accumulates plasma only in the drift region and not in the substrate. Thus, the SOI LIGBT is going to be very significantly faster and there will be no isolation problems as there is no plasma moving freely through the substrate. The structure (a) is going to have better on-state but at the expense of very slow speed and isolation problems when used with CMOS cells. Structure (b) has an additional 0.7 V (in total 1.4 V) drop across the base-emitter junction (due to the Darlington configuration) while not offering any other significant advantage. It still has very slow speed and isolation problems when compared to an SOI structure. Therefore in spite of being novel, it has little use. Note that the Draligton configuration in low power transistors was a mean to increase the collector/base small-signal current gain Here it has little use in device that is intended to be used as a switch.

[20%]

5. The body diode, comprising the p-well short as the anode, the n- region as the thick drift layer and the n+ drain as the cathode, is used to withstand high voltages when the device is off (in the blocking mode). The diode is based on a NPT junction design (see previous lecture). Interestingly, the diode may also be operated in the on-state when the potential at the source is greater than the potential at the drain (the gate is shorted to the source and the MOS component is inactive).



6. The IGBT has a pnp bipolar transistor structure in place of the body diode. This bipolar transistor is in anti-parallel configuration with the IGBT. The anti-parallel bipolar transistor has the p-well as the emitter, the n-drift region as the base and the p+ as the collector. We can incorporate the diode in an IGBT by designing an anode-shorted IGBT whereby the anode layer is made of shortcircuited layers of p+ and n+. (see picture below). The disadvantage is that this creates a snap-back for the IGBT as the anode junction will need to become forward-biased for the device to operate in a bipolar (IGBT mode). Therefore the performance of such IGBT will be inferior to a standard IGBT due to the undesirable snap-back present in its I-V static characteristics. Nevertheless careful optimisation of the p+/n+ ratio can be carried out to improve the trade-off between the IGBT vs diode performance.

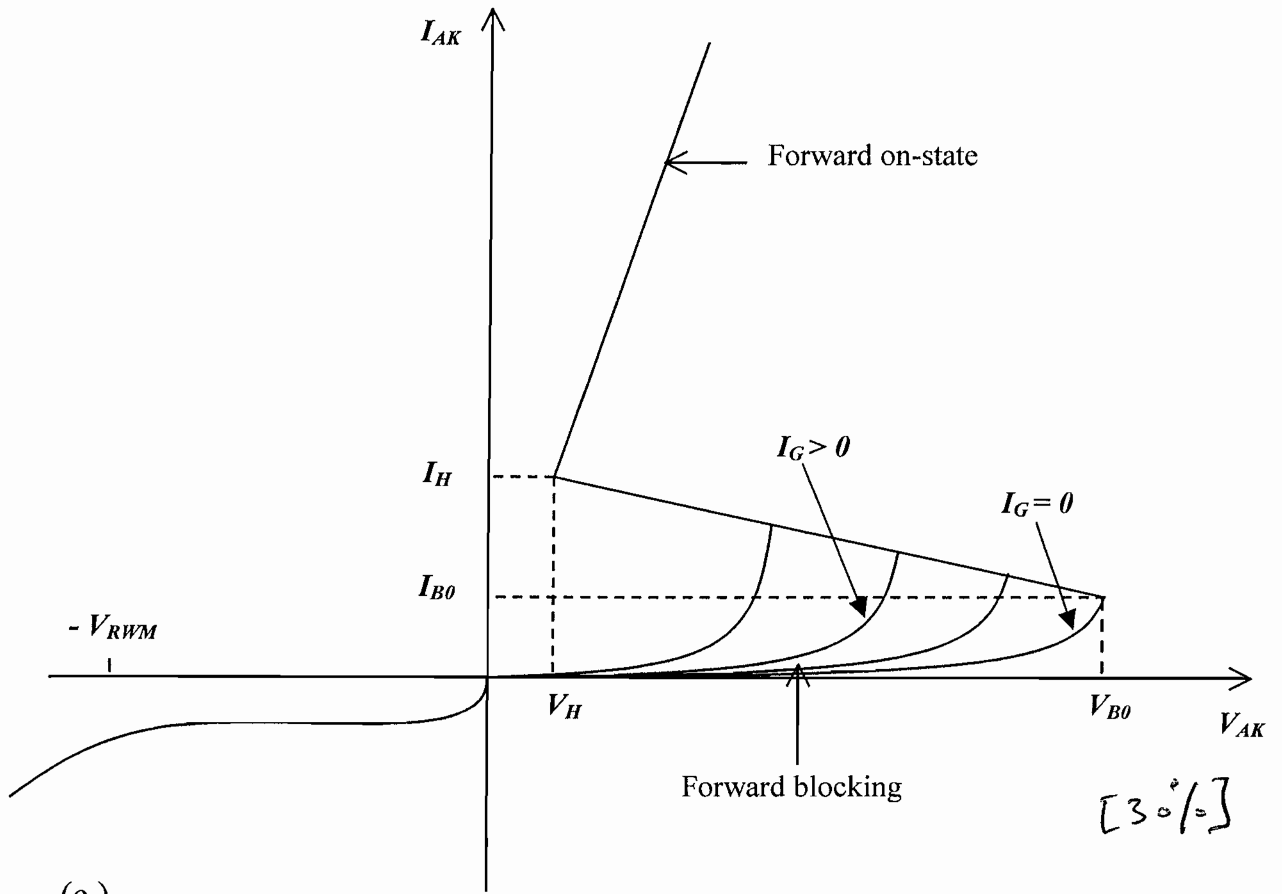
Gate
Cathode
Cathode
n+
n+
p -well
p -well
n- **drift region**
PIN diode (known as body diode)
n+
p+
n+
Anode

b) **Symmetrical thyristors (NPT)** have both forward and reverse blocking capability. In the forward blocking state the anode is biased positive with respect to the cathode while in the reverse blocking state the anode is biased negative with respect to the cathode. Symmetrical thyristors are based on a NPT junction design. For this reason the drift layer of symmetrical thyristors is very thick (larger than the maximum extension of the depletion region) and its losses, both in on-state and transient, tend to be relatively high. The device has however reverse-blocking capability which can be of use in special power electronic circuits. In addition, these devices can be turned-off by reverse biasing the voltage between anode and cathode. Classical thyristors use most commonly this design.

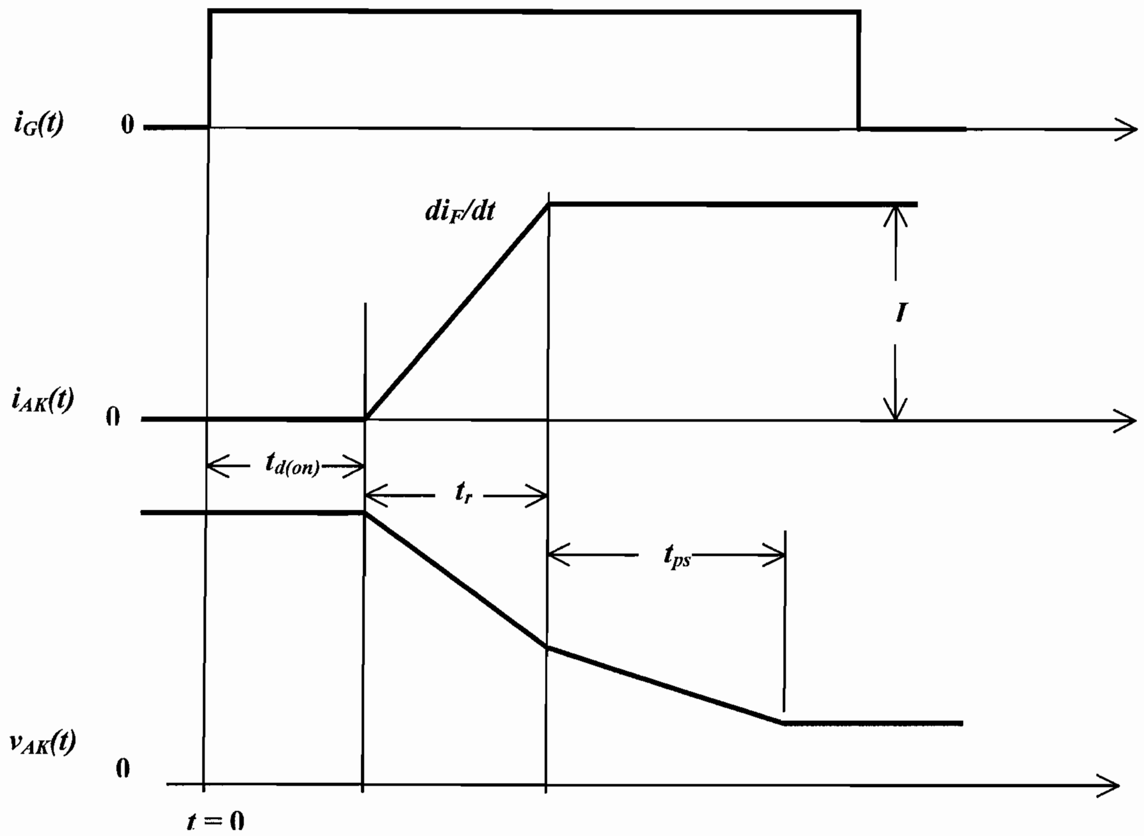
Aymmetrical thyristors (PT) have only forward blocking capability. They are based on a PT junction design and they feature a buffer between the n- drift region and the p-anode to make sure that no punch-through breakdown occurs. The lowly doped drift region is however fully depleted at breakdown. When compared to the symmetrical thrristors, the asymmetrical thyristors have thinner n- drift region and therefore reduced on-state and transient losses. Because they do not offer reverse blocking capability, they cannot be turned-off by reversing the anode-cathode voltage. For this reason most of the asymmetrical thyristors are GTOs or GCTs where the turn-off is accomplished via the gate.

The I-V characteristics of a symmetrical thyristor are shown next page

- V_{RWM} - reverse blocking breakdown
- V_{B0} – the breakover voltage (the forward-blocking breakdown).
- I_{Bo} – the breakover current. This is the maximum leakage current (when gate is inactive) before the device turns-on.
- V_H – the holding voltage . This is the minimum on-state voltage in the device (>0.7 V)
- I_H – the holding current. This is the minimum current that flows through the thyritor and still maintain an on-state operation.
- I_G – the gate current injected in the device to facilitate turn-on of the thyristor (latching of the thyristor).



(c)



- ***di_F/dt*** is dictated by the external circuit.
- ***$t_{d(on)}$*** is the delay time. In this period the thyristor continues to block the voltage. Holes injected from the gate start to accumulate in the p base. $\alpha_1 + \alpha_2$ approaches 1. The thyristor is reaching the breakover point.
- ***t_r*** is the risetime. During this interval a large excess of carrier charge (plasma) is formed in the vicinity of the gates[1]. At the end of this phase the current reaches the full steady-state on-state level but the voltage needs to decrease further.
- ***t_{ps}*** is the time taken for the plasma to spread laterally across the face of the cathode until the entire cross-sectional area of the thyristor is filled with plasma. The voltage on the drift during this phase decreases further until it reaches its on-state level.

[1] This is the region where the emitter junction of the npn transitor is fully forward biased (0.7 V). The further the distance from the gate the less forward-biased the emitter junction is and thereby the weaker the thyristor action.