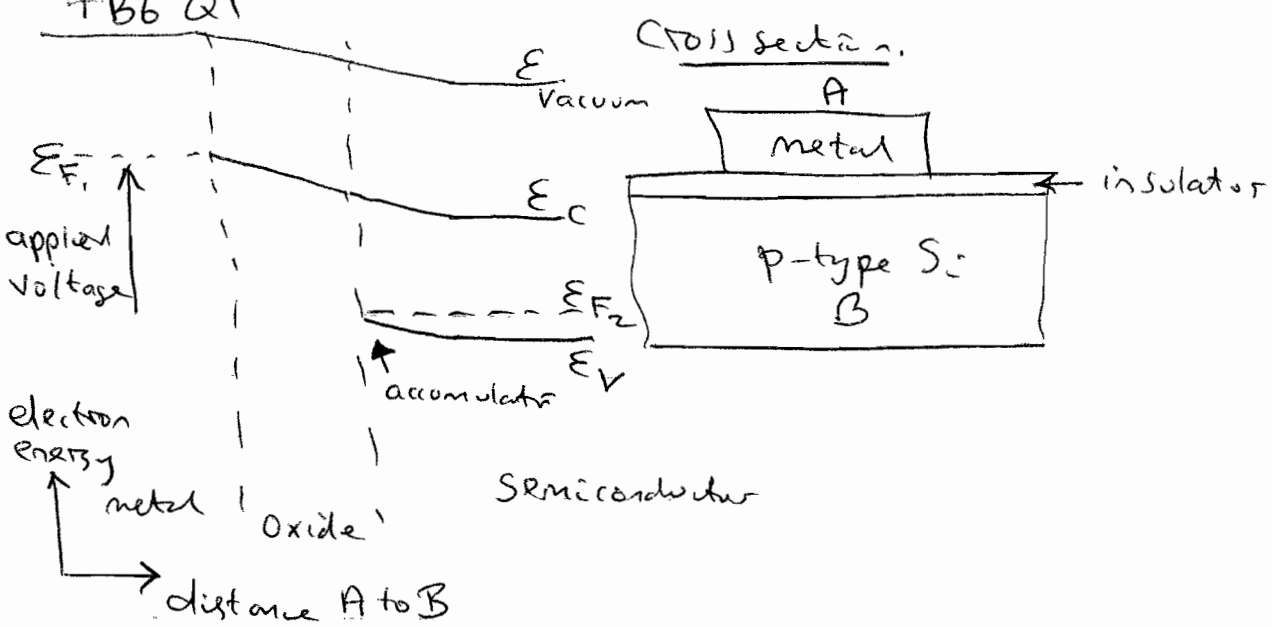
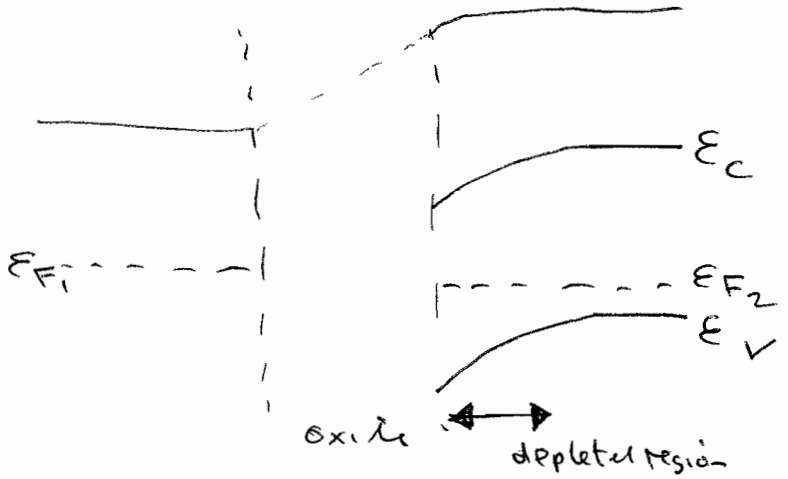
4B6 Q1



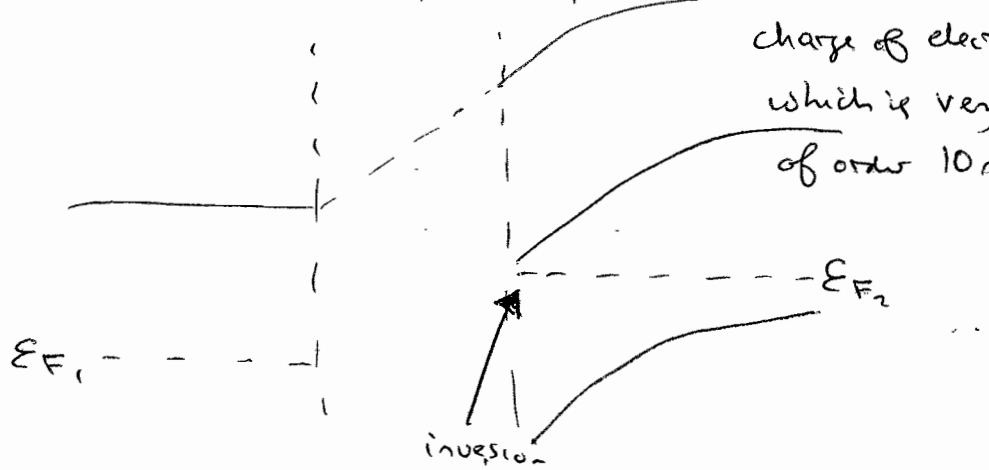
Accumulation of majority carriers (holes) occurs at the semiconductor/oxide interface in a layer $\lesssim 100$ nm thick when a negative potential is applied to the metal relative to the semiconductor

hole concentration $p = N_v \exp -\left(\frac{\mathcal{E}_F - \mathcal{E}_v}{kT}\right)$

Depletion of holes happens when a positive potential (repulsive) is applied to the metal and the thickness of the depleted layer is typically a fraction of a μm

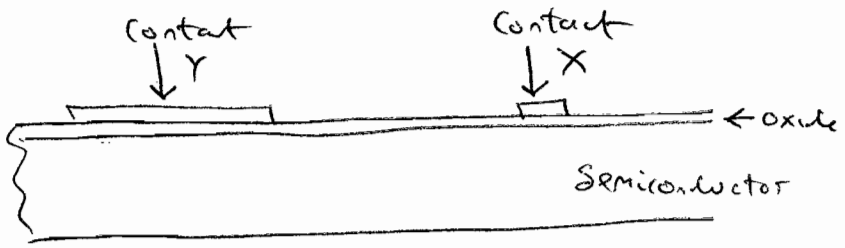


Further increases in the positive potential on the metal leads to an inversion charge of electrons $n = N_c \exp -\left(\frac{\mathcal{E}_c - \mathcal{E}_F}{kT}\right)$ which is very thin of order 10 nm in typical Si devices.



4B6Q1 (cont.)

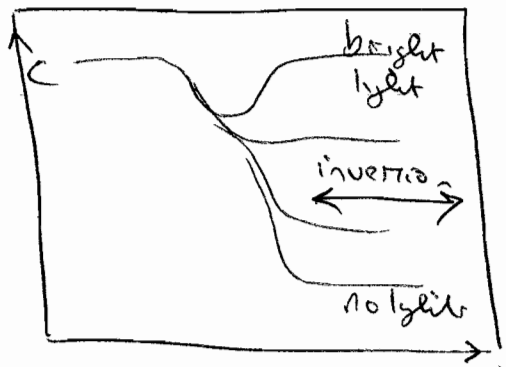
Measurement cross sectional set up.



By electrically probing the wafer with the contact X to a metal pad of known area and a second contact Y to a much larger area of metal the MIS structure under X can be biased into depletion to sweep carriers out of the semiconductor and measure the doping impurity density, or biased into accumulation when a capacitance measurement reveals the electrical properties of just the insulator.

In an ac measurement the drive voltage must be on a substantially smaller scale than any structures which are to be observed in the C-V curve to avoid washing out the required data.

With light producing many electron-hole pairs which can separate to form the necessary charges in the inversion charge density during the ac measurement cycle the capacitance is high in inversion. In lower light the capacitance is lower.



The semiconductor is p-type because a +ve gate voltage gives inversion. At negative gate (metal) voltage in accumulation there no significant light dependency because the semiconductor achieves equilibrium at all times. Similarly there is only an ac measurement frequency dependence in inversion/depletion

Calculate the oxide thickness from the capacitance in accumulation.

$$d_{oxide} = \frac{A \varepsilon_0 \varepsilon_{ox}}{C_{maximum}} = \frac{3\times10^{-8} \times 8.9\times10^{-12} \times 6}{28\times10^{-12}} = 5.4\times10^{-8}\ m$$

For the case of inversion at high illumination.

$$\frac{1}{C_{minimum}} = \frac{1}{C_{semiconductor}} + \frac{1}{C_{oxide}}$$

$$\frac{1}{5\times10^{-12}} = \frac{1}{C_{semiconductor}} + \frac{1}{28\times10^{-12}} \quad \therefore C_{semi} = 6.1\times10^{-12}\ F$$

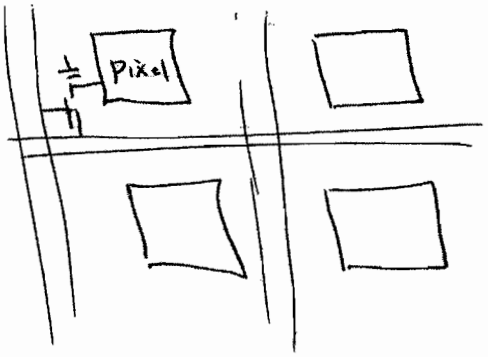
$$d_{depletion} = \frac{A \varepsilon_0 \varepsilon_{semi}}{C_{semi}} = \frac{3\times10^{-8} \times 8.9\times10^{-12} \times 10}{6.1\times10^{-12}} = 4.4\times10^{-7}\ m$$

With pulsed dc bias applied deep depletion could be achieved at lower C

4B6 Q2 a) A projection display must be bright with good contrast. In the case of presentation displays the resolution is very important whereas the speed requirements on the display are more severe in the cases of tv or movies.

thin film transistor driven liquid crystal display devices are widely used for professional projection displays.

each pixel element is driven by an x-y addressing system of thin film transistor

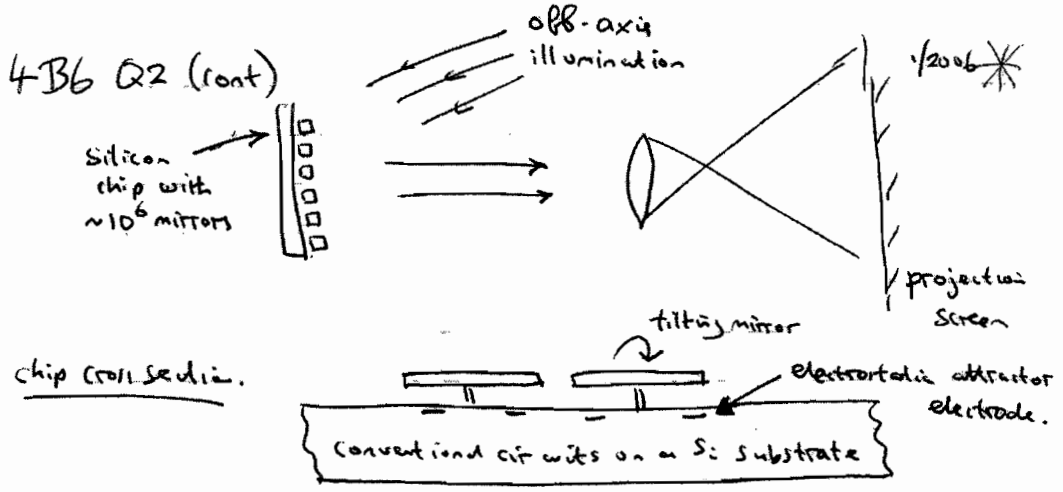


the performance is good but limited in speed by the liquid crystal switching time (a few milliseconds) and limited in power handling capability by the power absorbed by the liquid crystal.

digital micromirror displays are very fast since the mechanical switching time of the tilting mirror is a few tens of microseconds, and the power handling capability is excellent because the mirrors are highly reflecting (~90%) at all times since in the "off" pixels the light is also reflected but simply not directed along the optic axis.

The cost of both of the above technologies is greatly increased for higher resolution displays because they rely on direct x-y addressing on a silicon chip at an electrical storage device (transistor or capacitor) at each pixel location to hold the image information between refreshes.

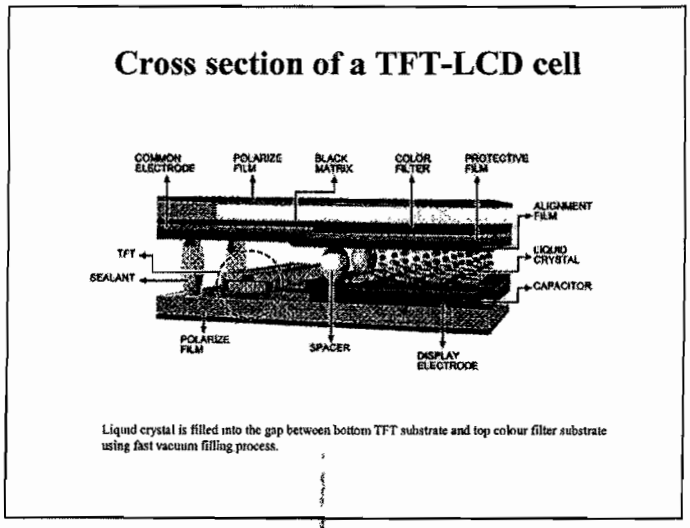
b)



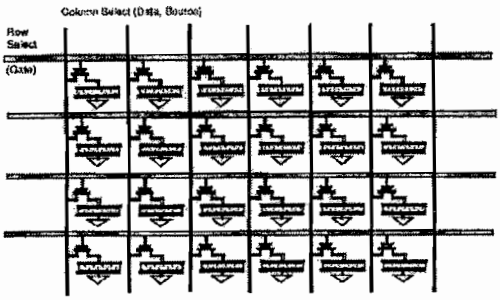
After Silicon IC circuit fabrication

(1) a sacrificial layer such as polyimide is spun onto the wafer
(2) the mechanical layer (e.g. Silicon Nitride) followed by the reflector layer (e.g. aluminium) are deposited and patterned.
(3) the sacrificial layer is removed leaving a structure which can flex.
(4) proprietary lubricants are introduced to reduce the possibility of stiction.
(5) the device is encapsulated for protection against dust and water vapour.

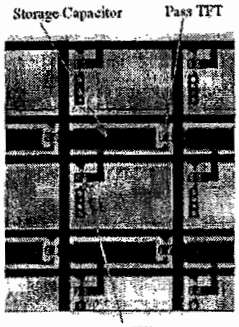
c)



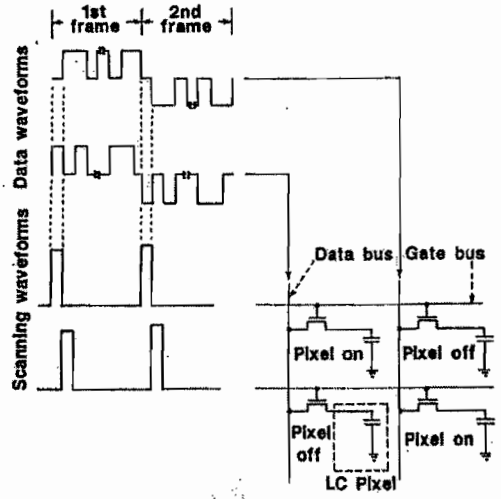
Active matrix TFT-LCD



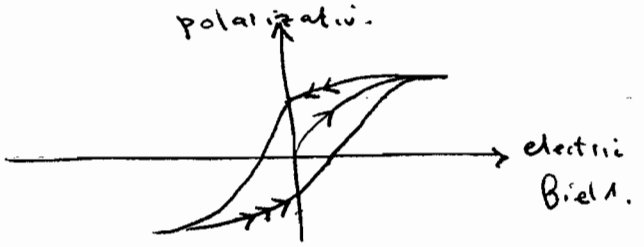
As liquid crystal material is of dielectric nature, each LCD cell has the property of a capacitor under external bias.

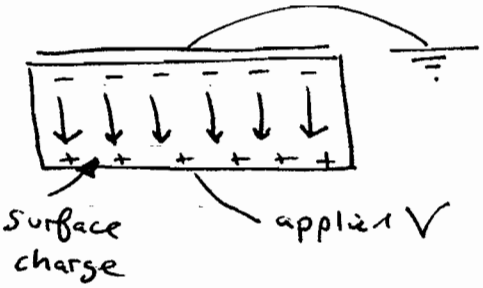


Driving AM-LCD



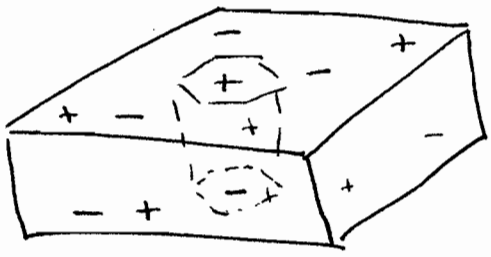
4B6 Q3 Polarization in a ferroelectric material the polarization is the alignment of the electric dipoles which is accomplished by applying an external electric field.



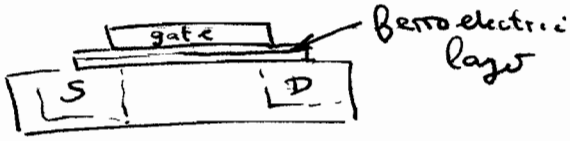


domains result when a macroscopic sized sample of ferroelectric material is not uniformly polarized but broken up into domains of opposite polarization thereby lowering the total electrostatic energy

the application of a sufficiently strong external electric field would nevertheless align the domains

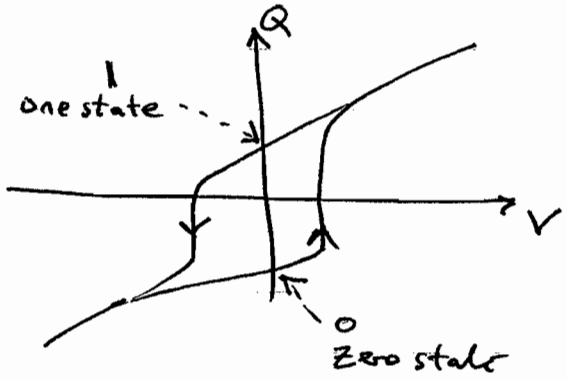


non-volatile memory cells are constructed by putting thin film of ferroelectric material under the gate electrode of an FET



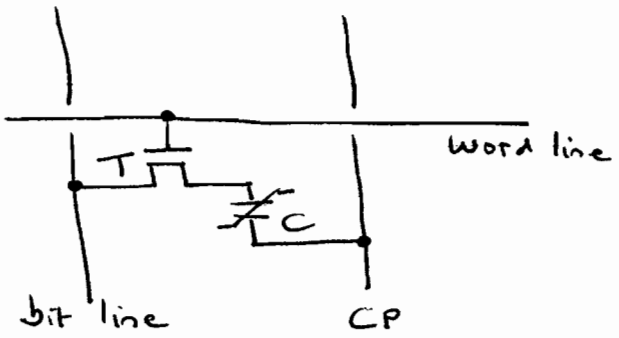
In the charge approach to device readout $\Delta Q = A \Delta P$

In the field approach to device readout $E \sim P$

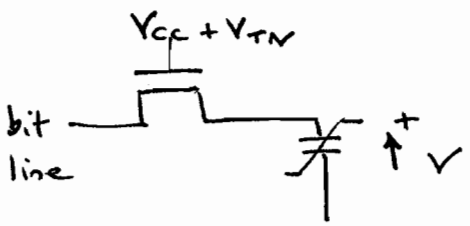


4B6 Q3 (cont)

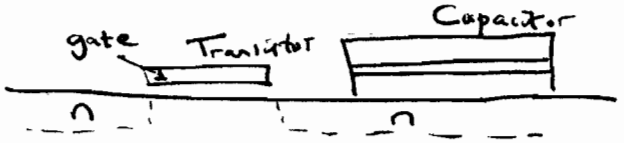
1 transistor/1 capacitor memory cell



write operation



Cross section



With reference to figure 2

A labels the doped n-type regions forming the source and drain regions in the p-type Si and one electrode of the ferroelectric capacitor

B is a diffusion barrier such as Pt/Ti necessary to avoid chemical interactions between the ferroelectric materials and the Si

C is the top electrode of the ferroelectric capacitor

D is an insulator layer which also provides a hermetic seal against atmospheric corrosion

ferro electric memory is becoming widespread for low power portable applications.

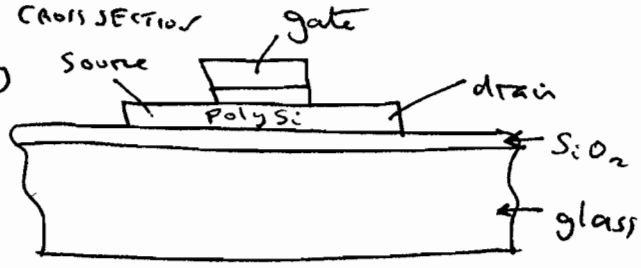
devices are made with a stacked geometry and 0.18 μm minimum linewidth

lower voltage operation would be desirable which would necessitate the use of reduced thickness ferroelectric layers and the corresponding challenge of keeping leakage currents manageably low to maintain reliable operation.

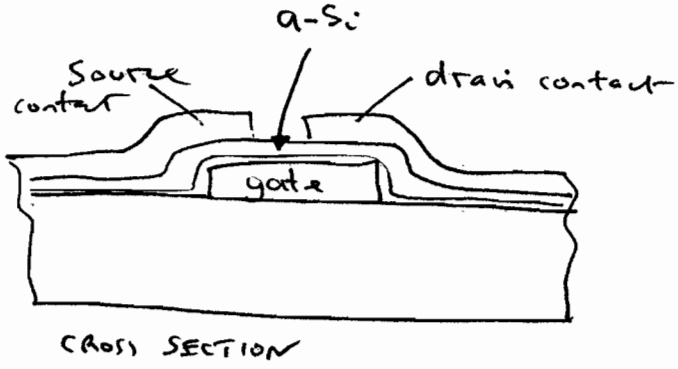
reliability is an outstanding issue because of diffusing hydrogen (even at room temperature) and the interface states have to be controlled.

4B6 Q4 (i) single crystal silicon based MOS transistors have high carrier mobility in the channel and the thermally grown SiO_2 gate insulator gives few interface states and excellent transistor characteristics.

(ii) Poly crystalline silicon deposited by chemical vapour deposition (CVD) on a glass substrate is made into thin film transistor with electrical characteristics which are good enough to use in decoding circuits at pixel drivers in LCD applications despite the lower channel mobility than single crystall Si. The advantage of the technology is that relatively cheap substrates such as glass can be used when a buffer layer of SiO_2 is deposited on them prior to CVD poly silicon.



(iii) amorphous silicon thin film transistor are typically made by first depositing and patterning the gate electrode,



and then an insulator such as SiN followed by the channel material amorphous silicon which is a low cost low temperature process giving low mobility devices but with sufficient performance to incorporate into liquid crystal display devices.

4B6 Q4 (cont.)

Fabrication of a-Si TFT

clean the substrate
deposit gate metal
apply photoresist + mask
wet etch metal

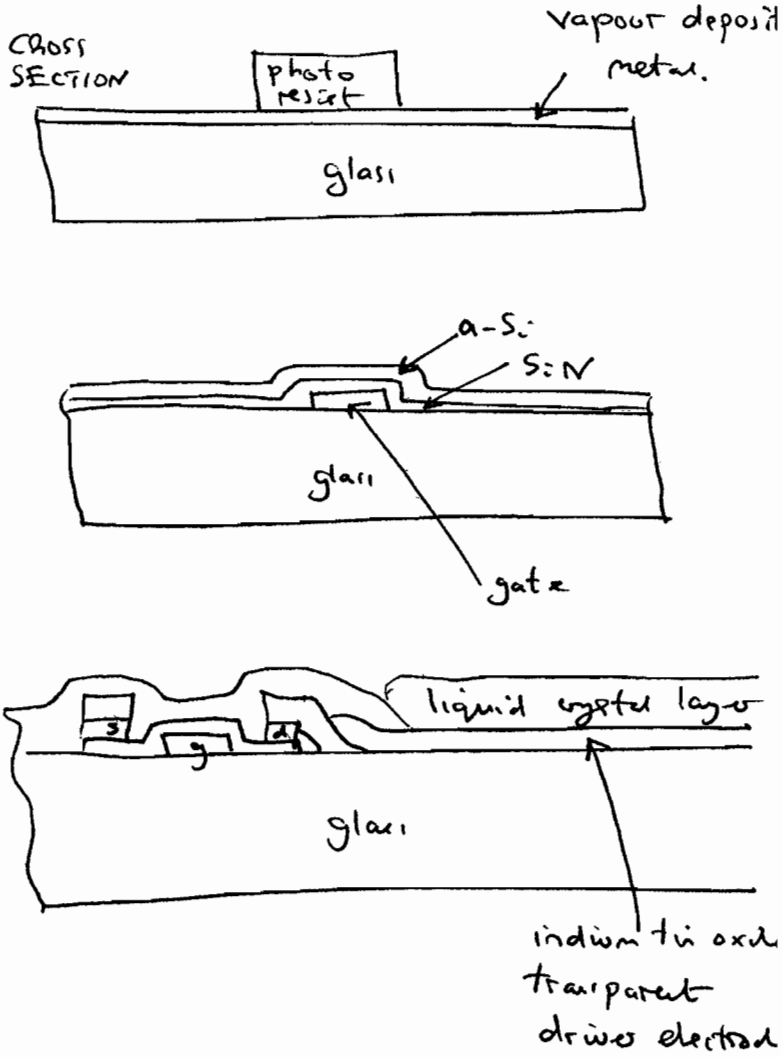
deposit Si_3N_4 gate dielectric

deposit a-Si

apply photoresist + mask
etch electrode structures

deposit contacts
pattern them
deposit insulator

apply liquid crystal material.

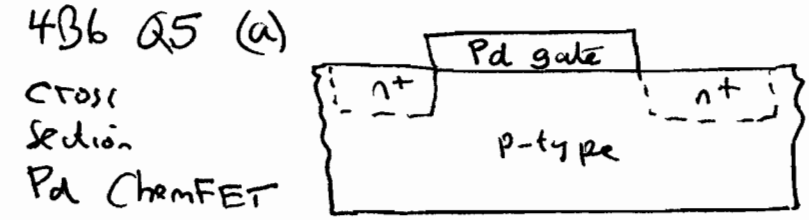


The important steps determining the transistor performance and the device yield are the gate insulator deposition and interface to the deposited a-Si channel layer.

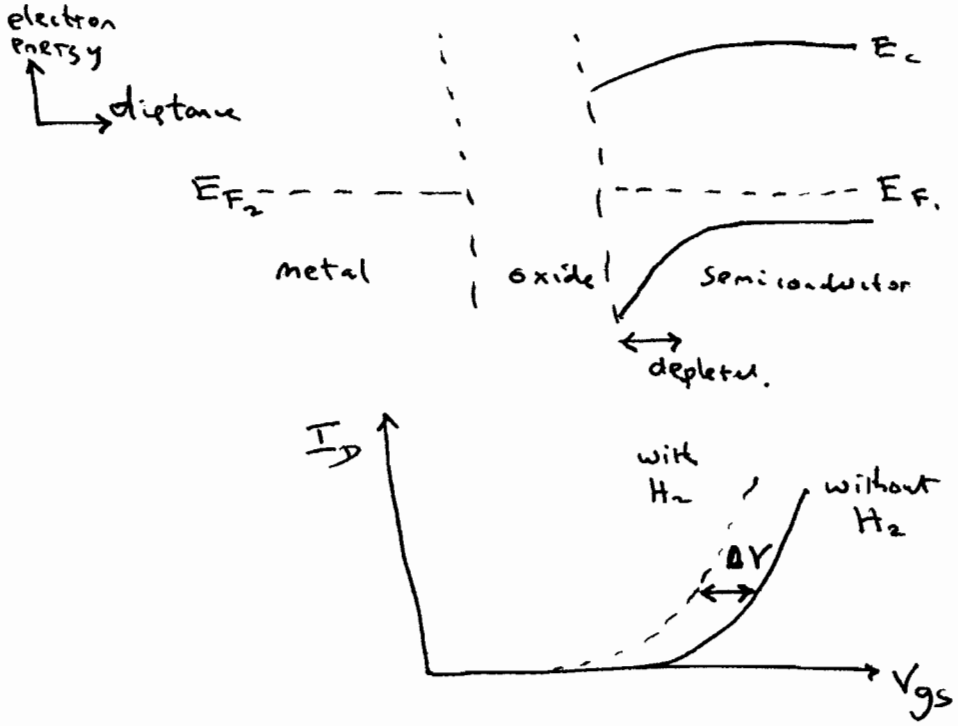
The final encapsulation steps are important to achieve high yield and long term reliability avoiding effects of water vapour and the atmosphere.

The range of applications of polycrystalline transistors is increasing as technology is developed to deposit poly-Si at lower temperatures with brief post deposition anneals allowing lower cost substrates to be used, reducing the number of applications of low performance a-Si devices.

4B6 Q5 (a)



Cross Section Pd ChemFET



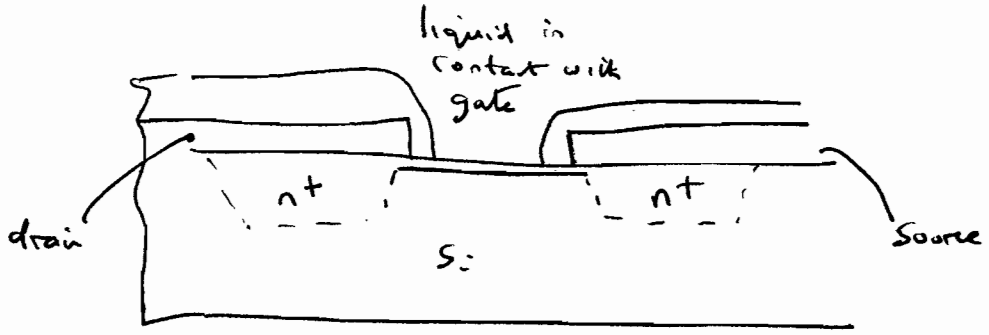
An MOS-based chemical sensor has a gas permeable gate electrode such as palladium. The presence of hydrogen diffusing through the gate and reaching the oxide interface results in a change in the metal work function and hence the threshold voltage in the MOS current voltage characteristic.

(b) In a biosensor a bioreceptor is immobilized on a compatible transducer for example an ENFET (enzyme field effect transistor) with glucose oxidase would be a glucose sensor.

Glucose oxidase promotes the reaction of sucrose with oxygen with the by products hydrogen peroxide and gluconolactone which hydrolyses with water forming gluconic acid.
The presence of acid in contact with the gate of the FET results in a threshold shift which is detected by measuring the transistor characteristics

4B6 Q5 (cont.)

K



In figure 3 I is a relatively conventional Si substrate
II are the doped source and doped drain regions (usually n type with a p type substrate)
III is an insulator such as SiN or SiO
IV is a conducting layer making ohmic contacts to the source and drain
V is an insulating layer
VI is the liquid electrolyte which is the transistor gate

In operation the ISFET in figure 3 senses and amplifys changes in the double layer potential due to changes in the pH of the electrolyte. By functionalizing the gate insulator biological molecules of interest can be detected as they bind to the surface.

A or D are the connections to source and drain.
B is the substrate connection (usually connected to the source)
C is the platinum reference electrode which is usually biased to ensure that the channel is inverted.

The detection circuit typically monitors the source-drain current under fixed biasing conditions, thus measuring variations in the threshold as a function of time.

ISFETs are used for sensing K^+, Na^+, Li^+ ions or NH_4^+ ions, etc.