1.

a) The input offset voltage, $V_{io}$, is the voltage measured at the output of the amplifier when inputs are connected to ground. Adding at the input voltage source forcing the output voltage to zero is defined as input offset voltage which is proportional to an amplifier gain. The input offset voltage is temperature dependant.

Input bias current, $i_b$, is the average of the current to the two input terminals when the input voltage is zero. For bipolar op-amplifier this is base bias current required by circuit. For amplifiers with FET input amplifiers this is leakage current through reverse diode and for MOS inputs leakage through the gate insulator. The input bias current is temperature dependent. [20%]

b) From the data sheet input offset voltage at $25^0$C and input bias current are defined as follows:

$V_{io} = 10\ \mu V$ and $i_b = 5$ nA.

Output voltage $V_0$ is defined as follows:

$V_0 = A * ( V_+ - V_- + i_{b+} * R_2 - i_{b-} * R_1 + V_{io} )$

$R_1 = R_2$ and $V_+ = V_- = 0$

$V_0 = A * V_{io}$

$V_0 = 20 * 10\ \mu V$

$V_0 = 200\ \mu V$ ( at $+25^0$C)

From data sheet average input offset drift is defined as follows:

$\alpha = 0.2\ \mu V/^0C$

Voltage output for $+80^0$C will be:

$\Delta t = 80 - 25 = 55\ ^0C$

$V_{55} = \alpha * \Delta t = 0.2 * 55\ \mu V = 11\ \mu V$

$V_{io/80} = V_{io} + V_{55} = 10\ \mu V + 11\ \mu V = 21\ \mu V$

$V_{0/80} = A * V_{io/80} = 20 * 21\ \mu V = 420\ \mu V$

Voltage output for $-40^0$C will be:

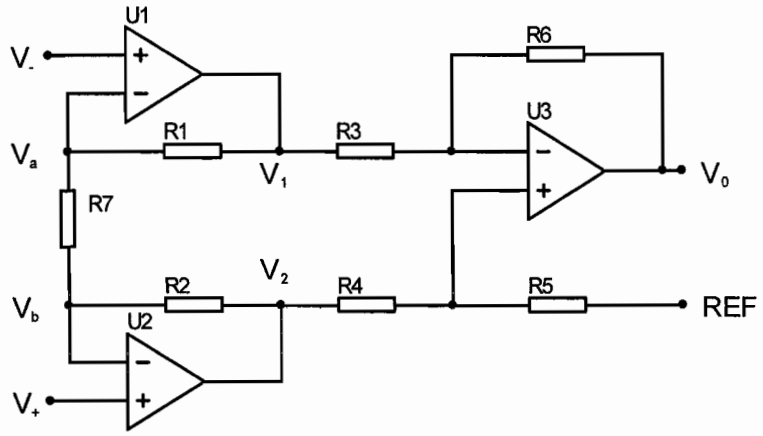
$\Delta t = 25 - (-40) = 65\ ^0C$

$V_{-40} = \alpha * \Delta t = 0.2 * 65 = 13\ \mu V$

$V_{io/-40} = V_{io} - V_{-40} = 10\ \mu V - 13\ \mu V = -3\ \mu V$

$V_{0/-40} = A * V_{io/-40} = 20 * (3)\ \mu V = -60\ \mu V$ [10%]

c) Schematic diagram of the instrumentation amplifier based on three amplifier is as follows.




With REF = 0

$V_1 = V_- * ( 1 + R_1 / R_7 ) - V_b * R_1 / R7$

$V_2 = V_+ * ( 1 + R_2 / R_7 ) - V_a * R_2 / R_7$

As $V_a = V_-$ and $V_b = V_+$

$V_1 = V_- * ( 1 + R_1 / R_7 ) - V_+ * R_1 / R7$

$V_2 = V_+ * ( 1 + R_2 / R_7 ) - V_- * R_2 / R_7$

$V_0 = V_2 * [R_5 / (R_4 + R_5)] * ( 1 + R_6 / R_3 ) - V_1 * R_6 / R_3$

If $R_3 = R_4 = R_5 = R_6 = R$

$V_0 = V_2 - V_1$

$V_0 = V_+ * ( 1 + R_2 / R_7 ) - V_- * R_2 / R_7 - V_- * ( 1 + R_1 / R_7 ) + V_+ * R_1 / R7$

If $R_1 = R_2 = R$

$V_0 = V_+ * ( 1 + R / R_7 ) - V_- * R / R_7 - V_- * ( 1 + R / R_7 ) + V_+ * R / R7$

$V_0 = V_+ * ( 1 + 2 * R / R_7 ) - V_- * ( 1 + 2 * R / R_7 )$

$V_0 = (V_+ - V_-) * (1 + 2 * R / R_7)$

If $R_7 = R_G$ than gain of the amplifier can be controlled from 1 to $A_0$ by changing single value of the resistor $R_G$.

The output voltage $V_0$ can be defined as follows:

$V_0 = V_{CM} * A_{CM} + \Delta V * A_D$

where are:
$V_{CM}$ = Common voltage at $V_+$ and $V_-$
$A_{CM}$ = Common voltage gain
$\Delta V$ = Differential voltage at $V_+$ and $V_-$
$A_D$ = Differential voltage gain

As we would like to define Common Mode Rejection Ratio for the instrumentation amplifier we can assume that both inputs $V_+$ and $V_-$ are short and on both inputs is applied same voltage $V_{CM}$.

$V_0 = V_{CM} * A_{CM}$

As

$CMMR = A_D / A_{CM}$

$CMMR = A_D * (V_{CM} / V_0)$ [30%]

d) If REF = 0

$V_0 = V_2 * (1 + R_1 / R_2) - V_1 * (1 + R_2 / R_1) * R_1 / R_2$

$V_0 = (V_2 - V_1) * (1 + R_1 / R_2)$

The advantage of this type of instrumentation amplifier is that required only two op-amplifiers.
Disadvantage is that Gain of the amplifier can not be lower than 2.
As input V2 is delayed for the propagation delay of the amplifier U1 and with increasing frequency phase of the input signal V1 will be different than that one at the input V2, CMRR of the amplifier will be frequency dependant.

[40%]

2.

a) In order to communicate with the microcontroller three control lines would be required such as:

a. START of CONVERSION
b. END of CONVERSION
c. OUTPUT ENABLED (DATA READY)

d. According to the pin out of the microcontroller pin B0 can be used as a START of CONVERSION as interrupt pin. Pin B1 can be selected as END of CONVERSION and pin B2 as OUTPUT ENABLE (DATA READY). Output of the comparator can be connected to the pin A4 as input to the microcontroller.
e. On interrupt from the line START of CONVERSION microcontroller will set in four cycles data to the DAC data bus starting from the MSB data set high first. After 16 sixteen cycles the output bit values will represent input voltage signalling with END of COVERSION. [10%]

b) The interface between microcontroller and DAC will convert four bit using D flip-flops into 16 bit data information. To achieve this four pins (B4 ..B7) will be data bits. Pin B3 can be used for LDAC control signal. Pins A0 and A1 would control flip-flop multiplex control unit while pins A2 and A3 would be used for DAC control signal R/W and /CS respectively. The block diagram is presented in Fig 2.1.

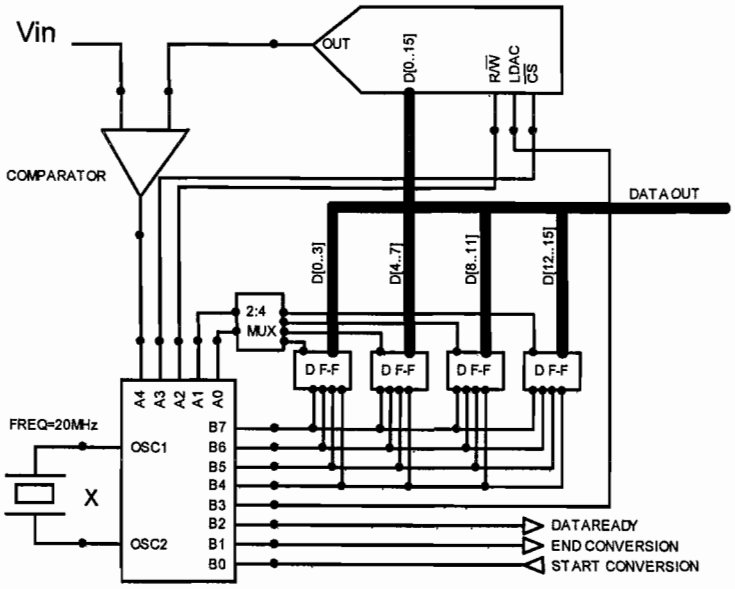
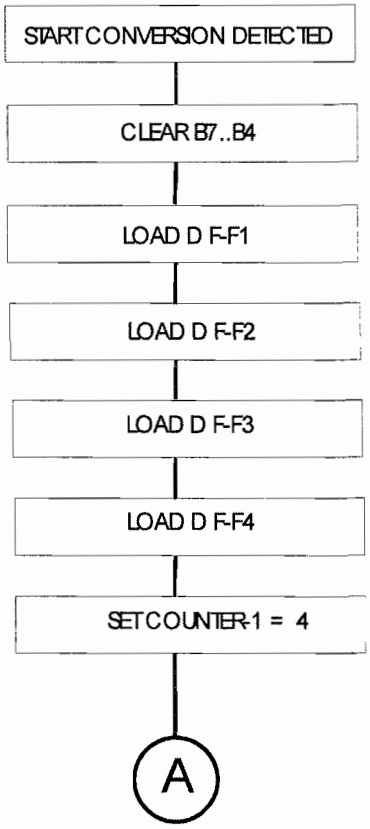
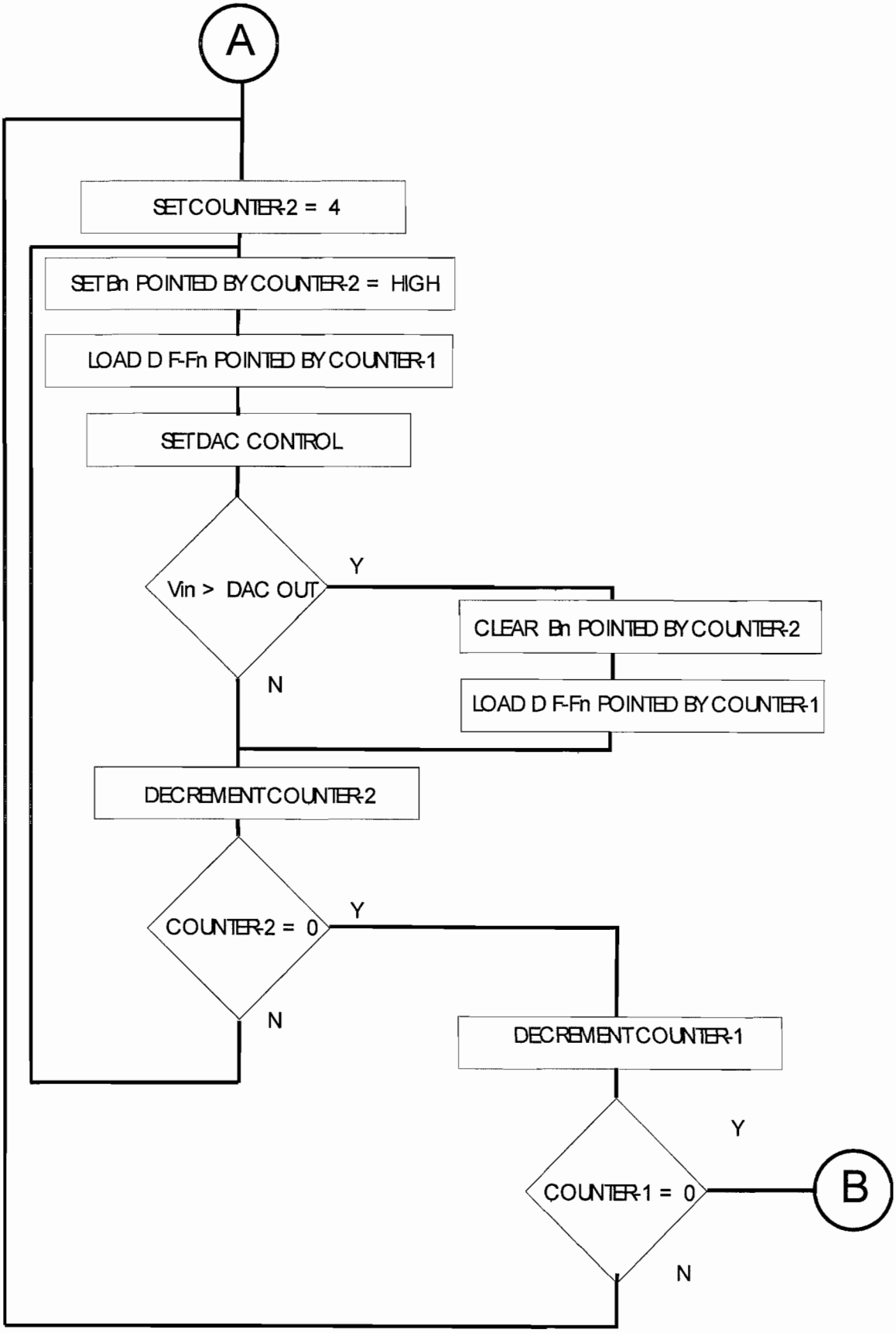


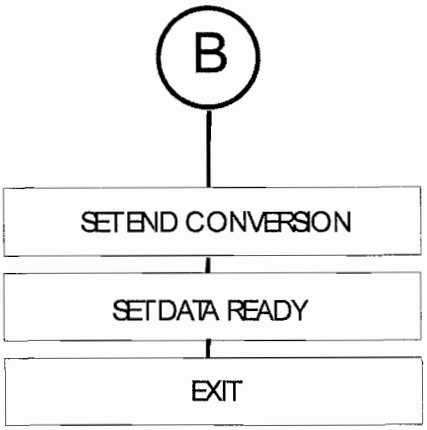

Fig 2.1

[40%]

c)


START CONVERSION DETECTED
CLEAR B7..B4
LOAD D F-F1
LOAD D F-F2
LOAD D F-F3
LOAD D F-F4
SET COUNTER-1 = 4
A


A
SET COUNTER-2 = 4
SET Bn POINTED BY COUNTER-2 = HIGH
LOAD D F-Fn POINTED BY COUNTER-1
SET DAC CONTROL
Vin > DAC OUT
Y
N
CLEAR Bn POINTED BY COUNTER-2
LOAD D F-Fn POINTED BY COUNTER-1
DECREMENT COUNTER-2
COUNTER-2 = 0
Y
N
DECREMENT COUNTER-1
COUNTER-1 = 0
Y
N
B




[30%]

d) The initial part of the A2D conversion from detection of the signal START CONVERSION to set up of the number of loops with COUNTER2 consist of seven step which can be calculated as single microcontroller instruction – 7 instructions
Setting COUNTER1 will require 1 instruction.
The first bit detection will require 8 – 9 instructions.
For four bits it will be 32 – 36 instruction.
Loading next D flip flop will require 4 instructions.
Next three D flip flop loading will require 12 instructions.
Each voltage setup at DAC will require 1 us per bit what will be in total 16 us.

It is possible to calculate that 16 bit conversion will require 66 instructions. If microcontroller oscillator is running on 20 MHz than each instruction cycle will be 200 ns. Total time used by microcontroller supporting Successive Approximation Conversion will be:

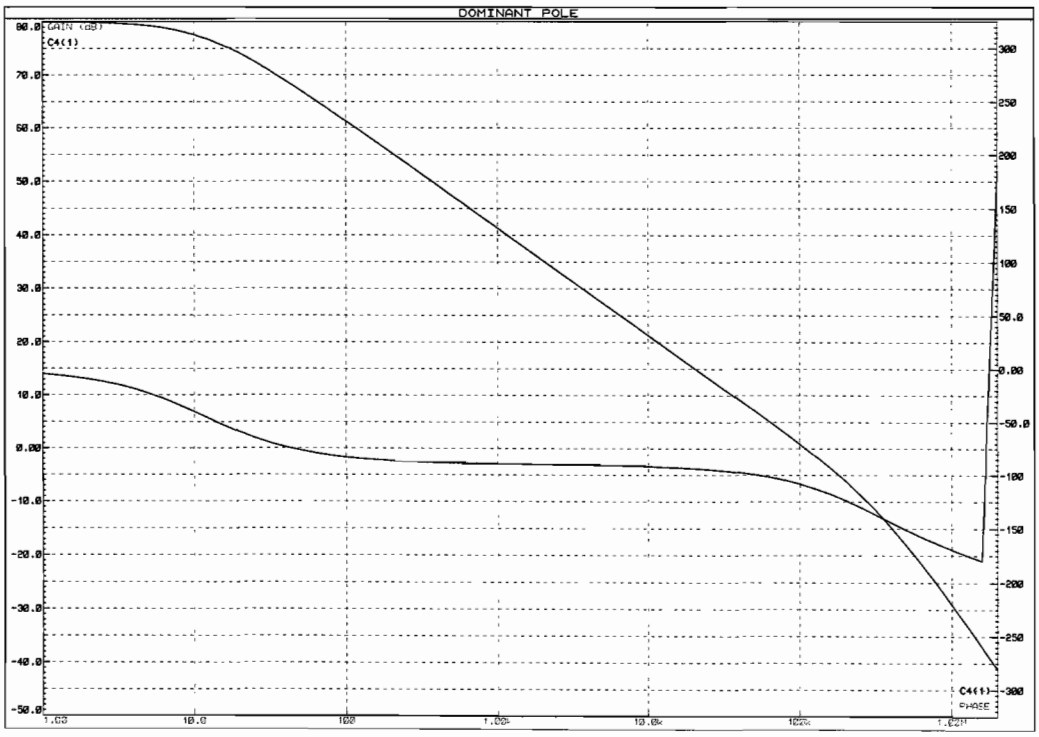
T micro = 66 * 200 ns = 13.2 us.
T dac = 16 * 1us = 16 us

Total time = T micro + T dac = 29.2 us.

[20%]

3.

a) Dominant pole is created pole so that unity gain of the amplifier coincides with the first op-amp pole and phase margin of 45 degrees. Dominant pole compensation is simple, and gives stable amplification with a waste of bandwidth.




[10%]

b) The lead compensation is presented in Fig 3.1

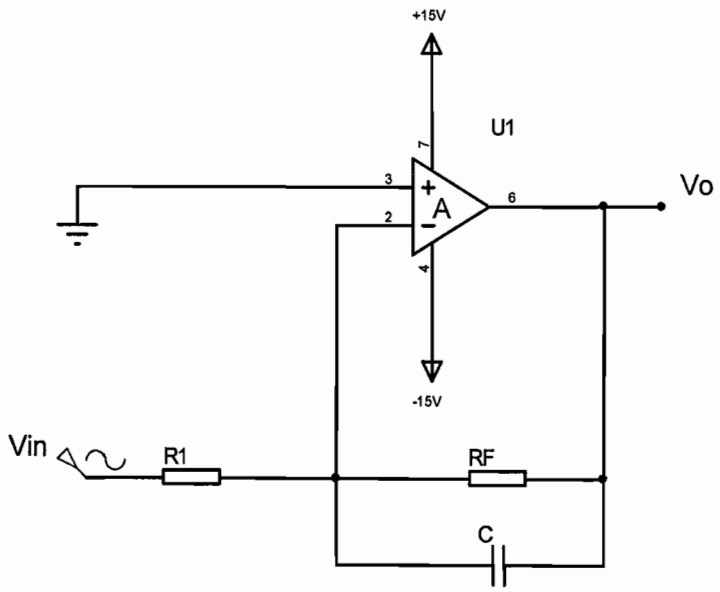
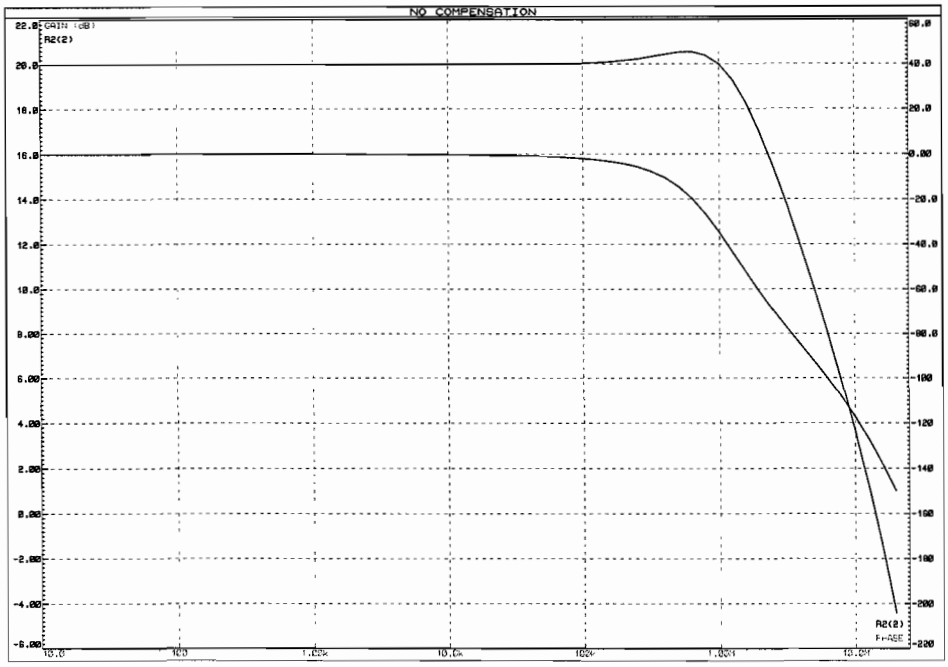
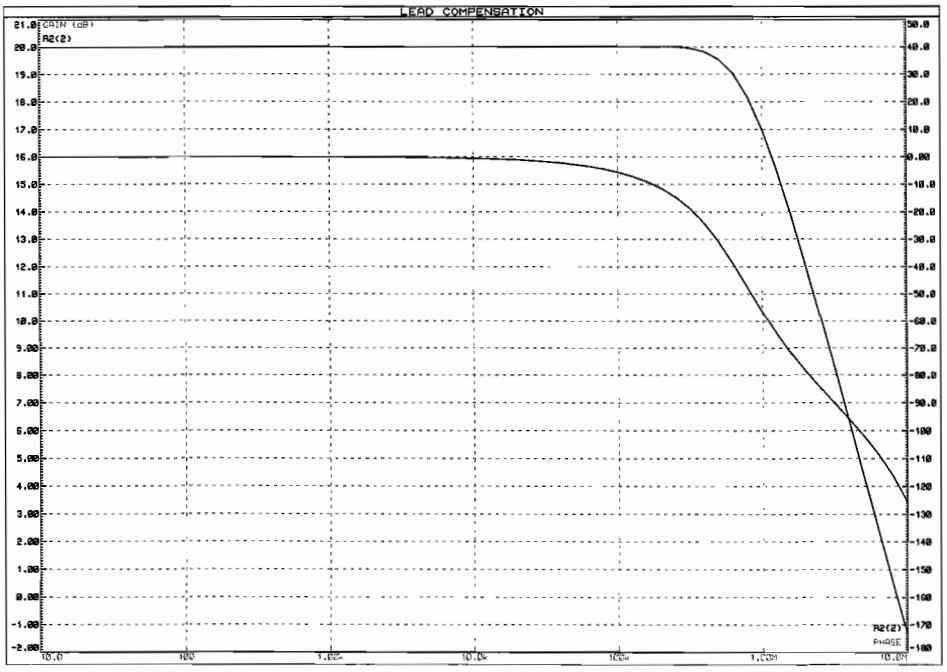



Fig 3.1

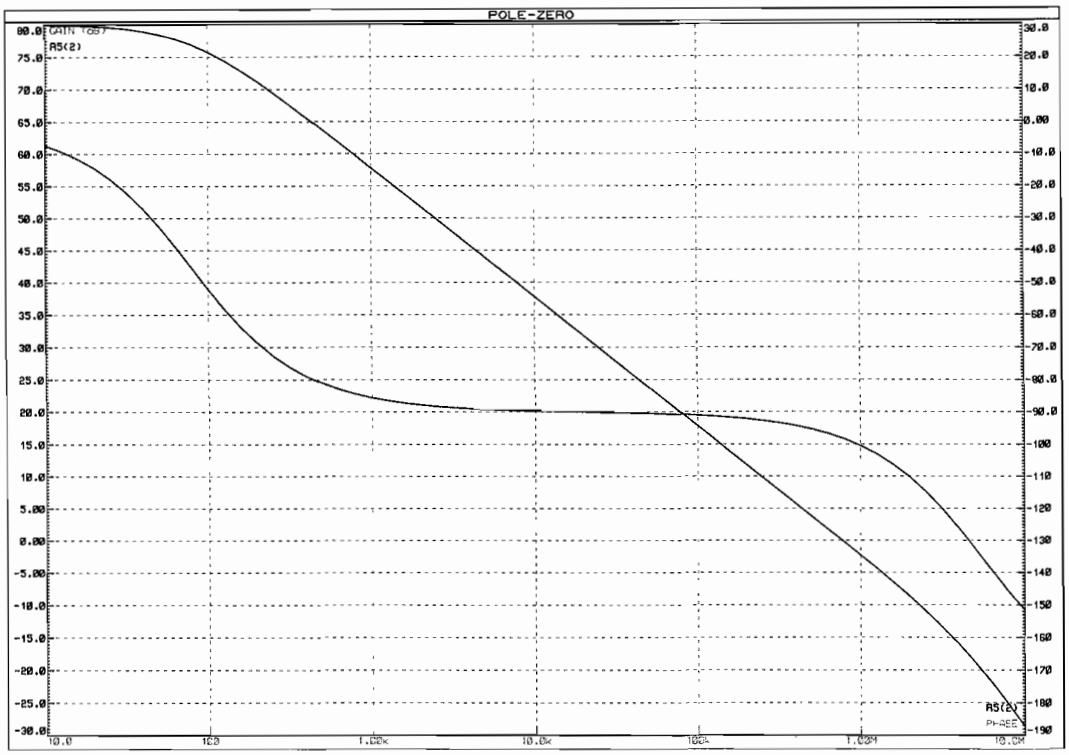
Lead compensation creates pole-zero in the loop of the transfer function and cancels out one of the poles. The best selecting point is to cancel negative phase shift caused by second pole. The bandwidth will be narrow and safe phase margin achieved for unity gain.




[20%]

c) Pole-zero (Lag-Lead) compensation cancels out one of the poles by adding an equivalent zero at that point. With this method it is possible to achieve wider bandwidth and stable operation for unity gain.




[10%]

d) In Fig 3.2 relevant voltage points and currents are marked.
i)

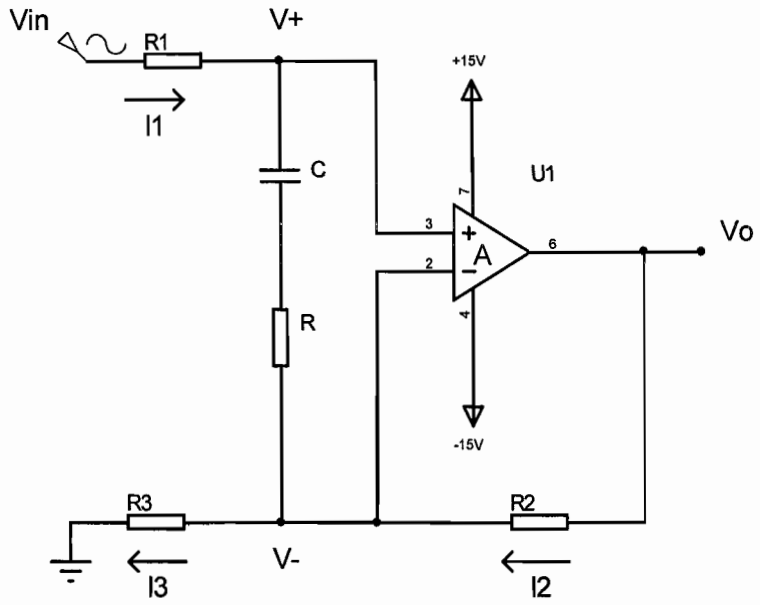



Fig 3.2

$I2 = (Vo - V-) / R2$

$I3 = I1 + I2$

$$Vo = A * I1*(R + 1/sC) \quad (1)$$

$$Z = R + 1/sC$$

$$Vo = A * I1* Z \quad (2)$$

$$V- = I3 * R3$$

$$V- = (I1 + I2) * R3$$

$$I2 = (Vo - V-) / R2 \quad (3)$$

$$V- = I1 * R3 + I2 * R3$$

$$V- = I1 * R3 + (Vo - V-) * R3 / R2$$

$$V- = I1 * R3 + Vo * R3 / R2 - V- * R3 / R2$$

$$V- + V- * R3 / R2 = I1 * R3 + Vo * R3 / R2$$

$$V- (1 + * R3 / R2) = I1 * R3 + Vo * R3 / R2$$

$$V- (R2 + * R3) / R2 = I1 * R3 + Vo * R3 / R2$$

$$V- (R2 + * R3) / R2 = (I1 * R2 + Vo) * R3 / R2$$

$$V- = (I1 * R2 + Vo) * R3 / (R2 + * R3) \quad (4)$$

$$R3 = R2 = R1$$

$$V- = (I1 * R1 + Vo) * / 2 \quad (5)$$

$$Vin - V- = I1 (R1 + Z) \quad (6)$$

$$Vin = I1 (R1 + Z) + V-$$

$$Vin = I1 (R1 + Z) + (I1 * R1 + Vo) * / 2$$

$$Vin = I1 (3 * R1 / 2 + Z) + Vo * / 2 \quad (7)$$

From eq. (2) it follows:

$$I1 = Vo / A * Z$$

Than eq. (7) will be:

$$Vin = Vo * [(3 * R1 /2 + Z) ] / A * Z + Vo * / 2$$

$$Vin = Vo *{ [(3 * R1 / 2 + Z) ] / A * Z + 1 / 2}$$

$$Vin = Vo *\{ [2 * ( 3 * R1 / 2 + Z) ] + A* Z\} / (2 *A * Z )$$

$$Vin = Vo *\{ [ (3 * R1 + 2 * Z) ] + A* Z\} / (2 *A * Z )$$

$$Vin * 2 *A * Z = Vo * ( 3 * R1 + 2 * Z+ A* Z)$$

$$Vo / Vin = (2 *A * Z ) / ( 3 * R1 + 2 * Z + A* Z)$$

$$Vo / Vin = 2 *A * Z / ( 3 * R1 + 2 * Z) / [1 + A * Z / ( 3 * R1 + 2 * Z)]$$

$$Vo / Vin = A * Z / ( 3 * R1 / 2 + Z) / [1 + A * Z / [2 * ( 3 * R1 / 2 + Z)]$$

$$Vo / Vin = A * Z / ( 3 * R1 / 2 + Z) / [1 + A / 2 * Z / ( 3 * R1 / 2 + Z)] \quad (8)$$

If compensation network Z is not present than eq. (8) will be as follows:

$$Vo / Vin = A / (1 + A / 2 ) \quad (9)$$

The gain of the circuit is defined as

$$Vo / Vin = A / (1 + A * \beta )$$

From eq. (9) I follows

$\beta = 1 / 2$ i.e.

Gain $= 1 / \beta = 2$ for equal resistors R3 and R2.

If compensation circuit is present than pole zero is defined by

$Z = R + 1 sC$

and pole is defined by

$3 * R1 / 2 + R + 1 / sC$

A pole zero will be at

$$R = 1 / sC = 1 / (2 * \pi * fpz * C )$$

$$fpz = 1 / (2 * \pi * R * C ) \quad (10)$$

A pole will be defined at:

$3 * R1 / 2 + R = 1 / sC$

$$3 * R1 / 2 + R = 1 / (2 * \pi * fp * C )$$

$$fp = 1 / [2 * \pi * C * (3 * R1 / 2 + R) ] \quad (11)$$

ii)

$f_{pz} = 1 / (2 * \pi * R * C) = 10^6 / (2 * 3.14 * 2.6 * 6) = 10.207$ kHz

$f_p = 1 / [2 * \pi * C * (3 * R1 / 2 + R)] = 10^6 / (2 * 3.14 * 6 * 17.6) = 1.507$ kHz

[60%]

4. a) The circuit of a half wave precision rectifier is shown in Fig 4.1

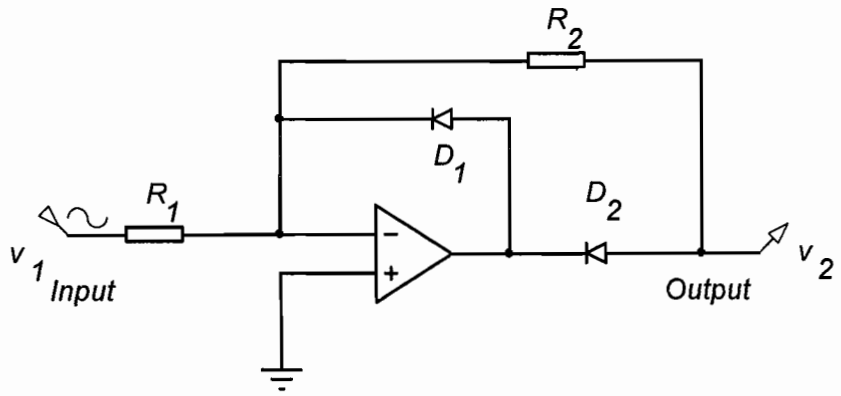



Fig 4.1

***To get a ( - ) swing rectified output, the diodes must "face away" from the output as shown.***

The ratio $R_2$ / $R_1$ will define the gain for the half cycle when diode $D_2$ is forward biased.

This is when the input is positive. Then the op-amp which inverts as inverting input is used giving negative output and $D_2$ conducts. When it is represented by an emf $V'$ as shown in Fig 4.2. The diode $D_1$ is reverse biased and runs a leakage current $I'$.

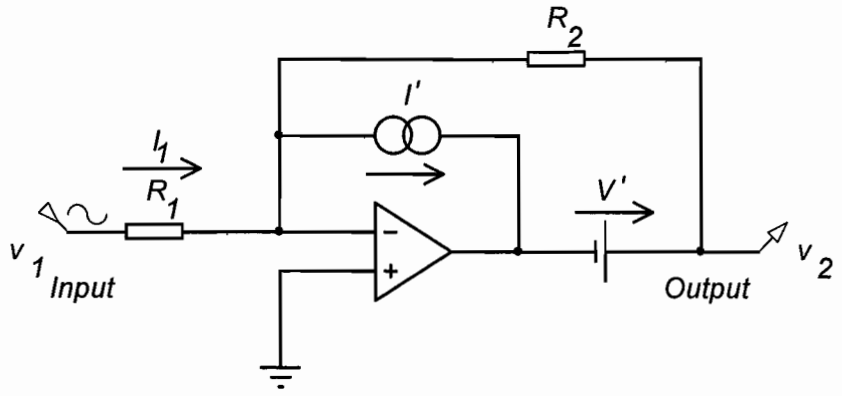



Fig 4.2

At the input:

$v_1 = I_1 * R_1 + ( v_2 - v') / (-A)$

when A is large (good amplifier)

$v_1 = I_1 * R_1$

so current through $R_2$ is:

$v_1 / R_1 - I'$

and

$+ v_2 = ( v_2 - v_1 ) / ( -A) - (v_1 / R_1 - I' ) * R_2$

as A is large

$+ v_2 = - (v_1 / R_1 - I') * R_2 = - v_1 R_2 / R_1 - I' * R_2$

the product $I' * R_2$ is error in expected output.

For the other polarity, negative input period, op-amp gives positive (inverted) output, so forwards biasing $D_1$ and it reduces to a voltage drop V'. The diode $D_2$ is reverse biased and the circuit is in Fig 4.3.

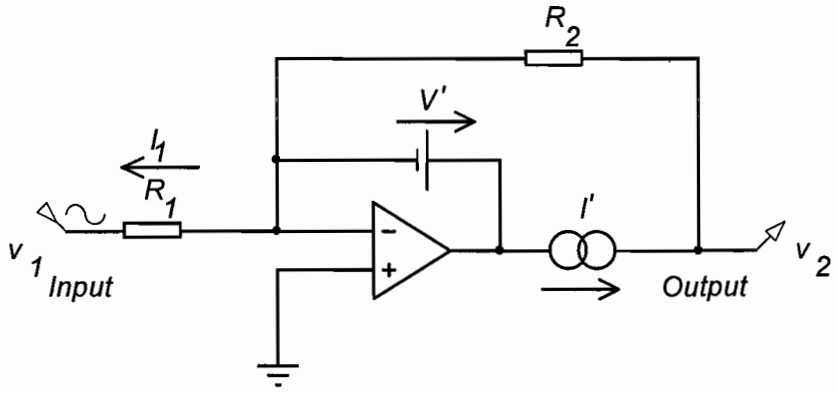



Fig 4.3

As the input, $v_1$ tends to $I_1R_1$ when A is very large and with $v_1$ negative in polarity is in direction shown. So $v_0$, the op-amp output is limited to close $V'$. Actual op-amp input is related:

$v_0 / (-A) = -V' + v_0$

as A is large

$v_0 \rightarrow -V'$

with $v_0$ swinging to positive the current I' flaws as shown and back through $R_2$,

so

$v_2 = I' * R_2 + v_0 / ( - A)$

as A is large $v_0 / (A)$ is zero

and is the small error ( a few kΩ * few nA )

[40%]

b) The resistor $R_1$ defines the input resistance:

$R_1 = 20$ kΩ

As gain of 25 is wanted:

$R_2 = 25 * R_1 = 500$ kΩ

If errors to be 0.2% of -5V and these are caused by $I' * R_2$ for both polarity swings:

$I' = 2 * 10^{-3} * 5 / (5*10^5) = 20$ nA (allowed diode leakage current)

[25%]

c) A capacitor added in Fig 4.4 will maintain the output shown in Fig 4.5.

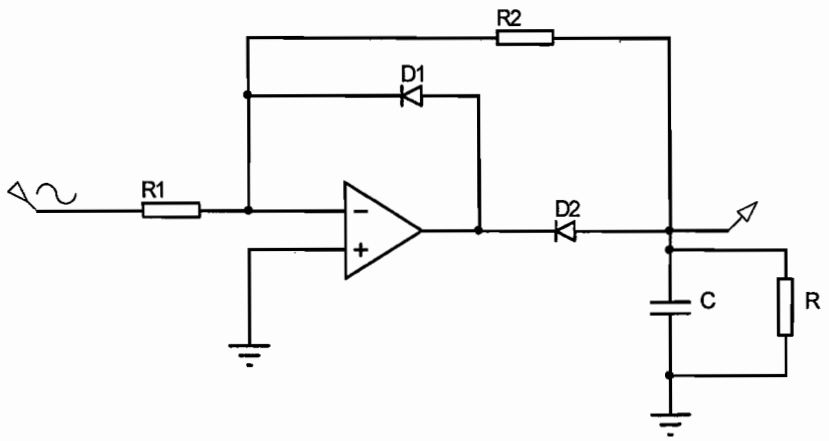



Fig 4.4

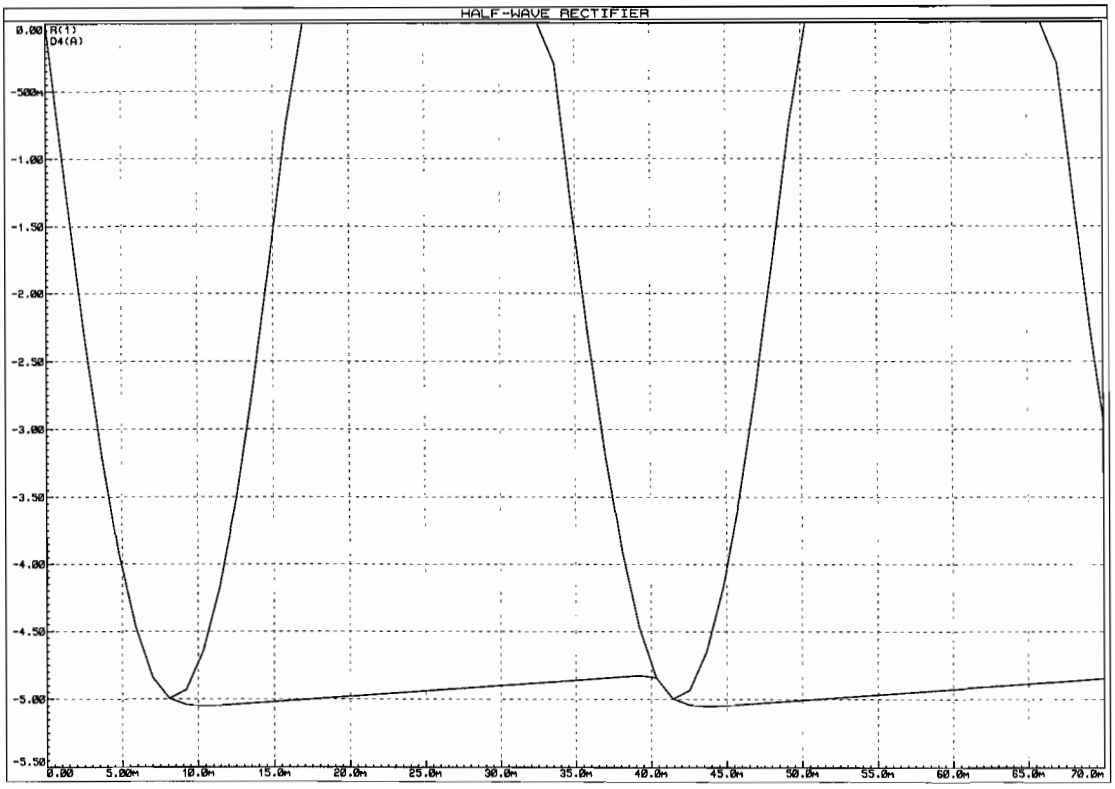



Fig 4.5

Wave will be an exponential down to 0.99 * (-5V) for the 1% droop so the equation for $v_2$ is as follow:

$v_2 = ( -5 ) * e^{-t/RC} = ( -0.99 * 5 )$

when

$t = 1 / 30$ s

$R = 5 * 10^5 \parallel 10^5 = 83.3$ kΩ

$\ln (0.99) = -0.01005 = -1 / ( 30 * C * 83.3 * 10^3 )$

$C = 1 / ( 30 * 83.3 * 10.05 )$

$C = 39.57\ 10^{-6}$

The closes value is 47 μF.

[25%]

e) Application is as a level detector to allow a recorder to fully saturate a tape say by limiting the gain as the signed amplitude wires – a fairly steady emf is fed in a gain limiting feedback circuit.

[10%]

5.

a) The Fig 5.1 shows Chebyshev ( C ) and Buterworth ( B ) responses.
Point ( A ) is defined as -3 dB at $\omega_1$ . Chebyshev filter may have a peak in gain, as shown, but then attenuate a little more rapidly both settling to -40 dB/decade for a second order filter.
Good for maintaining the gain near the turnover frequency but at the expense of light gain peak.
Gain-Bandwidth product limits the passband and give an upper -3dB point at $\omega_2$ where A * $\omega_2$ = G-B product.

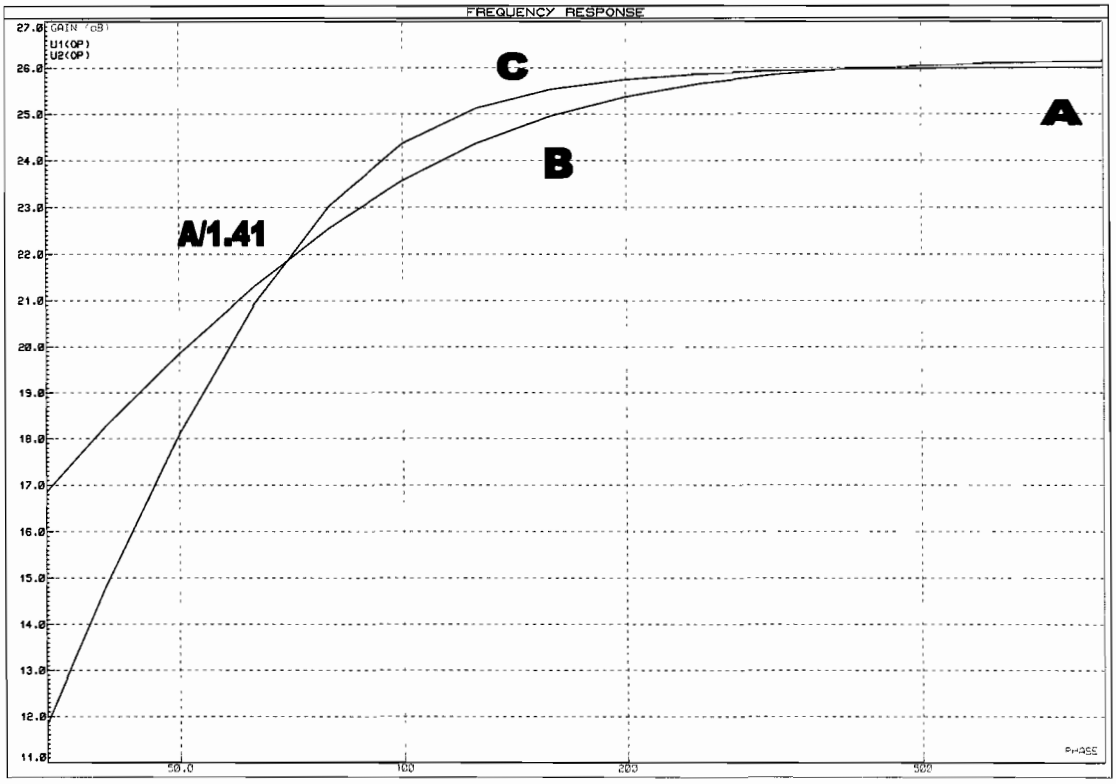



Fig 5.1

[20%]

b)

$v_2 / v_1 = As^2 / ( s^2 + 1.4s\omega_0 + 1.2\omega_0^2 )$

where $s = j\omega$

$v_2 / v_1 = A / (1 - 1.2\omega_0^2 / \omega^2 - 1.4\, \omega_0 / \omega )$

where $\omega = \omega_0$

$v_2 / v_1 = A / ( -0.2 - j\ 1.4) = A / \sqrt{2}$ ≡ Half power

when $\omega << \omega_0$

$v_2 / v_1 = A\ \omega^2 / ( -1.2\ \omega_0^2 )$

when $\omega = \omega_0 / 10$

$v_2 / v_1 = -A / 120$ ie less than Butterworth

[20%]

c) To get

$v_2 / v_1 = Y_1 Y_3 / [(Y_1 + Y_2 + Y_3 + Y_4) / R_5 + Y_3 Y_4] = As^2 / (s^2 + s + ..)$

$Y_1$ and $Y_3$ must be capacitors to get numerator OK. $Y_4$ must be a capacitor to get $s^2$ in denominator so $Y_2$ is resistive;

$Y_1 = s\ C_1$
$Y_3 = s\ C_3$
$Y_2 = 1 / R_2$

[10%]

d)

$v_2 / v_1 = s^2\ C_1 C_3 / [(sC_1 + 1/R_2 + sC_3 + sC_4) / R_5 + s^2 C_3\ C_4]$

and when divided all through to get $s^2$ term in denominator

$v_2 / v_1 = s^2 * (C_1 / C_4) /$

$[(s^2 + s * (C_1 + C_3 + C_4) / (R_5 * C_3 * C_4 ) + 1/(R_2 * R_5 * C_3 * C_4 ) ]$

Comparing this to the given equation:

Gain = $A = - C_1/C_4$ (1)

Turnover frequency:

$\omega_0 = 1/[1.2 * (R_2 * R_5 * C_3 * C_4 ) ]^{1/2}$ (2)

and

$1.4 * \omega_0 = (C_1 + C_3 + C_4) / (R_5 * C_3 * C_4 )$ (3)

[25%]

e) And desired performance figures give:

$A = 20 = - C_1/C_4$

for $C_4 = 22$ nF , $C_1 = 440$ nF

$C_4 = 22$ nF is given as is $R_5 = 10^5\Omega$

Equation (2):

$500^2 = 1/ [1.2 * 22 * 10^{-9} * R_2 * C_3 * 10^5 ]$

so

$R_2 = 1.516 * 10^{-3} / C_3$ (4)

Equation (3):

$1.4 * 500 = ( 440 + C_3 + 22 ) * 10^{-9} / ( C_3 * 10^5 * 22\ 10^{-9} * 10^{-9} )$

$1.4 * 500 * C_3 * 22 * 10^{-4} = 462 + C_3$

$C_3 = 855.56$ nF

Lastly (4) gives:

$R_2 = 1.516 * 10^{-3} / (855 * 10^{-9}) = 1.77\ k\Omega$

[25%]