ENGINEERING TRIPOS PART IIB

Tuesday 9 May 2006 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed
Supplementary pages: Extra copy of Fig. 1 (Question 1); extra copy of Fig. 2 (Question 2).

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Explain the most important technological and electrical characteristics of complementary metal-oxide-semiconductor (CMOS) silicon devices and why CMOS has displaced most other contending devices for integrated circuits. Outline briefly what is meant by a self-aligned gate technology, the current trends in device miniaturisation, and possible future limits. [40%]

(b) Figure 1 is a plan layout of a CMOS technology logic gate, where A is the 3 V power supply rail and B is the 0 V line. Explain the logic function of the device and the functions of the connections C, D, E and F.

Identify on the answer sheet copy of Figure 1 which transistors are p-type and which are n-type, and shade in each of the active regions under the transistor gates. Given that the electron mobility is twice the hole mobility in the semiconductor, comment on the relative sizes of the transistors and the relationship to device switching performance.

Sketch on the answer sheet copy of Figure 1 a suitable location for an n-type well in the p-type silicon substrate. Label the regions which are implanted with n-type dopants, and explain the electrical function of the structure near the point x=10, y=25 in Figure 1.

Draw a cross section through the transistor structures along the line y= 58 from x=0 to x=80 and identify the various conducting layers and their electrical function in the device. [60%]

(cont.

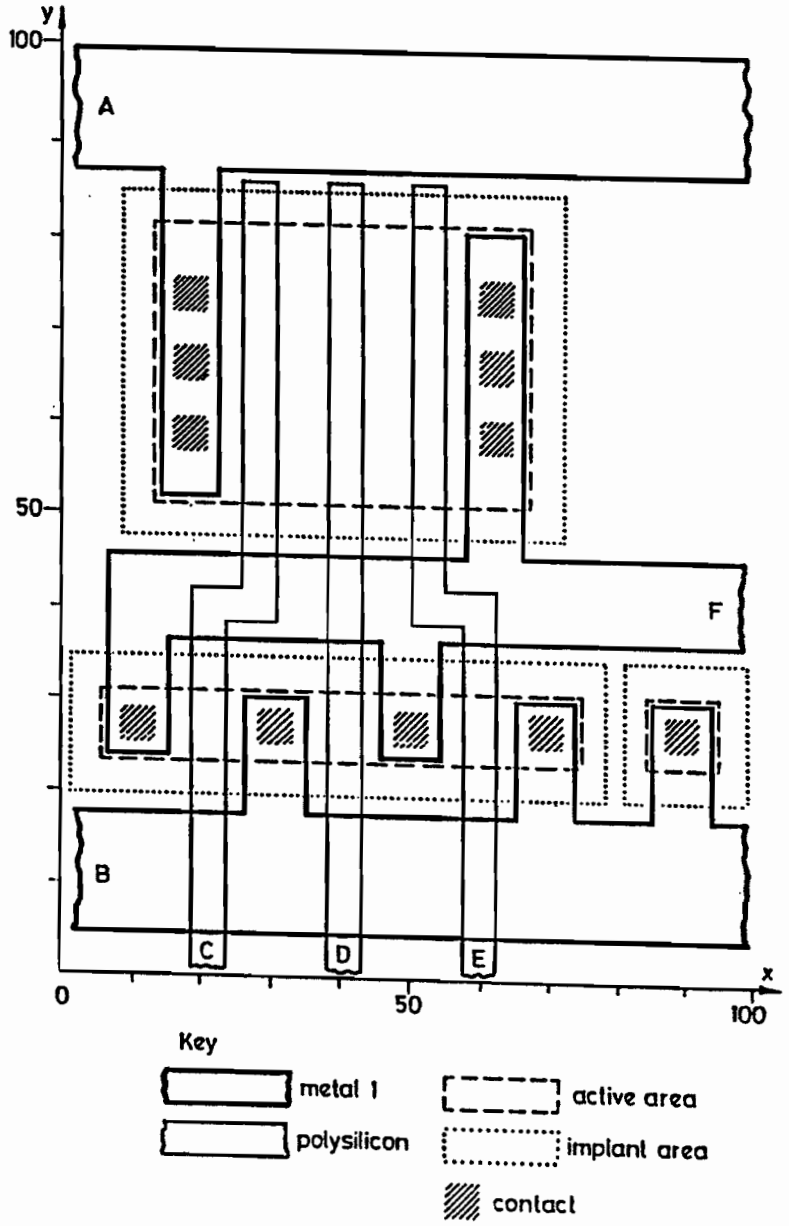


Fig. 1

(TURN OVER

2 (a) Describe the use of copper metallisation and double polysilicon in VLSI technologies. [30%]

(b) Explain why CMOS devices made using a twin-tub process are less prone to static latch-up when compared to those made in p-well or n-well processes. [20%]

(c) The cross-section of a CMOS inverter cell made in a specialised technology based on a combination of silicon-on-sapphire (SOS) and p-well VLSI technologies is shown in Fig. 2. Using the answer sheet copy of Fig. 2, draw on the cross-section the equivalent circuit responsible for the latch-up, showing specifically the transistor terminals, parasitic resistors and the connections between them. Which of the parasitic transistors is more likely to trigger the latch-up and why? [30%]

(d) State the static condition for the latch-up to occur as a function of the electrical parameters of the parasitic components. [20%]

(cont.

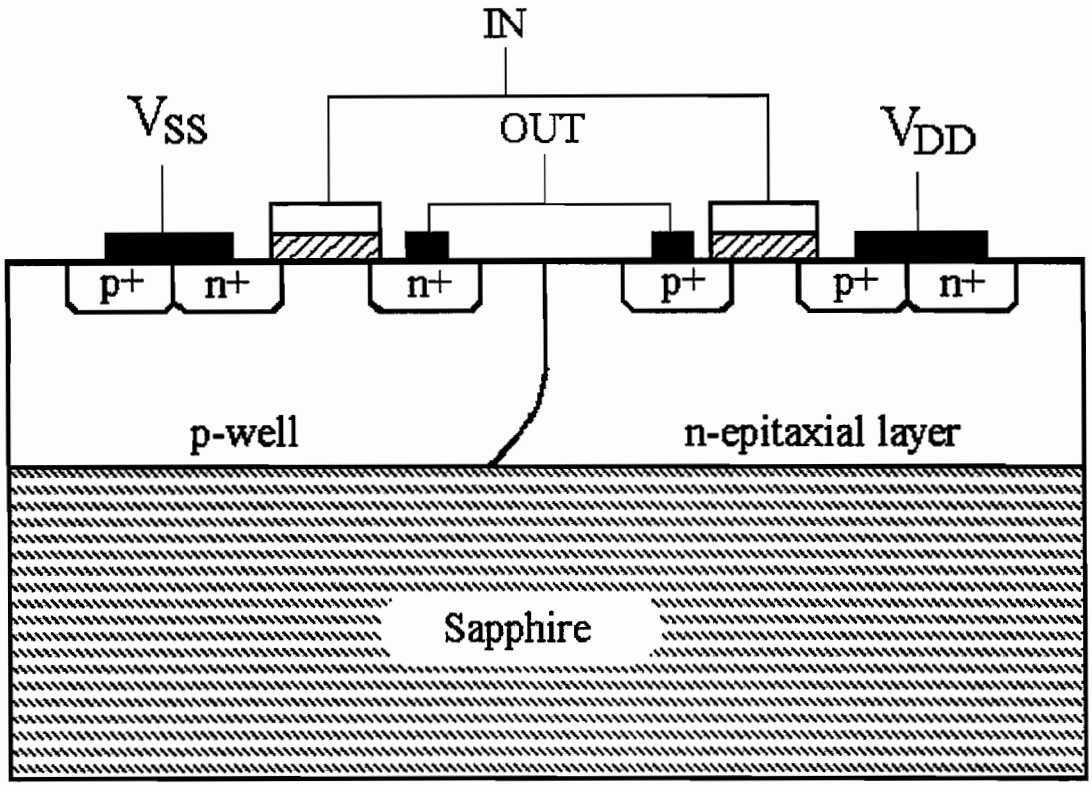


Fig. 2

(TURN OVER

3 (a) With the aid of a diagram, identify the various contributions to parasitic capacitance observed in a MOS transistor, and describe their origin. Explain how these contributions depend on:

(i) area,

(ii) perimeter, and

(iii) electrical potential

of the gate, drain and source electrodes. [40%]

(b) A simplified plan view (not to scale) showing a CMOS inverter and associated interconnect structures is shown in Fig. 3(a). The polysilicon interconnect and gate electrode are of width 2 μm, and the metal interconnect is of width 4 μm. The interconnect lengths are as shown. The active regions each have dimensions 4 μm × 16 μm.

Figure 3(b) is a table of information abstracted from the manufacturer's data about the process in use, and consists of specific capacitance values per unit area or per unit length. Using the data supplied, determine as accurately as possible the key capacitances at zero bias for this device at input and output. You should ignore the effects of contact structures for the purpose of this calculation. [40%]

Indicate qualitatively how these capacitances would be expected to change if normal device operating voltages were applied. State any assumptions made. [20%]

(cont.

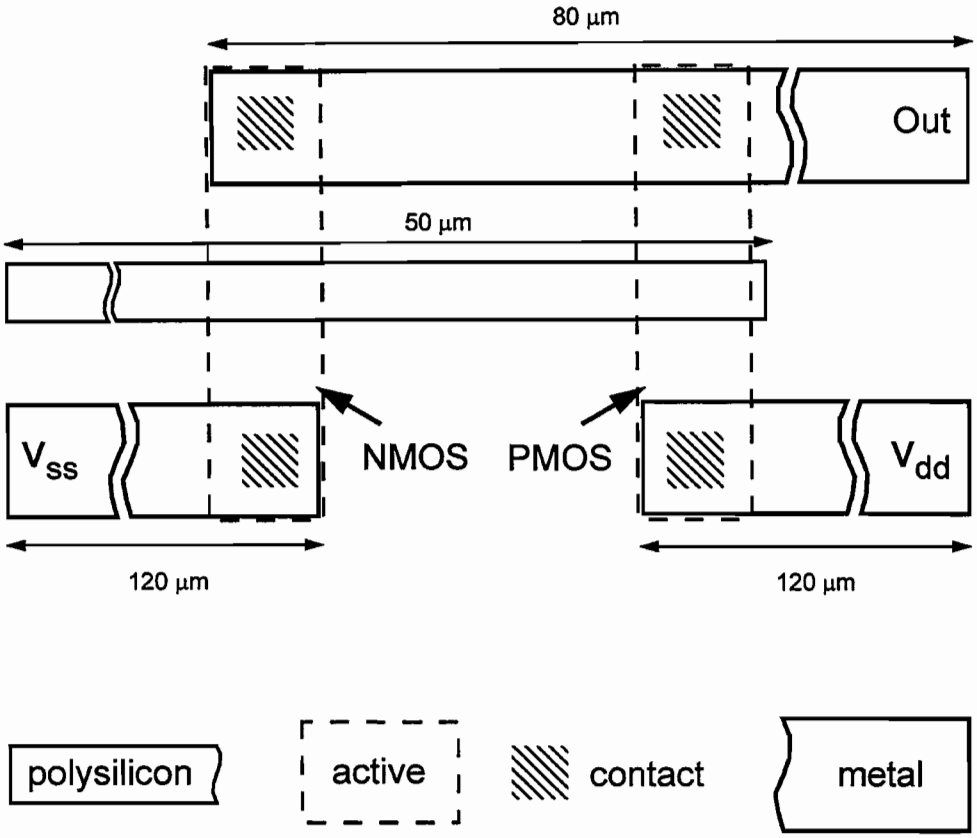


Fig 3(a)

Parameter	Value	Units	Description
C_O	7×10^{-4}	Fm^{-2}	Capacitance associated with gate oxide dielectric
C_{JA0}	1×10^{-4}	Fm^{-2}	Area capacitance to substrate (source or drain)
C_{JP0}	4×10^{-10}	Fm^{-1}	Peripheral capacitance to substrate (source or drain)
C_{GD0}	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with drain
C_{GS0}	3×10^{-10}	Fm^{-1}	Gate overlap capacitance associated with source
C_{MA}	3×10^{-5}	Fm^{-2}	Area capacitance to substrate of metal over field oxide
C_{MP}	4×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of metal over field oxide
C_{PA}	4×10^{-5}	Fm^{-2}	Area capacitance to substrate of polysilicon over field oxide
C_{PP}	5×10^{-11}	Fm^{-1}	Peripheral capacitance to substrate of polysilicon over field oxide

Fig 3(b)

(TURN OVER

4 What is the meaning of the term *clock skew* in the context of VLSI designs using CMOS technology? [30%]

In a microcontroller circuit, a clock buffer distributes a single-phase clock signal to a remote part of the circuit by means of a bus consisting of uniform polysilicon interconnect. The length and width of the interconnect are 10 mm and 2 μm respectively; the sheet resistance of the polysilicon is 40 Ω/square, and the capacitance per unit length is 2×10^{-10} F m^{-1}.

Estimate the delay incurred by the signal in propagating the length of the bus. Describe carefully how the delay would be affected if:

(i) the width of the interconnect were doubled;

(ii) a 'silicide' process were used, reducing the sheet resistance to 4 Ω/square. [40%]

Inverting buffers are available with delay properties shown graphically and algebraically in Fig. 4. Suggest a suitable amendment to the original polysilicon bus arrangement that will reduce the delay by at least a factor 2, noting that a non-inverted clock is required at the remote end of the bus. [30%]

Assume that the delay in each buffer depends only on the load capacitance it drives, and that all capacitances other than those due to interconnections can be ignored.

The following expression may be assumed for the propagation delay T of a pulse transmitted along a resistive conductor of length l:

$$T = 0.5\, rcl^2$$

where r is the resistance per unit length and c is the capacitance to substrate per unit length.

(cont.

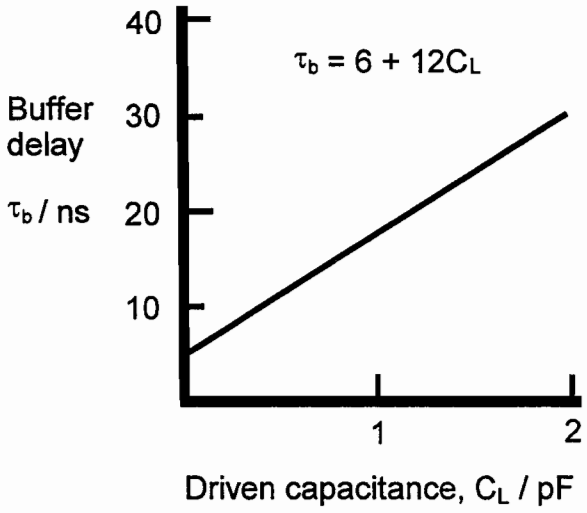


Fig 4

(TURN OVER

5 (a) Describe briefly how impurity atoms are introduced into a silicon device by

(i) growth,

(ii) diffusion, and

(iii) ion implantation,

with particular reference to CMOS technology. [30%]

Referring to the extract from the periodic table of the elements given in Fig. 5(a), which doping element would be suitable in a CMOS process for making:

(iv) a p-type well, and

(v) shallow source and drain regions for an n-channel transistor in silicon. [20%]

(b) Consider the current sink circuit shown in Fig. 5(b). Briefly describe its mode of operation. In what region of its characteristic must NMOS transistor M1 operate in order to provide a satisfactory current sink? Explain your reasoning. [10%]

Determine a suitable aspect ratio W/L for M1 if V_{GG} = 3 V and the required sink current is 100 μA. State any assumptions made. Sketch the current-voltage characteristic for the device, and estimate the small-signal output resistance. Over what range of values of drain potential V_{DS} will the circuit operate as required? [40%]

The following device parameters apply to device M1: V_T = +1 V, λ = 0.01 V^{-1}, and $\mu\varepsilon/t_{OX}$ = 15 × 10^{-6} AV^{-2}. You may assume the following expressions for the drain current I_D in a MOS transistor.

$$I_D = \frac{\mu\varepsilon}{t_{OX}}\frac{W}{L}\left((V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right)(1+\lambda V_{DS}) \qquad 0 < V_{DS} < (V_{GS}-V_T)$$

$$I_D = \frac{1}{2}\frac{\mu\varepsilon}{t_{OX}}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS}) \qquad 0 < (V_{GS}-V_T) < V_{DS}$$

(cont.

B	C	N	O
Al	Si	P	S
Ga	Ge	As	Se

Fig 5(a)

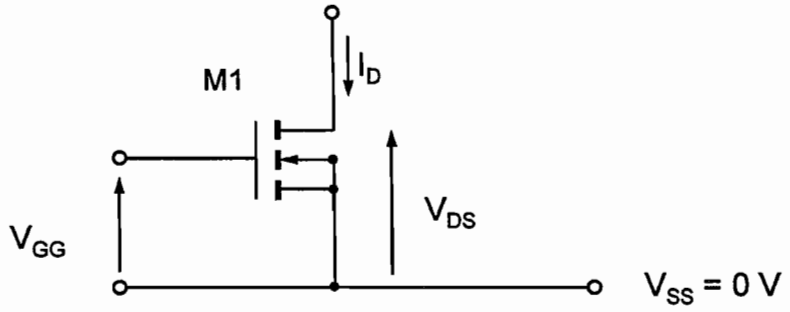


Fig 5(b)

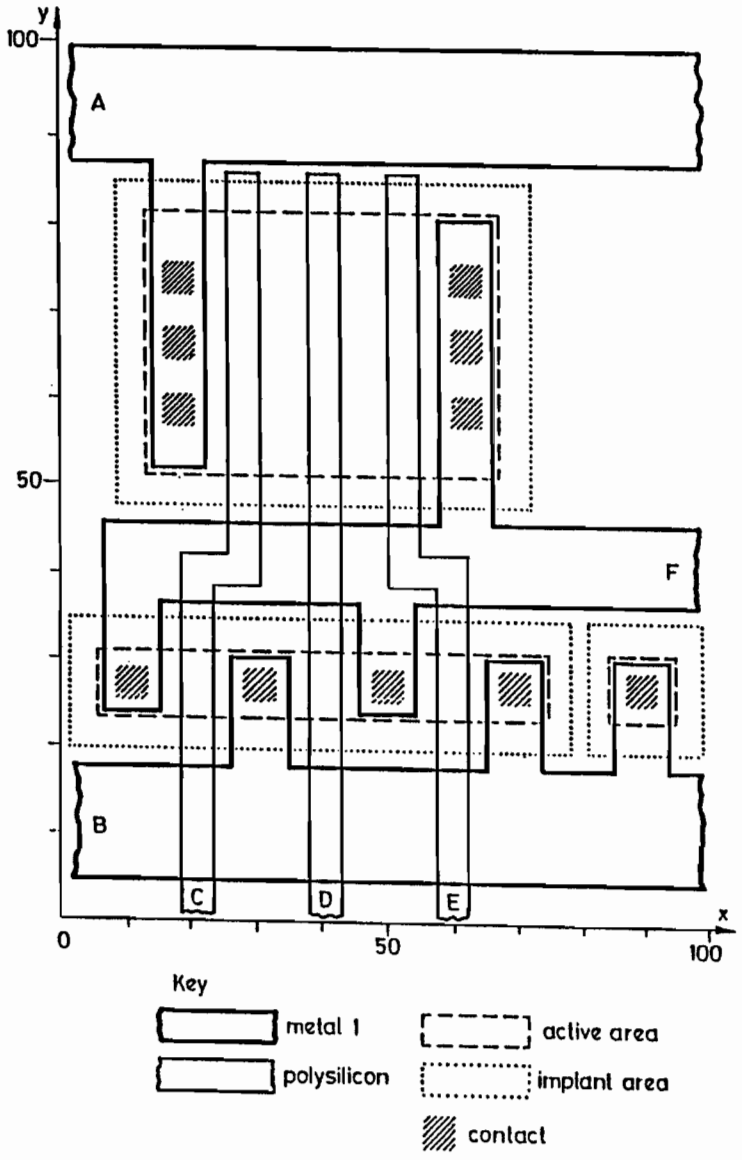
END OF PAPER

ENGINEERING TRIPOS PART IIB

Tuesday 9 May 2006 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD



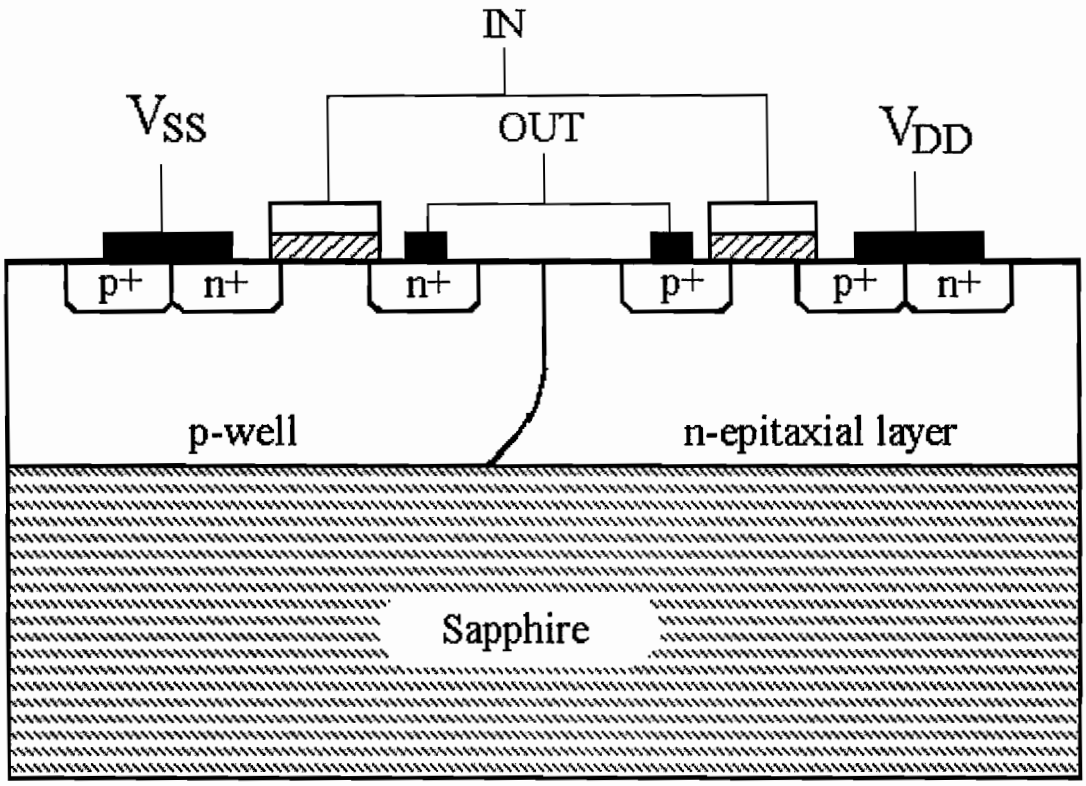
Additional copy of Fig. 1
(may be handed in with your script)

ENGINEERING TRIPOS PART IIB

Tuesday 9 May 2006 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD



Additional copy of Fig. 2
(may be handed in with your script)