ENGINEERING TRIPOS PART IIB

Monday 1 May 2006 9.00 to 10.30

Module 4B8

ELECTRONIC SYSTEM DESIGN

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachments: data sheets
Appendix 1 - OP-270A data sheet (2 pages)
Appendix 2 - DAC 7741 data sheet (1 page)
Appendix 3 - PIC16F84 data sheet (1 page)

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed
Supplementary pages: Two extra copies of Fig. 2 (Question 2).

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

Version: 6

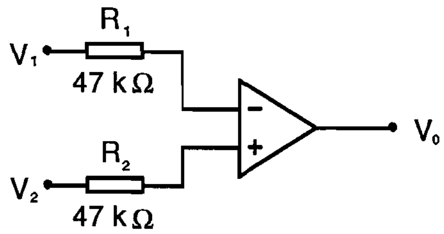
1. For low frequency and precision measurements with an op-amp the non-ideal characteristics of the amplifiers should be considered, such as the input offset voltage, input bias current, temperature effects and common mode gain.

a) Define and describe the characteristics of an *input offset voltage* and an *input bias current.* [20%]

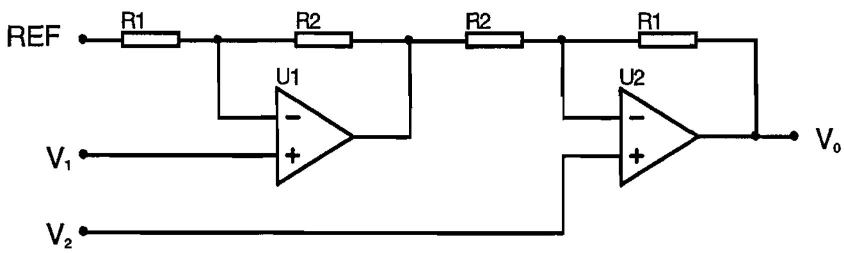
b) Fig. 1(a) shows an OP-270A op-amp with a gain of 20. Calculate the voltage output for ambient temperatures at -40°C and +80°C, using data from the data sheet in Appendix 1. [10%]

c) Draw the circuit structure for an instrumentation amplifier based on three op amps and derive expressions for its gain and CMRR (common mode rejection ratio). [30%]

d) Derive an expression for the gain of the instrumentation amplifier circuit shown in Fig. 1(b) and describe the advantages and disadvantages of this circuit. [40%]



(a)



(b)

Fig. 1

2. The partial block diagram of a *Successive Approximation Analogue to Digital Converter (ADC)* is shown in Fig 2. The Digital to Analogue Converter (DAC) is a 16 bit parallel input device with the timing diagram given in Appendix 2 (DAC7741). The pin out of the microcontroller is given in Appendix 3 (PIC16F84). A comparator is available, whose characteristics can be viewed as ideal.

a) Describe by annotating the answer sheet copy of Fig. 2, how would you use the microcontroller in order to achieve Analogue to Digital conversion. [10%]

b) Draw a block diagram schematic for the interface unit between the microcontroller and the DAC and describe your solution. [40%]

c) Using a flow diagram, describe a Successive Approximation Analogue to Digital conversion algorithm for your design. [30%]

d) What will be minimum data conversion time achievable if:

- reading the comparator status requires 2 instructions,
- setting an output bit from the microcontroller requires 1 instruction,
- the voltage settling of the DAC output is 1 μs and
- the microcontroller oscillator frequency is 20 MHz ? [20%]

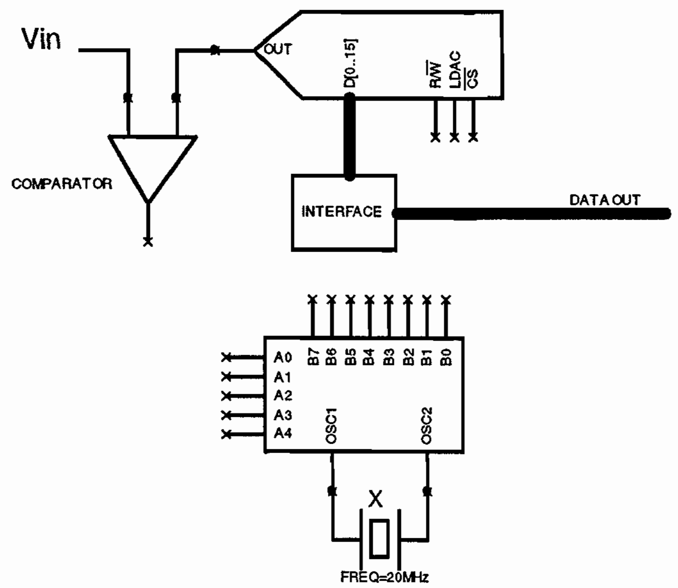


Fig. 2

3. a) Internally compensated op-amps are usually compensated with a method called "dominant-pole". Define and explain the "dominant-pole" compensation scheme. [10%]

b) Sketch an op-amp circuit with lead compensation and describe how it works including a Bode plot diagram for gain and phase. [20%]

c) Describe pole-zero compensation and draw a Bode plot diagram for gain and phase. [10%]

d) An example of input frequency compensation is shown in Fig 3.

i) Derive expressions for the pole and pole-zero assuming that the differential amplifier has a finite gain A and is otherwise ideal.

ii) If resistors R_1, R_2 and R_3 are equal to $10k\Omega$, $R = 2.6\ k\Omega$ and $C = 6\ nF$ calculate the pole-zero (lag-lead) and pole for this circuit. [60%]

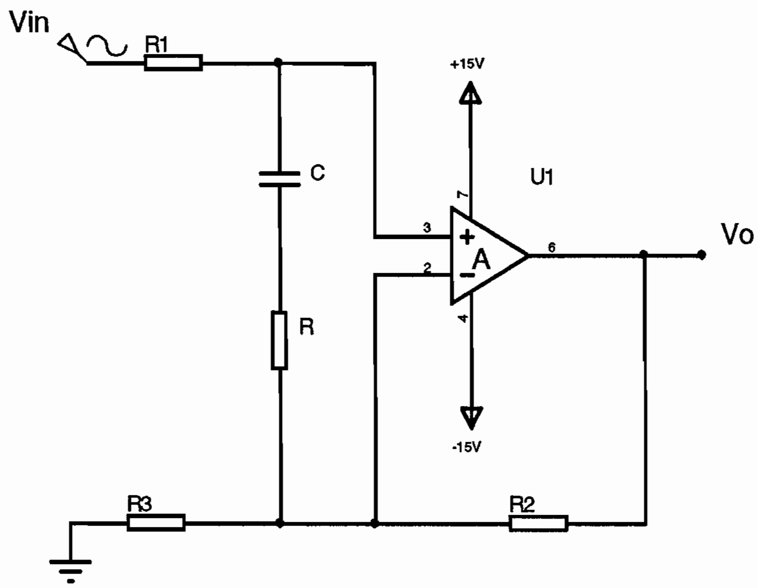


Fig. 3

4. An accurate *half-wave* rectifier is required using a *single* op-amp which will give a -5 V peak output when the input is a sine wave with a 0.2 V peak value. The circuit input resistance is to be $20\ \text{k}\Omega$ and errors of no more than 0.2% of the expected peak output voltage should be allowed.

a) Draw a suitable circuit diagram to achieve this. Explain clearly its operation for both polarities of the input voltage. Any diodes used are modeled as having a leakage current I_0 when reverse biased and having a forward voltage drop V_0 when forward biased. Explain clearly how errors arise. [40%]

b) Specify values of all components in the circuits and calculate the value of the parameter which would lead to an error of no more than 0.2% of the output peak value. [25%]

c) Show how additional components will allow the peak output voltage to be maintained on a capacitor with a droop of only 1% at 30 Hz. Determine the value of the capacitor needed if the voltmeter measuring the peak output voltage has an input resistance of $100\ \text{k}\Omega$. [25%]

d) Explain briefly a possible common application for a peak voltage detector. [10%]

5. a) A high pass active filter is to have a *Chebyshev* response. Sketch the expected gain against frequency response for this filter, comparing it to a *Butterworth* filter. For what applications are both filter types best suited ?
How does the (gain × bandwidth) product of the op-amp become a limitation ? [20%]

a) Consider the polynomial:-

$$\frac{v_2}{v_1} = \frac{As^2}{s^2 + 1.4s\omega_0 + 1.2\omega_0^2} \qquad \text{where } s = j\omega.$$

If it relates to a circuit input voltage v_1 and output voltage v_2, show how it has the desired *Chebyshev* high pass filter form with a turn-over frequency ω_0. What is the magnitude of the gain when $\omega = \omega_0$? [20%]

c) The *Chebyshev* active filter circuit shown at Fig. 5 has a gain given by:-

$$\frac{v_2}{v_1} = \frac{-Y_1 Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3 Y_4}$$

where Y_1 to Y_5 are the *conductances* of the components. If the component connected between the op-amp output and the inverting input is a resistor, determine the types of the other components to give the desired form of response. [10%]

d) Obtain expressions for the passband gain A and the turn-over frequency ω_0 for the circuit in Fig 5 in terms of the conductances Y_1 to Y_5. [25%]

e) If a filter is required with A = -20 , ω_0 = 500 rad / s , and if the resistor defining Y_5 is 100 kΩ and Y_4 is a capacitor with value 22 nF , determine the values of the other components. [25%]

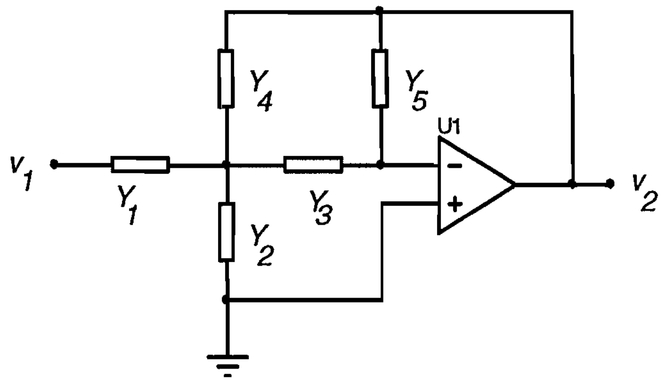


Fig. 5

END OF PAPER

OP-270

ground noise and power supply fluctuations. Power consumption of the dual OP-270 is one-third less than two OP-27s, a significant advantage for power conscious applications. The OP-270 is unity-gain stable with a gain-bandwidth product of 5MHz and a slew rate of 2.4V/μs.

The OP-270 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, dual buffers, and low-noise active filters.

The OP-270 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, SE5532/A, RM4558 and HA5102 dual op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-271, with a slew rate of 8V/μs, is recommended. For a quad op amp, see the OP-470.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±18V
Differential Input Voltage (Note 2) .... ±1.0V
Differential Input Current (Note 2) .... ±25mA
Input Voltage .... Supply Voltage
Output Short-Circuit Duration .... Continuous
Storage Temperature Range
P, RC, S, Z-Package .... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) .... 300°C
Junction Temperature (T_j) .... –65°C to +150°C
Operating Temperature Range
OP-270A .... –55°C to +125°C
OP-270E, OP-270F, OP-270G .... –40°C to +85°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jc}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-270's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±10V, the input current should be limited to ±25mA.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

			OP-270A/E			OP-270F			OP-270G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	–	–	10	75	–	20	150	–	50	250	μV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1	10	–	3	15	–	5	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	5	20	–	10	40	–	15	60	nA
Input Noise Voltage	$e_{n\,p\text{-}p}$	0.1Hz to 10Hz (Note 1)	–	80	200	–	80	200	–	80	–	nVp-p
Input Noise Voltage Density	e_n	$f_O = 10Hz$	–	3.8	6.5	–	3.6	6.5	–	3.6	–	nV/√Hz
		$f_O = 100Hz$	–	3.2	5.5	–	3.2	5.5	–	3.2	–	
		$f_O = 1kHz$ (Note 2)	–	3.2	5.0	–	3.2	5.0	–	3.2	–	
Input Noise Current Density	i_n	$f_O = 10Hz$	–	1.1	–	–	1.1	–	–	1.1	–	pA/√Hz
		$f_O = 100Hz$	–	0.7	–	–	0.7	–	–	0.7	–	
		$f_O = 1kHz$	–	0.6	–	–	0.6	–	–	0.6		
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$, $R_L = 10k\Omega$	1500	2300	–	1000	1700	–	750	1500	–	V/mV
		$R_L = 2k\Omega$	750	1200	–	500	900	–	350	700	–	
Input Voltage Range	IVR	(Note 3)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13.5	–	±12	±13.5	–	±12	±13.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	106	125	–	100	120	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	–	0.56	3.2	–	1.0	5.6	–	1.5	6	μV/V
Slew Rate	SR		1.7	2.4	–	1.7	2.4	–	1.7	2.4	–	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-270A/E MIN	OP-270A/E TYP	OP-270A/E MAX	OP-270F MIN	OP-270F TYP	OP-270F MAX	OP-270G MIN	OP-270G TYP	OP-270G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4	6.5	–	4	6.5	–	4	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	$V_O = 20V_{p\text{-}p}$ $f_O = 10Hz$ (Note 1)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	$A_V = +1$, 10V Step to 0.01%	–	5	–	–	5	–	–	5	–	µs

NOTES:
1. Guaranteed by not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$ for OP-270A, unless otherwise noted.

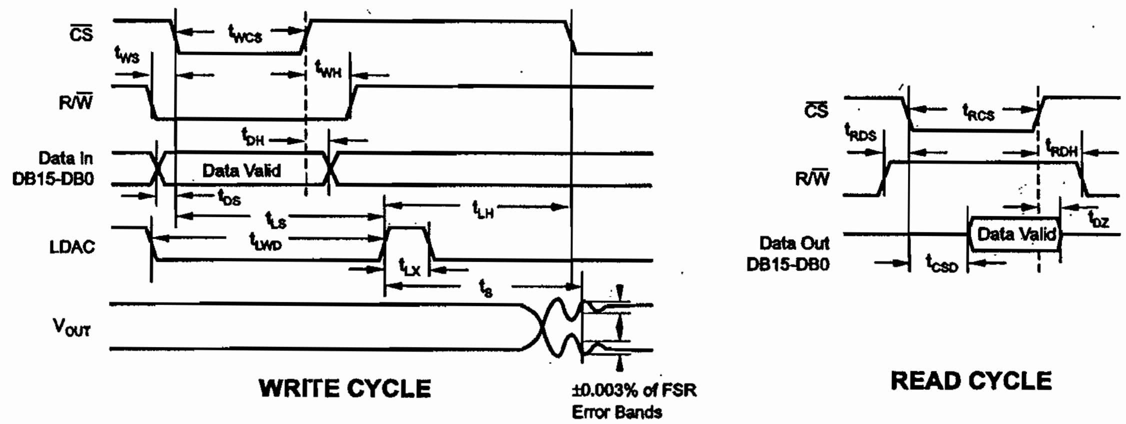
PARAMETER	SYMBOL	CONDITIONS	OP-270A MIN	OP-270A TYP	OP-270A MAX	UNITS
Input Offset Voltage	V_{OS}		–	30	175	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	2	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$	750	1600	–	V/mV
		$R_L = 2k\Omega$	400	800	–	
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	100	120	–	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm4.5V$ to $\pm18V$	–	1.0	5.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	7.5	mA

NOTE:
1. Guaranteed by CMR test.

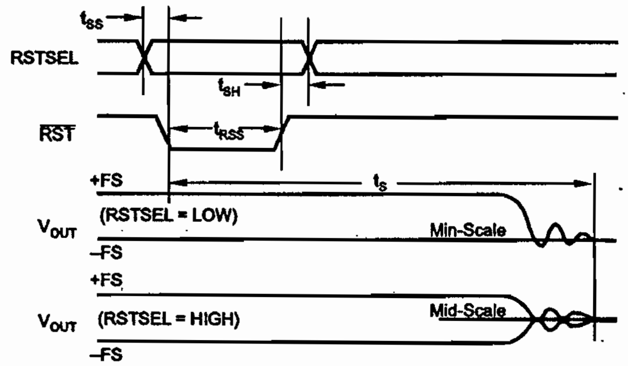
TIMING CHARACTERISTICS

PARAMETER	DESCRIPTION	DAC7741Y MIN	DAC7741Y TYP	DAC7741Y MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	100			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus High Impedance	10		70	ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		85	100	ns
t_{WCS}	$\overline{CS}$ LOW for Write	30			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	10			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{LS}	$\overline{CS}$ LOW to LDAC HIGH	40			ns
t_{LH}	$\overline{CS}$ LOW after LDAC HIGH	0			ns
t_{LX}	LDAC HIGH	30			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	20			ns
t_{LWD}	LDAC LOW	40			ns
t_{SS}	RSTSEL Valid Before $\overline{RST}$ LOW	0			ns
t_{SH}	RSTSEL Valid After $\overline{RST}$ HIGH	10			ns
t_{RSS}	$\overline{RST}$ LOW	30			ns
t_S	Voltage Output Settling Time			5	µs

TIMING DIAGRAMS



RESET TIMING



MICROCHIP

PIC16F84A

18-pin *Enhanced* FLASH/EEPROM 8-Bit Microcontroller

High Performance RISC CPU Features:

- Only 35 single word instructions to learn
- All instructions single-cycle except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- 1024 words of program memory
- 68 bytes of Data RAM
- 64 bytes of Data EEPROM
- 14-bit wide instruction words
- 8-bit wide data bytes
- 15 Special Function Hardware registers
- Eight-level deep hardware stack
- Direct, indirect and relative addressing modes
- Four interrupt sources:
  - External RB0/INT pin
  - TMR0 timer overflow
  - PORTB<7:4> interrupt-on-change
  - Data EEPROM write complete

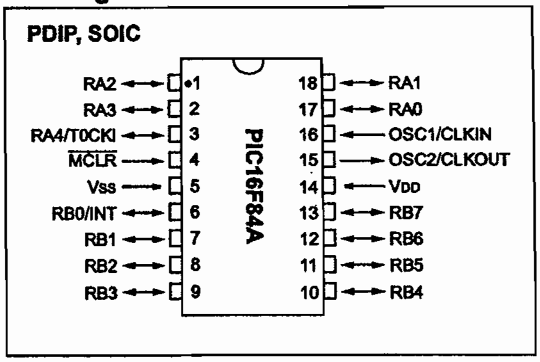
Peripheral Features:

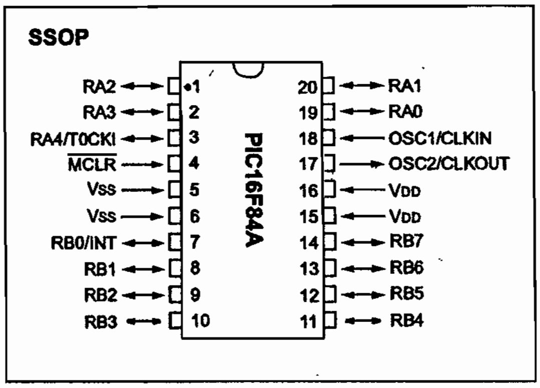
- 13 I/O pins with individual direction control
- High current sink/source for direct LED drive
  - 25 mA sink max. per pin
  - 25 mA source max. per pin
- TMR0: 8-bit timer/counter with 8-bit programmable prescaler

Special Microcontroller Features:

- 10,000 erase/write cycles *Enhanced* FLASH Program memory typical
- 10,000,000 typical erase/write cycles EEPROM Data memory typical
- EEPROM Data Retention > 40 years
- In-Circuit Serial Programming™ (ICSP™) - via two pins
- Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own On-Chip RC Oscillator for reliable operation
- Code protection
- Power saving SLEEP mode
- Selectable oscillator options

Pin Diagrams





CMOS Enhanced FLASH/EEPROM Technology:

- Low power, high speed technology
- Fully static design
- Wide operating voltage range:
  - Commercial: 2.0V to 5.5V
  - Industrial: 2.0V to 5.5V
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 2V, 32 kHz
  - < 0.5 µA typical standby current @ 2V

ENGINEERING TRIPOS PART IIB

Monday 1 May 2006 9.00 to 10.30

Module 4B8

ELECTRONIC SYSTEM DESIGN

Question 2

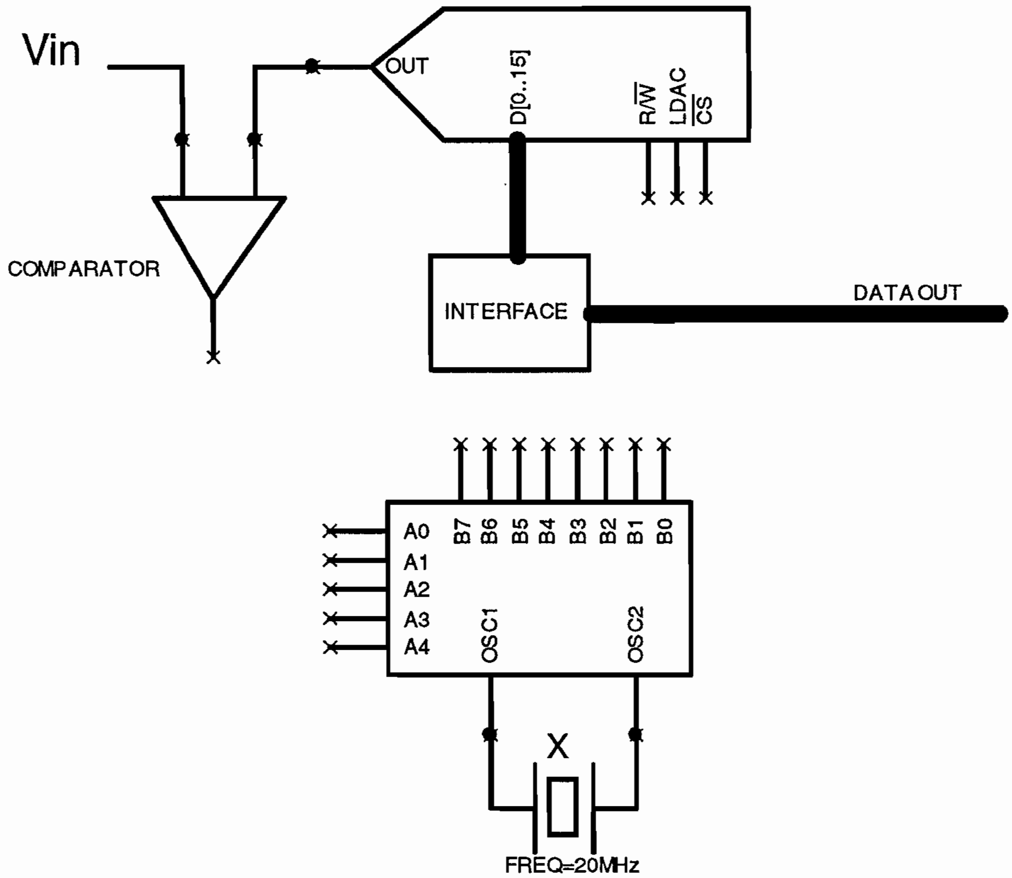


Fig. 2

ENGINEERING TRIPOS PART IIB

Monday 1 May 2006 9.00 to 10.30

Module 4B8

ELECTRONIC SYSTEM DESIGN

Question 2

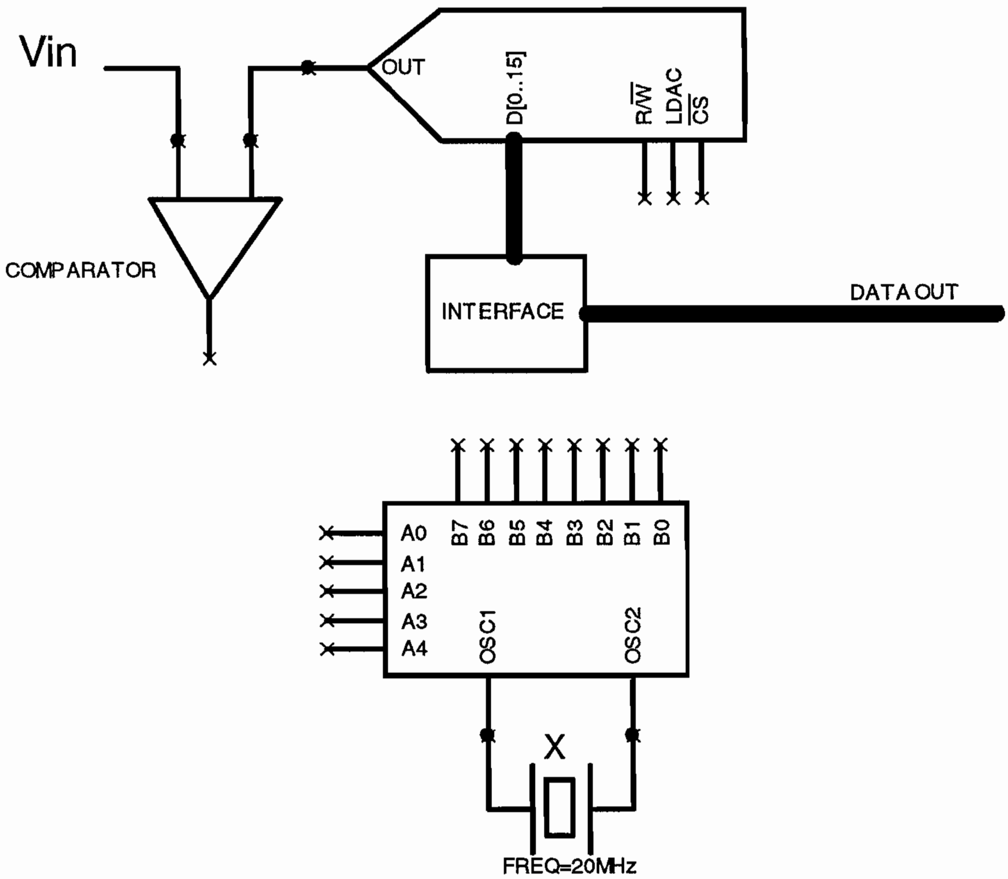


Fig. 2