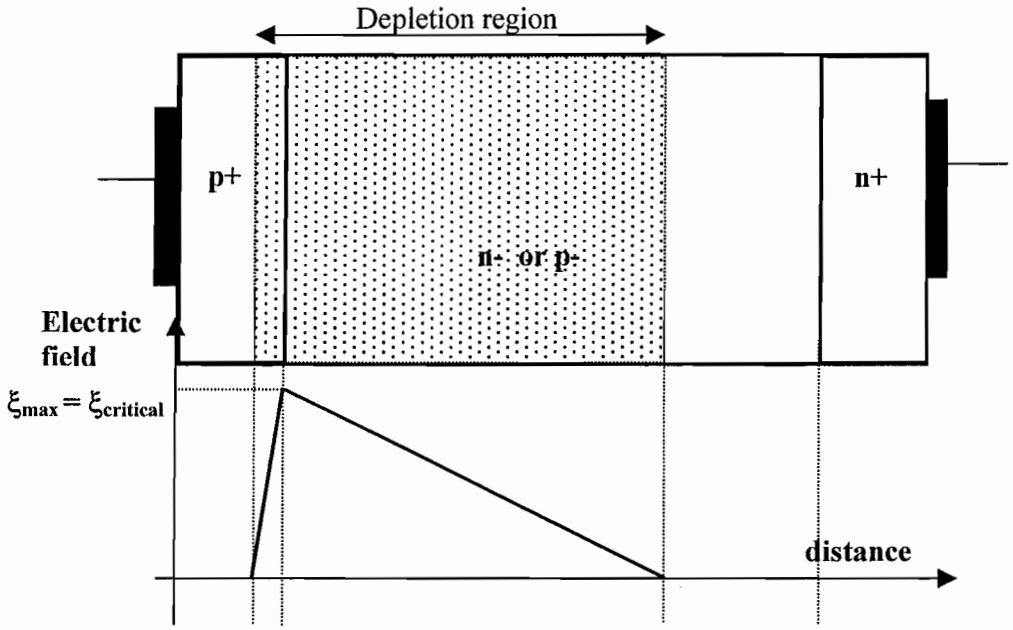
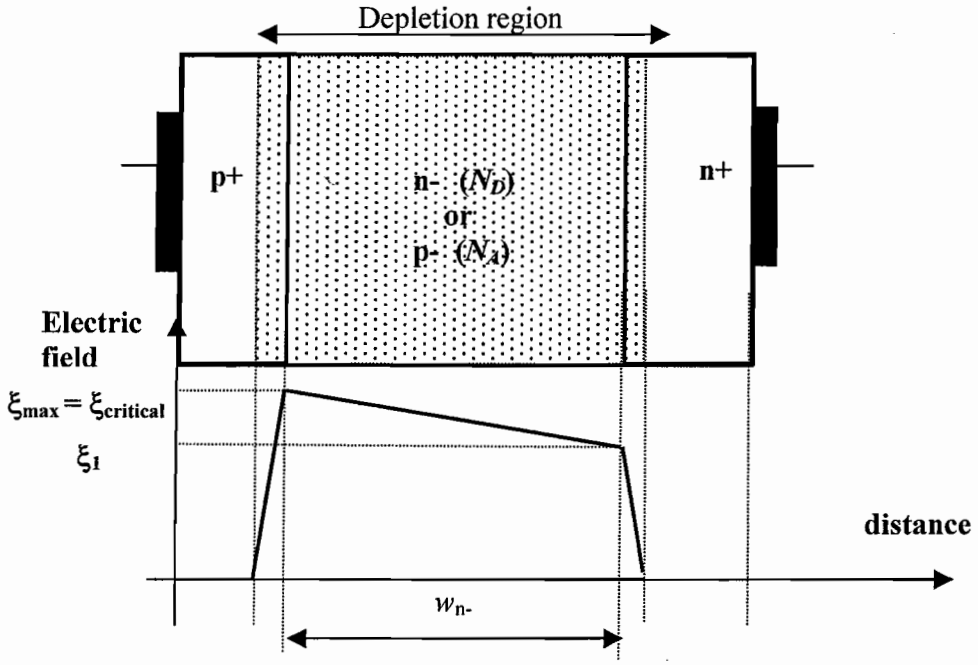
Answers:

1. (a) The Non punch-through (NPT) high voltage diode is a based on a PIN diode where the thickness (width) of the lowly doped layer (n- or p-) is larger than the depletion region thickness (width) at breakdown. Thus the depletion region never reaches the n+ cathode region.



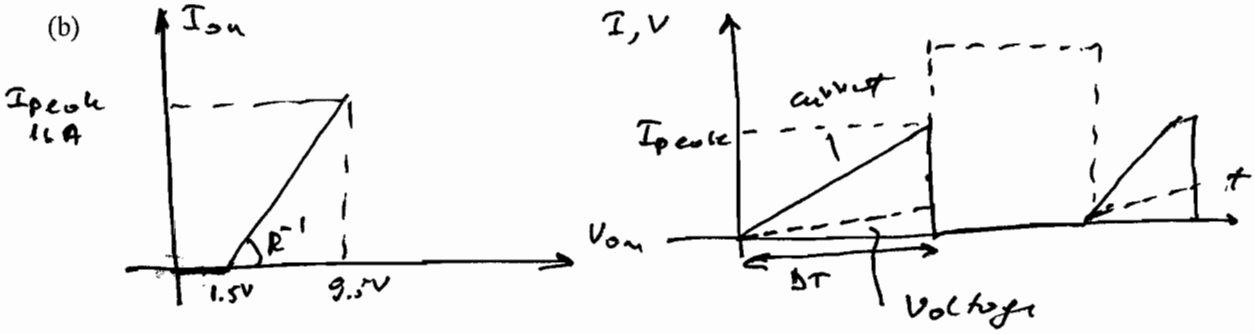
The Punch-through (PT) high voltage diode is a based on a PIN diode where the thickness (length) of the lowly doped layer (n- or p-) is smaller than the depletion region thickness (length) at breakdown. Thus the depletion region reaches the n+ cathode region before avalanche breakdown takes place.



- For the MOSFET the NPT design is more appropriate. Although the drift length is shorter in the PT design, the NPT offers higher doping for the same breakdown voltage. The ratio between the doping and length of the drift region is higher in the NPT than in the PT design leading to smaller on-state drift resistance in the NPT case.

[30%]

(b)



$$P_{on} = \frac{1}{T}\int_0^{\Delta T} VI\,dt = \frac{1}{T}\int_0^{\Delta T} \alpha \cdot t\,[V_{offset} + R\alpha t]\,dt$$

where α is the ramp of the current growth in time

$$\alpha = \frac{I_{peak}}{\Delta T}$$

$$P_{on} = \int_0^{\Delta T} \frac{I_{peak}}{\Delta T} V_{offset}\, t\,dt + \int_0^{\Delta T} \left(\frac{I_{peak}}{\Delta T}\right)^2 \cdot R\, t^2\,dt$$

$$= \frac{I_{peak} \cdot V_{offset}}{2}\Delta + \frac{I_{peak}^2 R}{3}\Delta =$$

$$= \frac{16 \cdot 1.5}{2}\cdot\frac{1}{2} + \frac{16^2 \cdot \frac{1}{2}}{3}\cdot\frac{1}{2} = \underline{\underline{27.33\,W}}$$

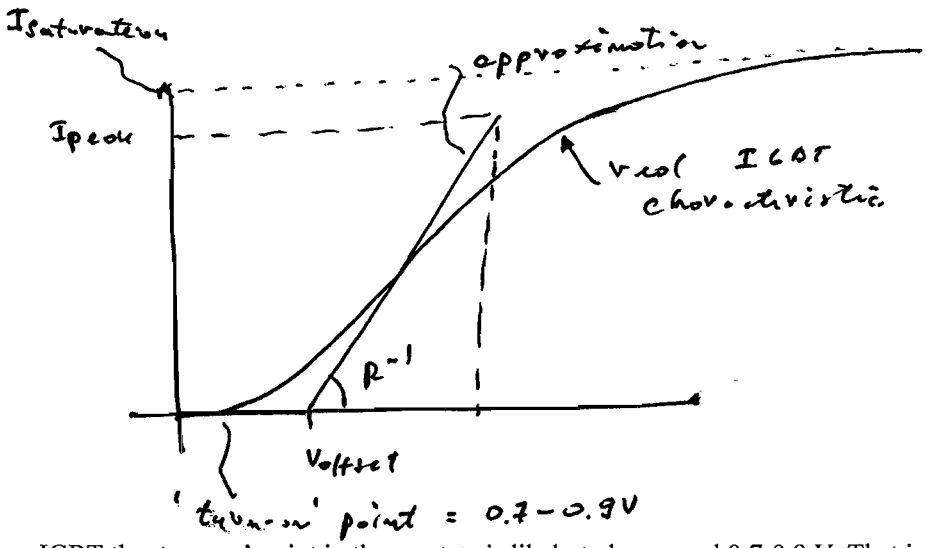
[30%]

$P_{turn-off} = E \cdot f = 3 \cdot 10^{-3} \cdot 50 \cdot 10^3 = 150\,W$

The switching losses are much higher than the on-state losses indicating that the switching frequency is too high.

f should be around $\underline{\underline{10\,kHz}}$ for a more balanced system

[20%]

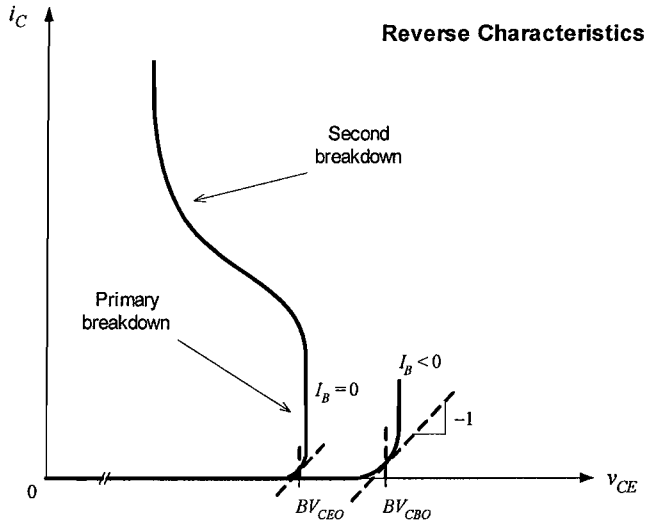


In an IGBT the turn-on' point in the on-state is likely to be around 0.7-0.9 V. That is ssmaller than Voffset which is 1.5 V. So at low currents, the approximation is likely to overestimate the voltage drop on the IGBT. The approximation is based on a linear increase in the current with the voltage beyond the offset voltage. In reality, as the device heads towards the saturation, the characteristics become sub-linear and the approximations is likely to underestimate the voltage drop on the IGBT. We also make the assumpations that the peak current Ipeak is greter than the saturation current.

So if the SMPS peak on-state current is much lower, when compared to the saturation current of the IGBT, it is most likely that the approximation will overestimate the on-state voltage drop in the IGBT. A practical device would therefore have lower on-state losses than those predicted by using eq. 1.

On the opposite, if the peak current is close to the saturation current of the IGBT the approximation will underestimate the on-state voltage drop in the IGBT. A practical device would therefore have much higher on-state losses than those predicted by using eq. 1. [2 0/3]

2. (a)

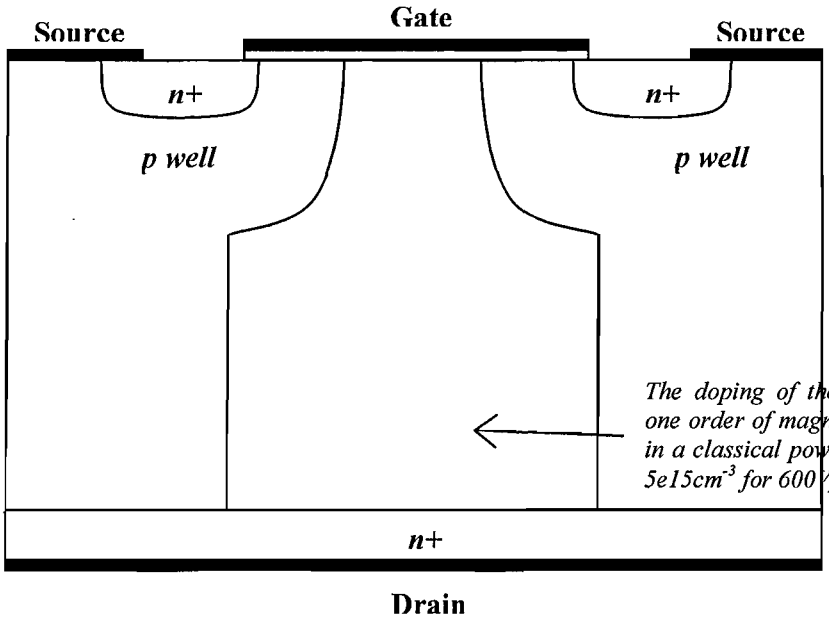


- ***Second breakdown*** is characterized by a snap-back in the breakdown characteristics. Second breakdown appears at large currents and results in a fast drop in the collector-emitter voltage. As the current increases, the temperature increases. If the temperature increases the injection is stronger and the current increases again. Hence BJTs suffer from a positive current-temperature feedback. This is known as *thermal runaway.* The thermal runaway is usually a local effect and leads to creation of hotspots.

[30%]

(b) The superjunction effect is based on multiple junctions disposed in the drift region with alternate layers of relatively highly doped n and p layers. The drift region is therefore made of thin n/p stripes rather than a single n- layer. The depletion of the drift region is in this case dictated by these n/p multiple junctions rather than by the classical p+/n- junction. Since the stripes are very thin (compared to their length), they deplete at much lower voltage (due to the extension of the depletion region across the n/p junctions). The net advantage is a major reduction in the on-state resistance for the same breakdown capability.

The Cool MOS is shown below:

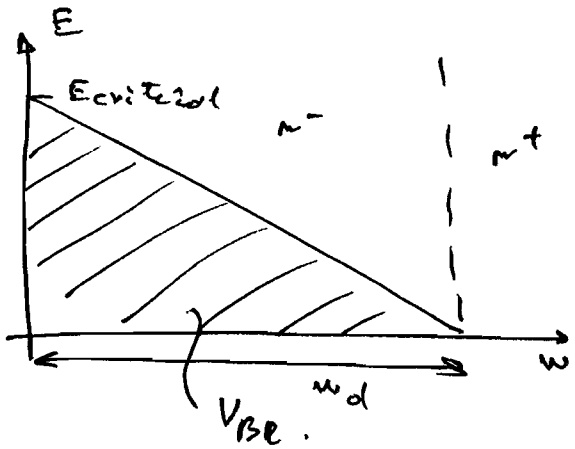


The Cool MOS is base on superjunction effect. The on-state conduction area is limited to the n-stripe, but its doping is around one order of magnitude higher than in a classical MOSFET, leading to a factor of 5 reduction in the on-state resistance.

- The device has a limited breakdown range (300 – 1 kV), because at very low voltages, the channel resistance tends to dominate the overall resistance. A trench solution at such voltages would be more appropriate. At higher voltages (above 1 KV), IGBTs, tend to be more efficient in terms of performance and cost. Also above 1 kV, the technological implementation of the n/p pillars in the drift region becomes extremely difficult.

[30%]

(c) To minimize the on-state resistance an NPT design should be used with the electric field at breakdown should just 'touch' the n+ drain contact region. Therefore the drift width W_d should equate $W_{critical}$.



$W_d = W_{critical}$

$$V_{BR} = \frac{E_{critical} \cdot W_d}{2} \qquad (1)$$

but $W_d = \sqrt{\frac{2 \varepsilon_0 \varepsilon_r V_{BR}}{q N_D}}$ replace W_d in (1) and calculate V_{BR}^2

$$\Rightarrow V_{BR} = \frac{E_{critical}^2}{2} \cdot \frac{\varepsilon_0 \varepsilon_r}{q N_D} \qquad (2)$$

but $R_{specific} = \frac{W_d}{q \mu_n N_D} = \frac{2 V_{BR}}{E_{critical} \cdot q \mu_n N_D}$

$$\Rightarrow q N_D = \frac{2 V_{BR}}{E_{critical} \mu_n \cdot R_{specific}}$$ replace in (2)

$$\Rightarrow V_{BR}^2 = \frac{E_{critical}^2}{4} \cdot \varepsilon_0 \varepsilon_r \mu_n R_{specific}$$

$$\Rightarrow R_{specific} = \frac{4 V_{BR}^2}{E_{critical}^3} \cdot \frac{1}{\varepsilon_0 \varepsilon_r \mu_n}$$

$$\left| \frac{R_{specific\ SiC} - R_{specific\ Si}}{R_{specific\ Si}} \right| = \left| \frac{E_{Si}^3}{E_{SiC}^3} \cdot \frac{\varepsilon_{r\,Si}}{\varepsilon_{r\,SiC}} \cdot \frac{\mu_{n\,Si}}{\mu_{n\,SiC}} - 1 \right|$$

$$= \left| \left(\frac{0.3}{2} \right)^3 \cdot \frac{12}{9} \cdot \frac{1200}{800} - 1 \right| = 99.325\% \qquad [40\%]$$

This is equivalent to say that

$$R_{Si} = 148\, R_{SiC}$$

3. (a) The dI_F/dt condition appears during the turn-on of the thyrsitor. If the rise time is too short (dI_F/dt is too high), the plasma cannot spread fast enough from the edge of the cathode (in the proximity of the gates) to the middle of the cathode. Therefore during the risetime the device conduction is limited to a small area around the edge (compared to the cross-sectional area of the device) and the voltage cannot fall quickly enough. Hence, large instantaneous power dissipation occurs during this period of time which leads to hot spot formation followed by thermal runaway and eventually permanent failure.

Two ways to improve this:

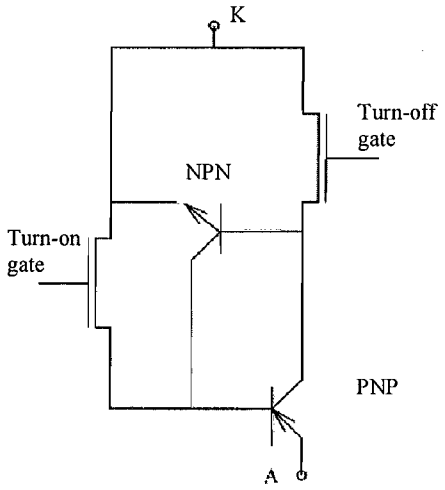
- increase the density of gates per total area – that is to say that we increase the density of gate-cathode inderdigitation. This also has the advantage of shortening the turn-off time (as well as the turn-on time).
- use a smaller auxiliary or pilot thyristor integrated on the same silicon chip with the main thyristor. The current injected into the gate of the pilot thyristor is relatively small but this is amplified by the pilot thyristor so that the gate current delivered to the main thyristor is relatively high

[30%]

(b) The MCT has a very low on-state resistance, similar to that of GTO thyristors.

- In comparison with the GTO thyristor, the MCT can be turned on and off using a high input impedance MOS gate.
- In the off-state the device behaves similarly to a thyristor with most of the voltage supported across the n- drift region. As with the thyristors, the device breaks when the sum of the current gains of the NPN transistor and PNP transistor reaches 1.
- The device is turned on by applying a positive voltage on the gate, thus allowing injection of electrons into the n- base.
- The current flow in the on-state occurs through the two coupled bipolar transistors (as shown on the equivalent circuit). As a result of high conductivity modulation specific to thyristor structures, the n- base resistance is reduced significantly.
- The turn-off of the MCT is achieved by short-circuiting the base (p base) -emitter (n+ cathode) junction of the NPN transistor (component of the thyristor structure) through a pMOS channel. To accomplish forced gate turn-off, the p-channel resistance should be so low as, when all the hole current is diverted via the p-channel MOS structure, the forward-bias of the n+ cathode/p base junction to remain below 0.5 V (the threshold voltage of the junction). However, due to non-uniform current distribution from cell to cell, hot-spot formation and the significant reduction of the cathode junction threshold voltage at high temperatures, the maximum controllable current density that satisfies the above condition is very low.

[30%]



[30%]

Compared to IGBT

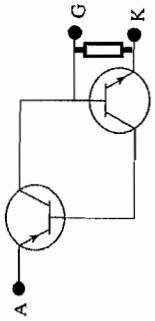
Advantage: The MCT offers lower on-state resistance – characteristic to thyristors (heavy injection of plasma from both sides of the drift region)

Disadvantages:

- Complex structure & high cost
- Filamentation effect. Negative temperature coefficient can lead to hotspot formations
- No on-state control of the current (no MOS current saturation)
- Lower breakdown voltage for the same doping and drift length compared to an IGBT (the device breaks via breakover mechanism rather than avalanche)

[10%]

4. (a) The turn-off process is based applying a reverse-baised voltage set by an external circuit for a minimum period of time. Initially the currents starts to decrease, but plasma is still present in the dvice (as this may take a long time to clear). The current becomes negative, while the plasma is decaying. At the end of this period, the plasma is removed allowing a depletion region to be formed. The reverse voltage is now fully applied to the device, while the negative current starts to decrease to zero. After the current is completely zero, a forward blocking voltage can be applied with a dV/dt ramp. The ramps should be carefully chosen as this introduces a displacement current C depl dV/dt. If this current is greater than the breakdover current, the transistor turns-on again (fails to turn-off).



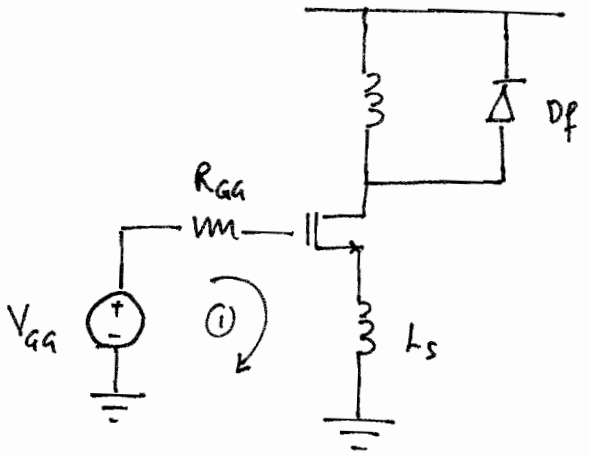
Equivalent circuit of a thyristor with cathode shorts.

To minimise the effect of the displacement current cathode-shorts or anode-shorts can be introduced. These shorts lower the current gains of the NPN and PNP transistor respectively, increasing the breakover current and absorbing some of the un-wanted displacement currents. The equivalent circuit of the thyristor showing cathode-shorts is given below, where a resistance is placed between the emitter and the base of the NPN transistor.:

For anode shorts the equivalent circuit is similar, with the short resistance placed between the anode and the base

[30%]

(b)



Given no transfer capacitance,

$$C_{iss} = C_{GS} = 120\,nF$$

$$\therefore i_G = C_{GS}\frac{dV_{GS}}{dt}$$

and $i_D = g_m V_{GS}$

Along loop ①,

$$V_{GG} = i_G R_{GG} + V_{GS} + L_S\frac{di_S}{dt}$$

$$= i_G R_{GG} + V_{GS} + L_S\frac{d}{dt}(i_D + i_G)$$

$$= C_{GS}R_{GG}\frac{dV_{GS}}{dt} + V_{GS} + L_S\frac{d}{dt}\left\{g_m V_{GS} + C_{GS}\frac{dV_{GS}}{dt}\right\}$$

$$= V_{GS} + \frac{dV_{GS}}{dt}\left\{R_{GG}C_{GS} + g_m L_S\right\} + \frac{d^2V_{GS}}{dt^2}L_S C_{GS}$$

Taking Laplace,

$$\frac{V_{GS}}{s} = V_{GS}\left\{1 + (R_{GG}C_{GS} + g_m L_S)s + L_S C_{GS}s^2\right\}$$

$$\Rightarrow V_{GS} = \frac{V_{GG}}{s\left\{1 + (R_{GG}C_{GS} + g_m L_S)s + L_S C_{GS}s^2\right\}}$$

$$= \frac{V_{GG}}{s\left(s + \frac{1}{\tau_1}\right)\left(s + \frac{1}{\tau_2}\right)} \quad \text{——— (*)}$$

$R_{GG}C_{GS} = 3.3 \times 120n = 396n$

$g_m L_S = 600 \times 2n = 1200n$

$L_S C_{GS} = 2n \times 120n = 240n^2$

Solving for τ_1 and τ_2,

$$\tau_1, \tau_2 = -\left[\frac{-1596n \pm \sqrt{(1596n)^2 - 4(240n^2)}}{2(240n^2)}\right]^{-1}$$

$$= 1595.8\,ns,\ 0.150\,ns \quad \text{(0.150 ns: too small!)}$$

Hence, taking the inverse laplace on (*) $\Rightarrow V_{GS}(t) = V_{GG}\left[1 - \exp\left(-\frac{t}{\tau_1}\right)\right]$.

[4.9]

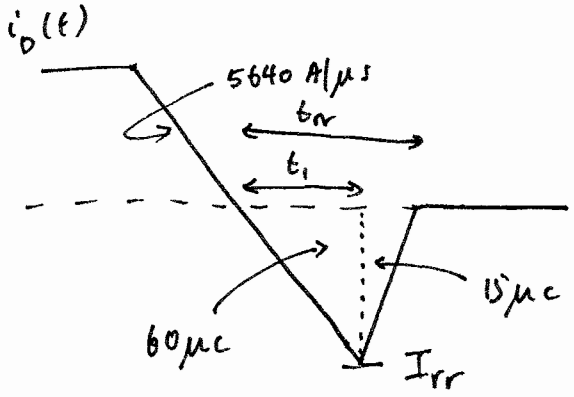
Hence, $i_D(t) = g_m V_{gs}(t)$

$= g_m V_{aa}\left[1 - \exp\left(-\frac{t}{\tau_1}\right)\right]$.

$\Rightarrow \frac{di_D(t)}{dt} = \frac{g_m V_{aa}}{\tau_1} \exp\left(-\frac{t}{\tau_1}\right)$. [10%]

At $t = 0$, initial decrease in current:

$$\left.\frac{di_D(t)}{dt}\right|_{t=0} = \frac{(600S)(15V)}{(1595.8ns)} = 5640\ A/\mu s.$$



Approximating $\frac{di_D(t)}{dt}$ to be linear,

$$\int_0^{t_1} \left.\frac{di_D(t)}{dt}\right|_{t=0} \cdot t\, dt = 60\mu c$$

$$\therefore t_1 = \sqrt{\frac{2 \times 60\mu c}{5640\ A/\mu s}}$$

$= 145.9ns$

Assuming linearity,

$$t_{rr} = \frac{2 \times 15\mu c}{823A} + t_1$$

$= 182.4\ ns$

$$\Rightarrow I_{rr} = \left.\frac{di_D(t)}{dt}\right|_{t=0} \cdot t_1$$

$= 5640\ A/\mu s \cdot 145.9\ ns$

$= 823\ A$ [20%]
