2007 IIB 4B8 Dr K Teo
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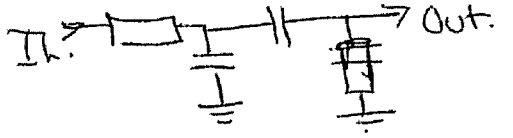
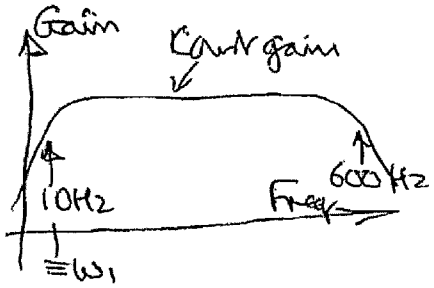
4B8 Cribs, 2007

1. (a) Made of 2 stages – a low pass filter first, then a high pass one — response as shown – with R-C elements, it would be:

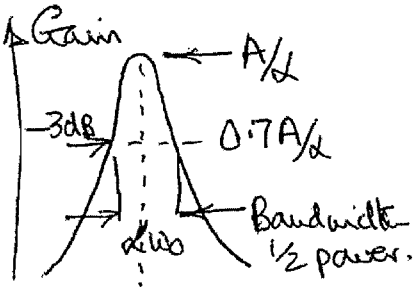




Main purpose would be to limit instrumentation bandwidth to help improve signal/noise ratio and remove aliasing if signals sampled. **15%**

———— // ————

(b). Using $s = j\omega$, $\frac{v_2}{v_1} = \frac{A j\omega\omega_0}{-\omega^2 + \alpha j\omega\omega_0 + \omega_0^2} = \frac{A}{\alpha + j\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}$



$= A/\alpha$ = Peak gain when $\omega = \omega_0$

When ω higher or lower than ω_0, the denominator increases so gain drops.

———— // ———— **15%**

(c) Signal at junction of R_1 and C_1 is v_x where

⊛ Top Op-Amp: $v_2/R_7 + v_x \cdot j\omega C_1 = 0$ or $V_x = -v_2/sC_1R_7$

Signal at junction of R_3 and R_6 is v_y and is given by

⊛ Right-Hand Op Amp: $v_y/R_6 + v_2 \cdot j\omega C_2 = 0$ or $V_y = -v_2 \cdot sC_2R_6$

Signal at junction of R_2 and R_5, by Potential Divider, is V_w where $V_w = \frac{R_5}{R_5+R_2} \cdot V_2$.

Note ⊛ For ideal op Amp, $A \to \infty$, $v_{in} \to 0$ so KCL at input gives these relations.

(Cont'd

So KCL at inverting input to Left hand Op Amp gives:-

$$\frac{V_1 - V_W}{R_4} + \frac{V_X - V_W}{R_1} + \frac{V_Y - V_W}{R_3} = 0$$

So $$\frac{V_1}{R_4} = \frac{V_2}{s C_1 R_7 R_1} + V_2 \cdot \frac{s C_2 R_6}{R_3} + V_2 \cdot \frac{R_5}{R_5 + R_2}\left(\frac{1}{R_4} + \frac{1}{R_1} + \frac{1}{R_3}\right)$$

or $$V_1 \cdot \frac{s C_1 R_7 R_1}{R_4} = V_2\left(1 + \frac{R_5}{(R_5+R_2)}\left(\frac{1}{R_4} + \frac{1}{R_1} + \frac{1}{R_3}\right) \cdot s C_1 R_7 R_1 + s^2 \cdot \frac{C_2 C_1 R_6 R_7 R_1}{R_3}\right) \quad (A)$$

Comparing this to $V_1 A s \omega_0 = V_2\left(s^2 + s\omega_0\alpha + \omega_0^2\right)$ which we desire, the s^2 term shows us all needs $\div \frac{C_2 C_1 R_6 R_7 R_1}{R_3}$ in equation (A) to make them identical.

So Left hand side gives $A\omega_0 = \frac{s C_1 R_7 R_1}{R_4} \cdot \frac{R_3}{C_2 C_1 R_6 R_7 R_1} = \frac{R_3}{C_2 R_4 R_6}$

$$= R_3 / C_2 R_4 R_6 \quad \text{—— (1)}$$

s term gives $\alpha\omega_0 = \frac{R_5}{R_5 + R_2}\left(\frac{1}{R_4} + \frac{1}{R_1} + \frac{1}{R_3}\right) \cdot s C_1 R_7 R_1 \cdot \frac{R_3}{C_2 C_1 R_6 R_7 R_1}$

$$= \frac{R_5 R_3 \cdot \left(\frac{1}{R_4} + \frac{1}{R_1} + \frac{1}{R_3}\right)}{(R_5 + R_2) R_6 C_2} \quad \text{—— (2)}$$

And $$\omega_0^2 = \frac{R_3}{C_2 C_1 R_6 R_7 R_1} \quad \text{—— (3)}.$$

45%

(cont'd)

(d). When $C_2 = C_1 = 10^{-8}$

$R_1 = 10^5$ $R_3 = 10^4$, and for $R_6 = R_7$.

equation (3):- $R_6 = R_7 = \sqrt{\frac{10^4}{10^5}} \cdot \frac{1}{C\omega_0} = \frac{\sqrt{0.1} \cdot 10^8}{2\pi \times 200}$

$= \underline{25.16\ k\Omega}$.

Now Peak Gain $= A/\alpha = 50$, so $A = 50\alpha$.

So $A\omega_0 = 50\alpha\omega_0 = 50 \times 10 \times 2\pi$ rad/sec { 10Hz Bandwidth

$= R_3/C_2 R_6 R_4 = \frac{10^4}{10^{-8} \cdot 25.16k \cdot R_4}$ { Eqn (1).

So $R_4 = \frac{10^{12}}{25.16 \times 10^3 \times 1000\pi} = \underline{12.68k\Omega}$

Also Bandwidth $= \alpha\omega_0 = 2\pi \times 10$

$= R_3 R_5 \left(\frac{1}{R_4} + \frac{1}{R_1} + \frac{1}{R_3}\right) / 10^{-8} \cdot R_6 (R_5 + R_2)$.

$= 10^4 \cdot R_5 \left(\frac{1}{25.16k} + 10^{-5} + 10^{-4}\right) / 10^{-8} \cdot 25.16k (R_5 + 10^5)$.

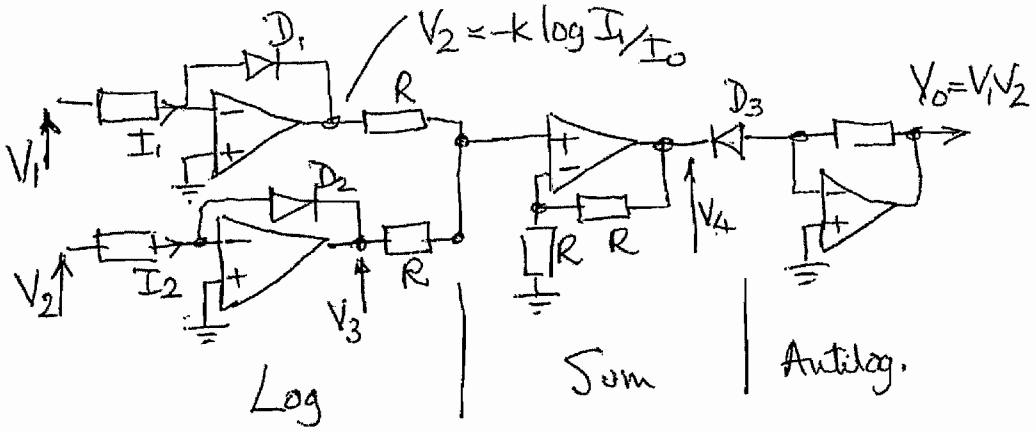
α gives $0.01581 (R_5 + 10^5) = 1.888 R_5$.

or $1.8727 R_5 = 1.581 \times 10^3 \Rightarrow \underline{R_5 = 844.2\Omega}$

(These values in a PSpice program all checked). **25%**

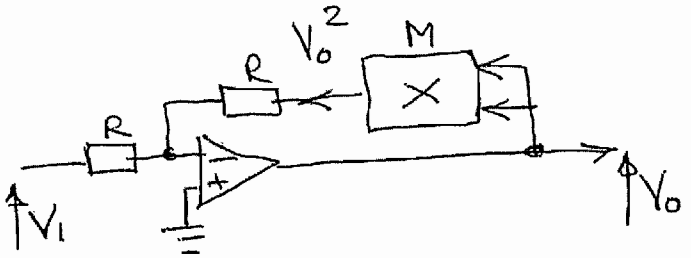
2.

a) Outline Circuit is :-



The input diodes D_1 and D_2 have to be put into conduction so that V_1 and V_2 must be ⊕ polarity. Input opamps invert. The summing circuit does not invert but has an input $\frac{V_2+V_3}{2}$ and has a gain of X2 so the output is V_2+V_3 – the sum of two log expressions. These will both be of ⊖ polarity. The diode D_3 will conduct for ⊖ inputs V_4 and gives an antilog function when as shown. **25%**

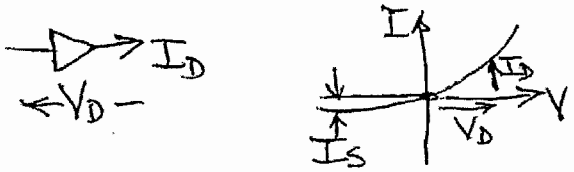
b). Arrangement is :-



Here the multiplier block has an output V_0^2 with both its inputs joined to any voltage V_0 developed. Then KCL at input stage gives $V_1/R + V_0^2/R = 0$ for a high gain amp. Or $V_0 = \sqrt{-V_1}$

The inputs must be ⊖ polarity. **10%**

c) Shockleys equation for a diode $I_D = I_S(\exp \frac{qV_D}{KT} - 1)$



Where Is is the reverse saturation current of the junction (contd)

c) contd Now when $V_D = 0.1V$, $e^{V_{DQ}/KT} \neq 54.6$. $= e^4$

So only with $V_D \geq 0.1V$ will the unity in the equation be under 2% of the exponential term — and so can be ignored.

Then $\frac{I_D}{I_S} = \exp \frac{V_D}{26\times10^{-3}} \log_e I_D/I_S$

So $V_D = 26\times10^{-3} \log_e \frac{I_D}{I_S} = \underbrace{26\times10^{-3} \times 2.302}_{.05987} \left(\log_{10} I_D - \log_{10} I_S\right)$

Constant term "nulled" if temp constant

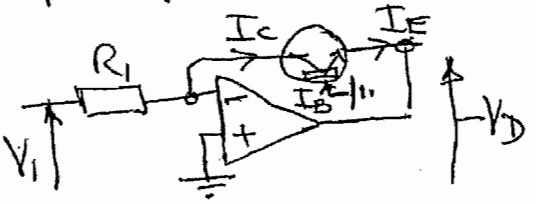
So circuit errors from log when :-

(1) $V_D \geq 0.1V$ AND

(1,) when $I_D <$ 1.0mA. At high junction currents, the bulk resistance of the rest of the p and n regions limit the V_D against I_D to the linear one of a resistor.

25%

d). The best circuit to null the Is term is a similar junction at a similar temperature. Matched transistors, closely mounted to each other in a small integrated circuit in one package are available for amplifier input stages.



A transistor is joined as shown. Then The Base Voltage is 0V, Collector Voltage is Virtual Earth,

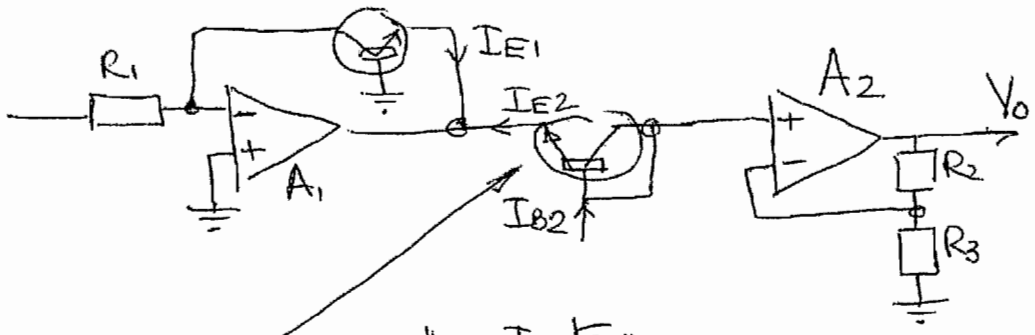
and so are almost identical.

Now I_E = junction current $\neq I_B + I_C = V_1/R_1\left(\frac{1}{h_{FE}} + 1\right) \rightarrow V_1/R_1$

So with $h_{FE} = 300$, the error will be only 1/3% and will give the desired low error condition.

20%

e)



Second transistor NULLS the Is term.
I_{B2} is set so I_{E2} is mid range value of I_{E1}.

Non inverting amplifier A_2 must have $R_2+R_3 > 10k\Omega$ for low loading requirements. Now we desire:-

$$V_o \propto 2 \times \log_{10} V_1$$

Gain of A_2 stage.

$$= \left(\frac{R_2+R_3}{R_3}\right) \times 0.05987.$$

$$\text{So } \frac{R_2+R_3}{R_3} = \frac{R_2}{R_3} + 1 = 2/0.05987 = 33.40$$

$$\text{So } R_2/R_3 = 32.40 \longleftarrow = \frac{324}{10} = \frac{3240}{100}$$

$$= \frac{9.72K}{300} \text{ or } \frac{10.7K}{330}$$

So by choosing R_3 as preferred value = 330 we would make up circuit as

R_2 { 1K pot TRIM, 10K 10K fixed

330 = R_3

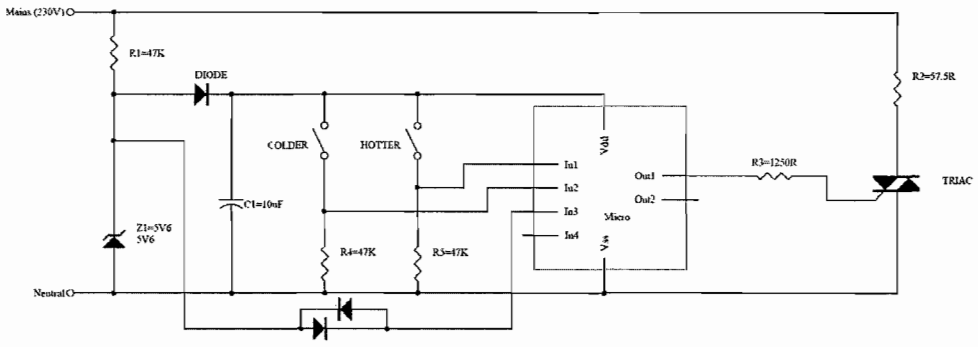
20%

3. a) Polling = "Sequence-based" programming. **[5%]**
Interrupt = "Event-based" programming. **[5%]**

Polling programs are easier to read. However, the main program is dedicated to checking inputs and cannot be used for other tasks, and hence cpu usage is inefficient. **[5%]**

Interrupt programs are more efficient as inputs generate interrupts which run service routines, leaving the main program for other tasks. However, interrupt-based programs are more difficult to read. **[5%]**

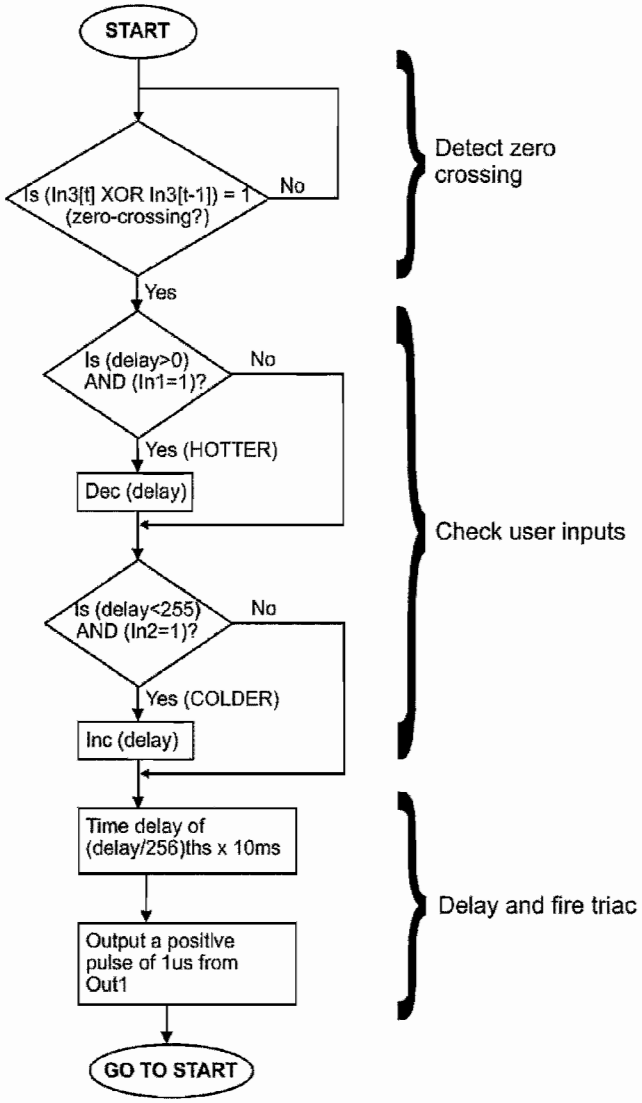
b)



[10%] for power supply for microcontroller. Choose Z1=5.6V to give a 5V Vdd after the diode. At worst case, this circuit must deliver 2.4mA (=2mA for triac+0.4mA for micro). Since it is a half wave rectifier, assume we need 4.8mA to supply enough current through R1 to power the micro+triac combo.
So R = V/I = (230-5.6)/4.8mA = 47K
[10%] for triac, load ($R=V^2/R=230^2/600=57.5\Omega$) and calculation of its drive resistor ($R=V/I=2.5/0.002=1250\Omega$).
[10%] for zero crossing circuit. At the 5V6 zener, we see a 'square wave' with 5.6V and -0.6V. The 2 diodes remove the 0.6V overvoltages and In3 essentially sees a 'square' wave of peak voltages of 5V and 0V.
[10%] for 2 user inputs – check that R4/R5 are reasonably large so as not to overload the power supply.

c) **[10%]** for detecting zero crossing part of flow diagram
[10%] for checking inputs
[10%] for delay and firing the triac
See next page

Anything reasonable along the lines of:



Note that for more heat, the delay is decreased (DEC)!

d) The watchdog timer is a timer which checks that the main program has not crashed. It is reset in every loop of the program. If it times out, the micro reboots. For 50Hz, the program cycle is 100Hz since there are 2 zero crossings. So the minimum period is 10ms. If a different implementation to the above is used for question (c), then the minimum period is one cycle of the main program. **[10%]**

4. a) The acquisition time is determined by the charge up time of the RC circuit formed by the resistance of the switch and the hold capacitor, plus the switch delay when an input channel is selected.

Delay of the RC circuit first:

$V = V_{in} (1 - e^{-t/RC})$

For 0.1% accuracy, V/Vin = 0.999

$0.999 = 1 - e^{-t/(10e\text{-}9 \times 40)}$
$\ln (0.001) = -t/(10e\text{-}9 \times 40)$
$-6.91 = -t / 4e\text{-}7$
$t = 2.76\mu s$

Total delay = 2.76 + 0.25μs = 3.01μs

[10%]

b) The hold step voltage is due to the switch injecting charge onto the capacitor.

Q = CV
V = Q/C
= 20 pC / 10nF
= 2 mV

[5%]

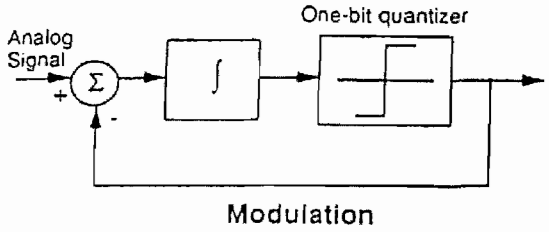
c) The droop rate is due to leakage current of the switch and the OP27.

Total leakage = 1 + 10 = 11nA
i = C dV/dt
11nA = 10nF (dV/dt)
Droop rate = dV/dt = 1.1V/sec

½ LSB voltage = ½ x $1/2^{16}$ x 5V = 38μV
Max conversion time = 38μV / 1.1
= 35μs

[15%]

d)



Modulation

[10%]

Subtractor	Integrator	Quantiser
=analog(t)-quantiser(t-1)	=subtractor(t)+integrator(t-1)	=level '1' if integrator > 0
		=level '0' if integrator < 0

[15%]

e)

Time	Input	Subtractor	Integrator	Quantiser
0	2	0	0	0
1	2	2	2	5
2	2	-3	-1	0
3	2	2	1	5
4	2	-3	-2	0
5	2	2	0	0

Bitstream = 1 0 1 0 0

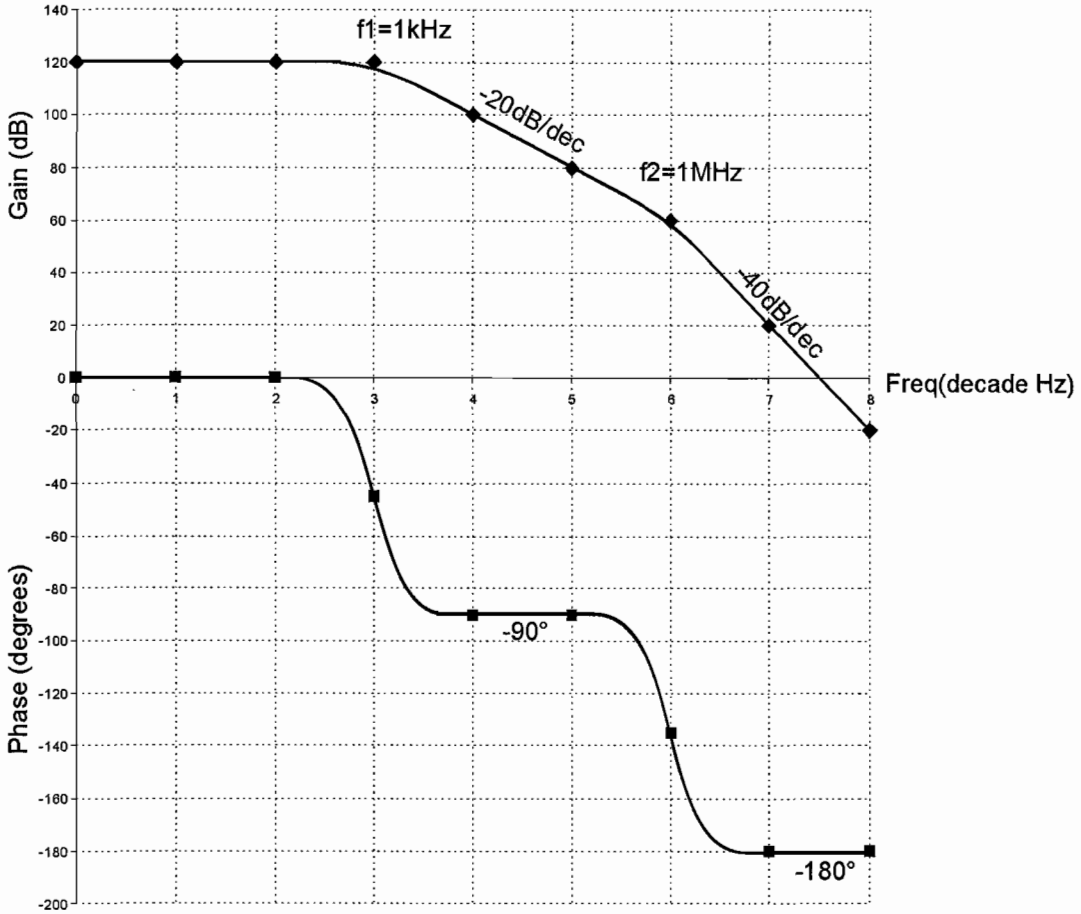
[35%]

f) Analog signal = Average of (5+5+0+0+0) = 2V

Any R-C / averaging circuit would be acceptable here.

[10%]

5. a) Any sketch that resembles:



b) $\omega_1 = 2\,\pi\,f_1 = 6283$ rad/s $\quad \omega_2 = 2\,\pi\,f_2 = 6283000$ rad/s

$A_0 = 10^6 \qquad \beta = 1/(1+399) = 0.0025$

$$\omega_n = \left[\omega_1\omega_2\left(1+\beta A_O\right)\right]^{1/2} = 9.94 \text{ rad/s}$$

$$k = \frac{\omega_1 + \omega_2}{2\omega_n} = 0.316$$

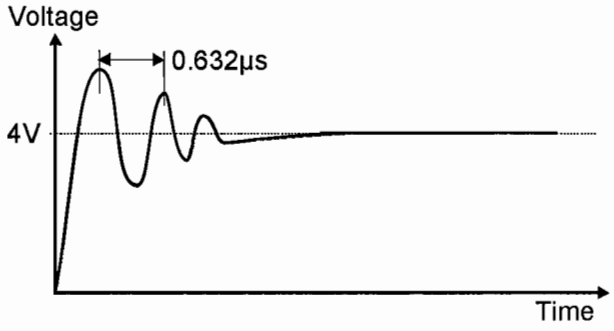
Since $k < 1$, it is underdamped.

c) $A_{of} = \dfrac{A_O}{1+\beta A_O} = 400 = 52\text{dB}$

So Vout = Vin x A_{of} = 0.01 x 400 = 4V

$f_n = \dfrac{\omega_n}{2\pi} = 1.58\,\text{MHz}$

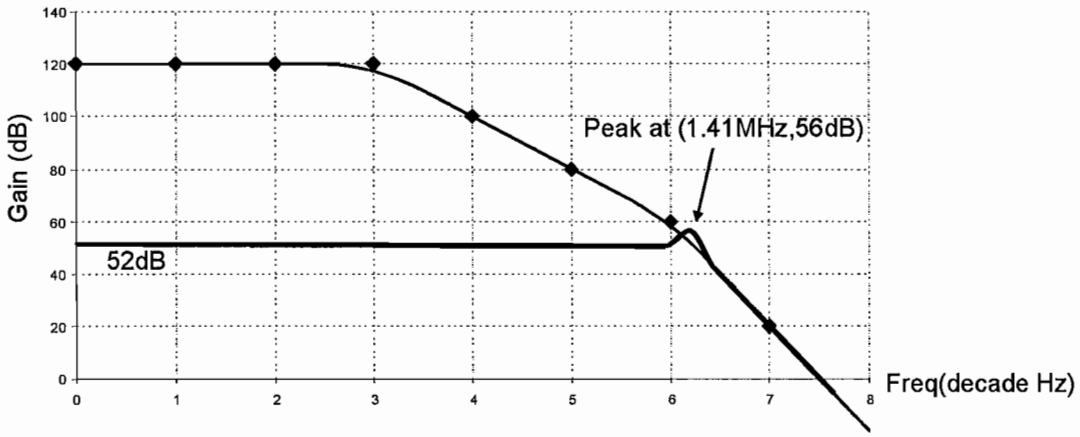
So period of underdamped oscillations = 1/1.58MHz = 0.632μs



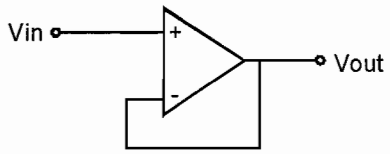
d)

Max occurs at: $\omega = \omega_n\left(1-2k^2\right)^{1/2} = 8.89\text{Mrad/s} = 1.41\text{MHz}$

Peak gain: $\left|A_{peak}\right| = \dfrac{\left|A_{of}\right|}{\left\{2k\left(1-k^2\right)^{1/2}\right\}} = 666 = 56\text{dB}$

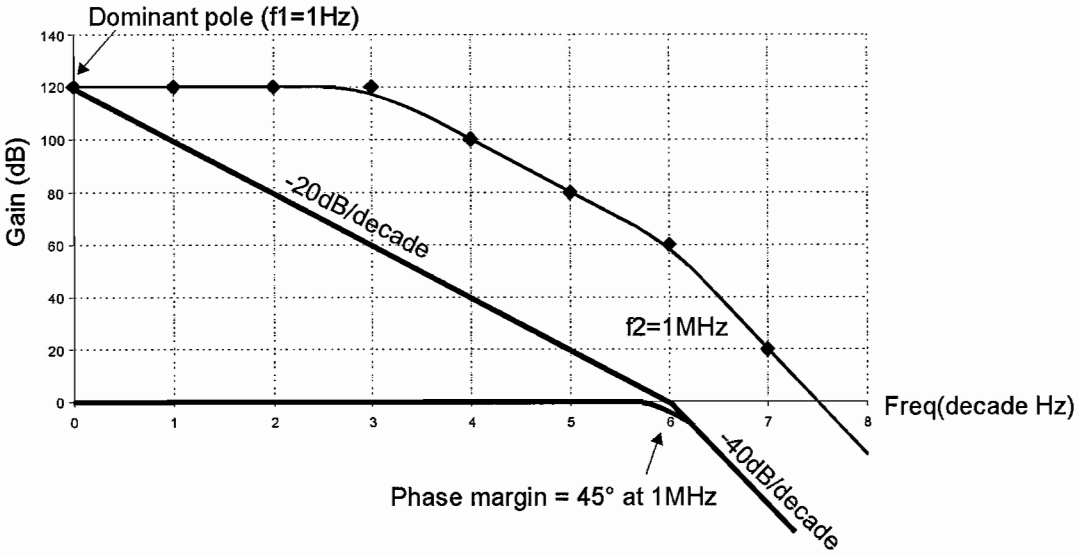


e)



Require second pole, 1MHz at gain = 0dB, to achieve a phase shift -135° or 45° margin.
Hence, to reach 120dB (op-amp gain at dc), we need to go backwards at 20dB/decade, and hence 6 decades to the first pole.
So first pole (dominant) must be 1Hz (ie. 6 decodes back from 1MHz).

f)



Gain bandwidth = 1Hz x 10^6 = 10^6 Hz

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Peter Spreadbury
2007