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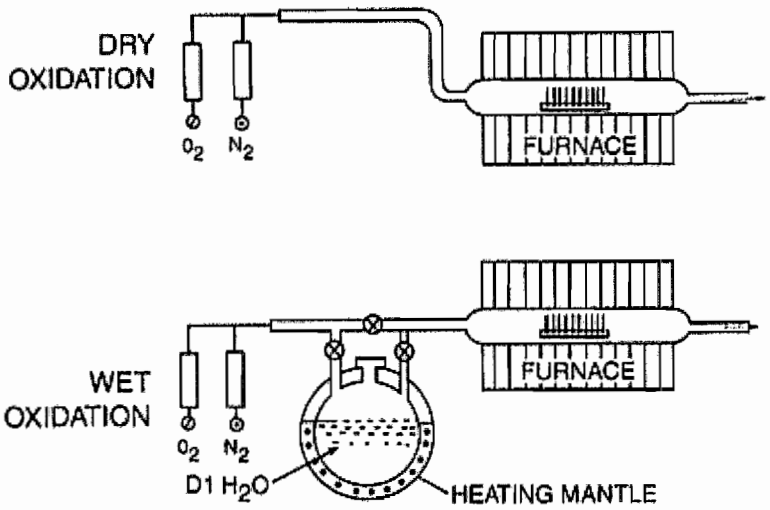
1 (a) For the special case of silicon oxide formation on crystalline silicon, thermal oxidation may be used to produce an oxide of exceptionally high quality. In dry oxidation, the silicon wafer is heated in a furnace at atmospheric pressure in an atmosphere of nitrogen and oxygen at a temperature between 700° and 1250° C. The high temperature aids the diffusion of oxygen into the silicon bulk where a reaction takes place of the form

$$Si + O_2 \rightarrow SiO_2$$

In the case of wet oxidation, the O_2/N_2 gas mixture is bubbled through a simmering water bath to add steam to the mixture. This changes the reaction to

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

and a faster oxidation rate results. The silicon substrate is consumed in this reaction, and 460 nm of silicon is required to produce a 1000 nm thick silicon dioxide layer. [30%]



[10%]

(b) Silicon oxide is an important material for producing free-standing silicon microstructures as it has a very high etch rate in hydrofluoric acid (HF) compared to that of silicon. Therefore, a silicon structure can be patterned on top of a layer of SiO_2, and immersed in HF to remove the underlying SiO_2. The following process flow illustrates this: [15%]

Step No	Code	Description
1	HFD1	HF dip of the SOI wafer to remove the native surface oxide layer and clean the SOI wafer.
2	PHO1	Spin a layer of photoresist onto the surface of the SOI wafer.
3	BAK1	Pre-bake the photoresist.
4	EXP1	Expose the photoresist through a mask to produce a pattern in the photoresist that is a positive image of the free-standing structure. Care must be taken to ensure that the support structure is large compared with the size of the features that must be undercut, as the HF etch is isotropic in SiO_2. The photoresist must be thick enough to ensure that the silicon etch (ETH1) does not completely remove the protecting photoresist.
5	DEV1	Develop the photoresist.

6	ETH1	Etch the exposed silicon using proprietary silicon etchant (HNO_3:HF:CH_3COOH) ensuring that all of the exposed silicon is removed, but avoiding undercutting of the silicon structure through over-etching.	
7	DIR1	DI water rinse	
8	ETH2	Etch the underlying SiO_2 using a buffered HF etch, ensuring sufficient time to fully undercut the silicon structures to be released, but avoiding overetching that would lead to undercutting of the support structure.	
9	DIR2	DI water rinse.	
10	IPA1	Isopropanol	
11	ACE1	Remove the photoresist and also reduce surface tension for drying.	
12	DRY1	Blow dry under nitrogen and bake.	[20%]

(c) The maximum cantilever length if there is always to be sufficient elastic restoring force is

$$s^{*4} = \frac{3Eh^3g^2}{2\gamma}$$

where E is the Young modulus, h is the cantilever thickness, γ is the surface energy and g is the gap between the cantilever and the substrate. Hence, g is given by

$$g = \sqrt{\frac{2\gamma s^{*4}}{3Eh^3}}$$

$$= \sqrt{\frac{2\times 0.1\times\left(100\times10^{-6}\right)^4}{3\times160\times10^9\times\left(1\times10^{-6}\right)^3}} \qquad [15\%]$$

$$\underline{g = 6.45\ \mu\text{m}}$$

where E is the value for polycrystalline silicon taken from the data book and assuming:

- that the Young modulus and not the plate modulus is appropriate.
- there are no residual stress gradients in the poly-Si.
- the system is in a dry environment.
- the poly-Si is homogeneous

[5% each; max 10%]

2 (a) The presence of thermal or intrinsic stress within these materials will cause deformation of the structure upon release from the substrate. Whilst such stresses can be tolerated in free-standing structures made from a single material if no stress gradient is present, in a bilayer structure, the difference in stress between the two layers will cause the whole structure to deform, and may even result in delamination in extreme cases. [20%]

(b) Thermal stresses are produced when a material is deposited at high temperature. The material contracts upon cooling, and this would normally not be a problem in its own right. However, if it is in contact with another material which contracts at a different rate, then the two materials will cause a stress to exist in each other, with the material that contracts less being under compressive stress and that which contracts more under tensile stress. [15%]

Other potential sources of intrinsic stress include:

- Impurities, such as dopant atoms can induce both compressive and tensile stress into the material. Atoms smaller than the host tend to induce tensile stress and vice versa.
- Atomic peening due to ion bombardment produces compressive stress.
- Microvoids in the material bulk produced during deposition yields tensile stress.
- Absorption of surface contaminants can effectively cause a new layer to form on the top of a material when its environment is changed. Water absorption and oxidation are two common situations.
- Grain boundaries, which contain a large number of defects are also a source of intrinsic stress in polycrystalline materials.
- Incorrect stoichiometry. In particular, SiN must be silicon rich to produce a low stress material. [5% each; max 20%]

(c) The process flow is as follows:

Step No	Code	Description
1	RCA1	Boil the silicon substrate in RCA Clean 1 ($NH_{3(aq)}$:H_2O:H_2O_2) to remove organic contaminants.
2	RCA2	Boil the silicon substrate in RCA Clean 2 (HCl:H_2O:H_2O_2) to remove metallic ion contaminants.
3	SIN1	LPCVD growth of the 300 nm thick SiN layer using a SiH_2Cl_2 gas mixture at a temperature of 800 °C. A low stress layer is required, and so in the absence of any thermal constraints, LPCVD is preferred, however, a silicon rich material should be deposited to minimise stress.
4	EVP1	Thermally evaporate the nickel this film. Care should be taken to avoid heating the sample to reduce the likelihood of thermal stresses existing between the SiN and Ni layers.
5	PHO1	Spin a layer of photoresist onto the surface of the sample wafer.
6	BAK1	Pre-bake the photoresist.
7	EXP1	Expose the photoresist through a mask to produce a pattern in the photoresist that is a positive image of the cantilever structure, and aligned to the (110) planes in the silicon wafer. The photoresist must be thick enough to ensure

		that the subsequent Ni and SiN etches do not completely remove the protecting photoresist.	
8	DEV1	Develop the photoresist.	
9	NIE1	Etch the nickel using a proprietary nickel wet etchant.	
10	DIW1	Rinse the sample in DI water.	
11	DRY1	Blow dry the sample under dry nitrogen.	
12	RIE1	Etch the silicon nitride by rf-RIE using a CF_4:O_2 gas mixture.	
13	RIE2	Expose the sample to a short O_2 rf-RIE plasma to remove any remaining polymer from the CF_4 plasma etch.	
14	KOH1	Etch the sample in a 25% KOH solution at 80 °C to undercut the structure.	
15	DIW2	Rinse the sample in DI water.	
16	IPA1	Rinse the sample in isopropanol.	
17	ACE1	Rinse the sample in acetone to minimise surface tension during drying.	
18	DRY2	Blow dry the sample under dry nitrogen.	[45%]

3 (a) (i) Process partitioning. Some elements rapidly diffuse through others, changing the material properties. It is for this reason that sodium, gold and copper are usually forbidden from entering a CMOS processing line, and therefore processes are normally partitioned into front-end processes (deposition, high temperature processing) which must be completed first, and back-end processes (interconnect formation and packaging) which are completed last. [10%]

(ii) Contamination constraints. It is normally the case that although samples can proceed from clean to less clean areas of a lab, reverse progression is rarely permitted. This can fix the order in which certain processes can be performed. [10%]

(iii) Wafer architecture. Not all points on a wafer are equivalent. There will always be some variation in photoresist thickness with position. Both dry and wet etches can vary in local rate as a function of pattern density (loading effect). Some areas of the wafer will be 'dead' due to sample handling. Therefore, the process (and particularly masks) must be designed to ensure that critical patterns are not placed in 'dead' areas and that the pattern density is fairly even across the wafer. [10%]

(iv) Packaging. The issue of how the device is to be finally packaged must be considered. Some die separation will almost certainly be necessary as will bonding of connectors onto the device. It may be necessary to package the device in vacuum or in a particular atmosphere (e.g. pressure sensors). On the other hand, some environmental access may actually be necessary, as is the case for biosensors, for example. [10%]

(b) (i) Process flow for production is as follows:

Step No	**Code**	**Description**
1	RCA1	Boil the silicon substrate in RCA Clean 1 ($NH_{3(aq)}$:H_2O:H_2O_2) to remove organic contaminants.
2	RCA2	Boil the silicon substrate in RCA Clean 2 (HCl:H_2O:H_2O_2) to remove metallic ion contaminants.
3	SOX1	Thermally oxidise the surface of the silicon wafer by heating to ~1000 °C in an atmosphere of O_2, N_2 and water vapour. A DRIE step will be use later in the process to etch the pillar structures. Typical selectivities of this process are ~100:1 and so a 3 μm thick layer of silicon oxide will suffice.
4	PHO1	Spin a layer of photoresist onto the surface of the sample wafer. This will be followed by an HF etch to remove the exposed oxide, and photoresist is generally not etched by HF, so a 1 μm thick layer will suffice.
5	BAK1	Pre-bake the photoresist.
6	EXP1	Expose the photoresist through a mask to produce a pattern in the photoresist that is a positive image of the pillar structure.
7	DEV1	Develop the photoresist.
8	HFD1	Etch the exposed silicon oxide in a buffered HF solution.
9	DRE1	Etch the exposed silicon in a deep reactive ion etch to produce the vertical trenches required to define the silicon pillars.

10	RIE1	Expose the sample to a high pressure oxygen plasma to remove any polymer on the sides of the pillars that would later impede the deposition of the copper thin film.	
11	ACE1	Dip the sample in acetone to remove any remaining photoresist.	
12	PHO2	Spin a layer of photoresist onto the surface of the sample wafer. This will be followed by an HF etch to remove the exposed oxide, and photoresist is generally not etched by HF, so a 1 μm thick layer will again suffice.	
13	BAK2	Pre-bake the photoresist.	
14	EXP2	Expose the photoresist through a second mask to leave photoresist everywhere except over the pillars. In practice, this should be a negative tone resist, and there should be a solid square pattern which sits over the pillars, although it should not extend over the whole square, as significant exposure will not occur within the trenches.	
15	DEV2	Develop the photoresist.	
16	HFD2	Etch the exposed silicon oxide in a buffered HF solution. This will remove the oxide on the surface of the pillars.	
17	IMP1	Use immersion plating to produce a thin film of copper onto the exposed silicon surface.	
18	ACE1	Dip the sample in acetone to remove any remaining photoresist.	
19	RIE2	Etch the remaining silicon oxide in a CF_4:H_2 plasma.	[50%]

(ii) As dimensions are reduced, the surface to volume ratio of structures becomes very large. Therefore, reaction rates are increased. Also, minimum amounts of the chemical required can be produced at the point of use. [5% each; max 10%]

4 (a) The act of pattern transfer onto a substrate by definition leads to a degree of surface roughness with some features standing proud of the surface. The addition of new layers on top of such a structure will tend to preserve at least some of this topography. Such roughness can lead to problems with bonding such surfaces and to errors in photolithography due to the presence of deep trenches which will tend to be underexposed. It also leads to the formation of stringers – material on a side wall which is not removed by a plasma etch. Therefore, it is sometimes necessary to planarise the surface to remove this roughness, and hence avoid these undesirable effects. [25%]

(b) (i) Chemical mechanical polishing. CMP is widely employed in the fabrication of both microsystem and microelectronic devices. It provides a means of planarising a surface by removing the top layers of material. A rotating platen is pressed against the surface to be planarised and a slurry injected between the two surfaces. The slurry contains both an abrasive and a chemical etchant, and the two act in tandem to produce a faster etch rate than either can achieve alone (faster even than the algebraic sum of the two processes) whilst yielding a very flat surface. This is an extremely useful process which can also be used to produce patterned structures. CMP does have its disadvantages. It uses very large quantities of slurry. There is an etch rate dependency on pattern density and material type. Dummy structures are frequently required to ensure a uniform etch over a whole surface. Also, large areas of a soft material surrounded by a harder material can 'dish' in which the centre of the soft region is etched more than the edges. CMP can be used to produce patterned thermal oxide in a silicon wafer, as shown below. The surface silicon structures can then be used to support free-standing structures where the quantity of silicon oxide that is sacrificially removed is defined by the size of the silicon oxide trenches.

1. Pattern photoresist onto a bare silicon wafer.

2. Dry etch vertically into the silicon wafer to produce silicon mesas.

3. Remove the remaining photoresist and thermally oxidise the surface of the silicon.

4. Perform CMP on the sample to expose the unoxidised silicon mesas leaving silicon oxide filled trenches. [25%]

(ii) Polymer planarisation. Surface tension will tend to cause a spin-on polymer to form a flat surface. As the polymer dries, its thickness will reduce and some of the underlying structure will be transferred to the surface, but with reduced amplitude. The application of several layers will eventually result in a highly planarised surface. Polyimide makes an excellent planarisation polymer. Not only can it be spin coated, but it can also withstand temperatures up to ~300 °C. SU8 is also suitable for this purpose. The major disadvantage of this technique is that it only produces flat surfaces in polymers. However, it could be used to produce a flat surface upon which a three dimensional SU8 structure is to be produced, ensuring that photolithographic exposure is uniform over the whole sample area. [25%]

(iii) Resist etchback. Polymers can also be used to planarise an oxide layer using dry etch technology. A rough oxide surface is coated in a polymer which has similar dry etch characteristics to the oxide. The polymer will tend to form a smooth surface due to surface tension. After drying and curing, the polymer coated oxide is dry etched. This transfers the smooth topography of the polymer surface back to the oxide surface. A schematic of the use of this technology is shown below. It can be used to provide a flat surface on silicon oxide for the subsequent production of free-standing silicon structures, where the flatness of the silicon structure is important (e.g. a micromirror). However, care must be taken to find a polymer with the same etch rate as the oxide. Also, surfaces which have more than one material present (e.g. both silicon and silicon oxide) cannot be planaraised in this way.

1. Silicon wafer is coated with a rough oxide surface.

2. A photoresist is spin coated onto the oxide to produce a flat surface

3. A dry etch removes both oxide and photoresist at the same rate.

4. All the photoresist is removed to leave a planarised oxide surface.

[25%]