ENGINEERING TRIPOS PART IIB

Wednesday 25 April 2007 9 to 10.30

Module 4B2

POWER MICROELECTRONICS

Answer not more than ***three*** *questions.*

All questions carry the same number of marks.

The ***approximate*** *percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS	SPECIAL REQUIREMENTS
Single-sided script paper	Engineering Data Book CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Discuss briefly the differences between a punch-through (PT) high voltage junction and a non-punch-through (NPT) high voltage junction. Which of the two is preferred in the design of a vertical MOSFET and why? [30%]

(b) An Insulated Gate Bipolar Transistor (IGBT) used in a Switch Mode Power Supply (SMPS) application has current waveforms as shown schematically in Fig. 1. During the on-state period, the current increases linearly with time reaching a peak value, I_{peak} = 16 A from where the device switches off. The IGBT operates at a frequency of 50 kHz with a duty cycle, D = 50%. The turn-off energy loss per switching cycle is estimated to be 3 mJ while the turn-on and off-state losses can be neglected.

For a first order approximation, the on-state voltage drop in the IGBT is estimated to vary linearly with the on-state current as shown in eq. (1)

$$V_{on} = V_{offset} + R\, I_{on} \qquad (1)$$

where V_{offset}=1.5 V and $R = 0.5\ \Omega$.

(i) Estimate the on-state power losses in the IGBT. [30%]

(ii) Estimate the switching power losses, and given the result, comment on the choice of the operating frequency for the IGBT. [20%]

(iii) For accurate modelling of a real IGBT, eq (1) leads to significant errors. Explain why this might be the case and discuss the impact of its use in the power loss estimation. [20%]

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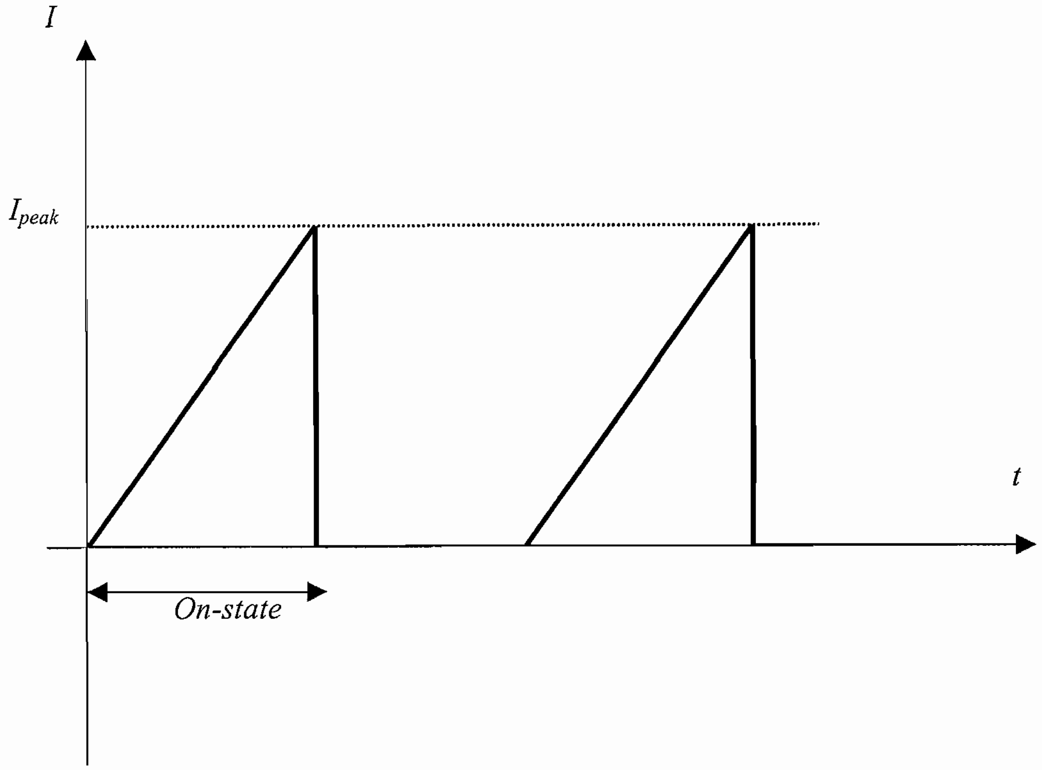

Fig. 1

2 (a) Show schematically the reverse characteristics of the bipolar junction transistor (BJT), indicating clearly the specific breakdown values. Explain briefly the phenomenon of second breakdown. [30%]

(b) What is the super-junction effect? Draw schematically the structure of a Cool MOS and explain briefly its operation. Why does this structure have a limited breakdown range? [30%]

(c) Table 1 shows some material parameters for a 1.2 kV Silicon MOSFET and a 1.2 kV Silicon Carbide (SiC) MOSFET. Both designs are optimised to have a minimum specific on-state resistance. Calculate the relative decrease in the specific on-state resistance given by the SiC MOSFET with respect to that of Silicon. State any assumptions made. [40%]

	Silicon	**Silicon Carbide (SiC)**
Critical Electric field, E_{cr} [V/cm]	$3 \cdot 10^5$	$2 \cdot 10^6$
Relative permittivity, ε_r	12	9
Electron mobility, μ_n [cm^2/(Vs)]	1200	800

Table 1

You may assume the following equations in the calculations of breakdown and specific on-state resistance:

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q}\frac{1}{N_D}\right]^{\frac{1}{2}}$$

$$R_{specific-drift} = \frac{w_{drift}}{q\mu_n N_D}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, w_{drift} is the width of the drift region, μ_n is the electron mobility in the drift region, V is the reverse voltage and the other symbols have their usual meaning.

3 (a) Describe briefly the *dI/dt* effect in thyristors and give two main solutions to improve the device *dI/dt* rating. [30%]

(b) The structure in Fig. 2 is a MOS Controlled Thyristor (MCT). The device can be switched on and off using MOS control.

(i) Explain briefly its operation during on-state, off-state, turn-on and turn-off. [30%]

(ii) Draw an equivalent circuit for the device. *[Hint: draw the turn-on and the turn-off MOS gates separately]* [30%]

(iii) Give one advantage and two disadvantages of this device compared to a conventional Insulated Gate Bipolar Transistor (IGBT). [10%]

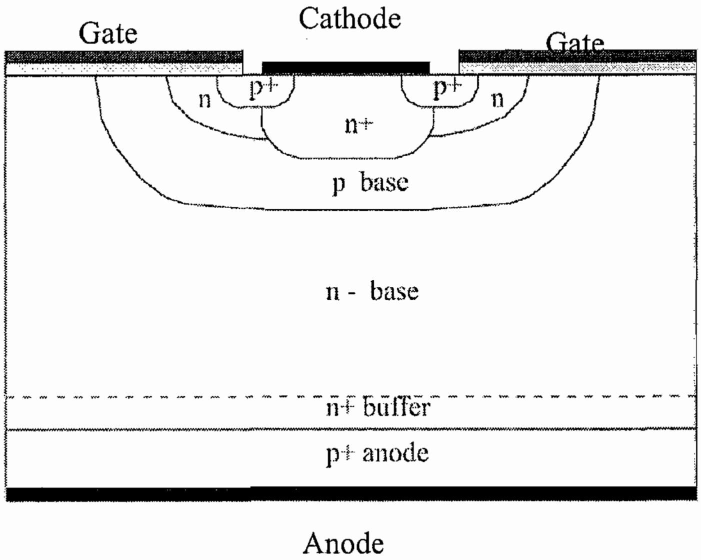

Fig. 2

4 (a) Describe briefly the turn-off process in thyristors, giving detail to the design modifications needed to guard the device against *dv/dt* surges. [30%]

(b) Fig. 3 shows a 600 V n-channel MOSFET, the source of which has been coupled with a small stray inductance L_S. The gate voltage V_{GG} is implemented as a 15 V step at turn-on, and the inductive load current is 400 A. The drain current of the MOSFET is proportional to the gate-source voltage V_{GS}, where the transconductance, g_m is assumed to be constant. Show that the expression for V_{GS} reduces to

$$V_{GS}(t) = V_{GG}\left[1 - \exp\left(-\frac{t}{\tau}\right)\right],$$

where τ is a constant. [40%]

Estimate the *di/dt* applied to the associated freewheel diode D_f by the MOSFET at turn-on. [10%]

If the stored and depletion charges in the diode are 60 μC and 15 μC respectively at 400 A, find the peak reverse recovery current in D_f and the reverse recovery time of the MOSFET. [20%]

Take $L_S = 2$ nH, $g_m = 600$ S, $C_{iss} = 120$ nF, $C_{rss} = 0$ nF, $V_{th} = 0$ V, $R_{GG} = 3.3\ \Omega$.

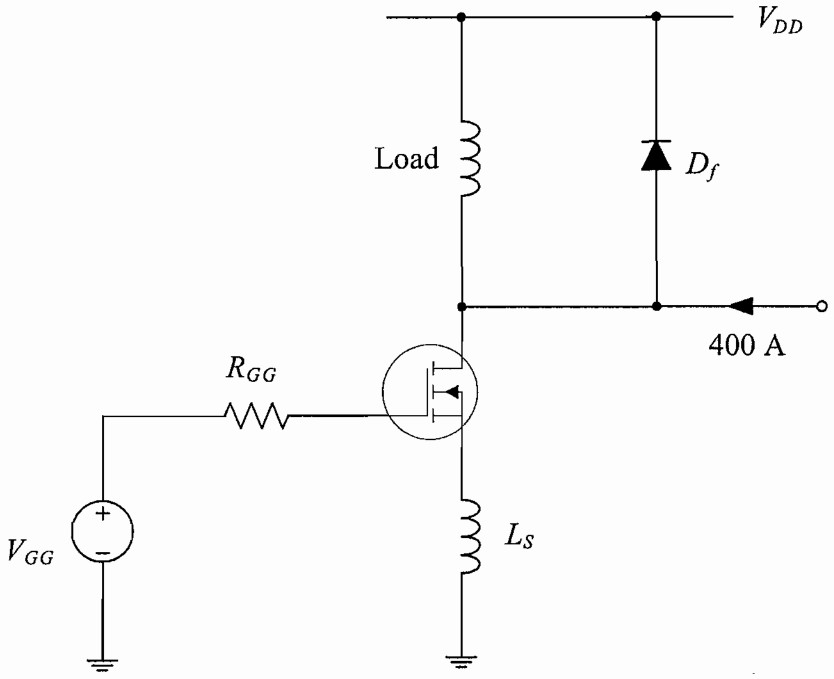

Fig. 3

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Answers 4B2 – 2007.

Q1. (b) P_{ON}=27.33W, $P_{turn\text{-}off}$=150 W

Q2(c) (ii) $R_{si} = 148R_{SiC}$

Q4 (b) $\tau = 1.6\ \mu s$ di/dt= 5640 A/μs (c) t1=145.9ns trr=182.4ns Irr=823 A