ENGINEERING TRIPOS PART IIB

Tuesday 8 May 2007 2.30 to 4

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed
Supplementary pages: None.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 The inverting circuit shown in Fig. 1 is a NOT gate in Bi-CMOS technology.

(a) Explain the DC operation of the gate describing the states of the transistors and the output voltages. Find V_{OL} and V_{OH}. Explain the roles of the transistors M_1 and M_2. What are the advantages and disadvantages of this Bi-CMOS gate compared to a standard CMOS gate? [30%]

(b) Sketch the mask layout of the three transistor block, 'A', shown with dashed contour in Fig. 1. The layout should clearly indicate the surface diffusion layers (except the buried layers), the polysilicon layer, the metallisation and the contacts. [40%]

(c) Draw a modified circuit diagram of the NOT gate in Fig. 1 to provide a two input Bi-CMOS NAND gate. [30%]

(cont.

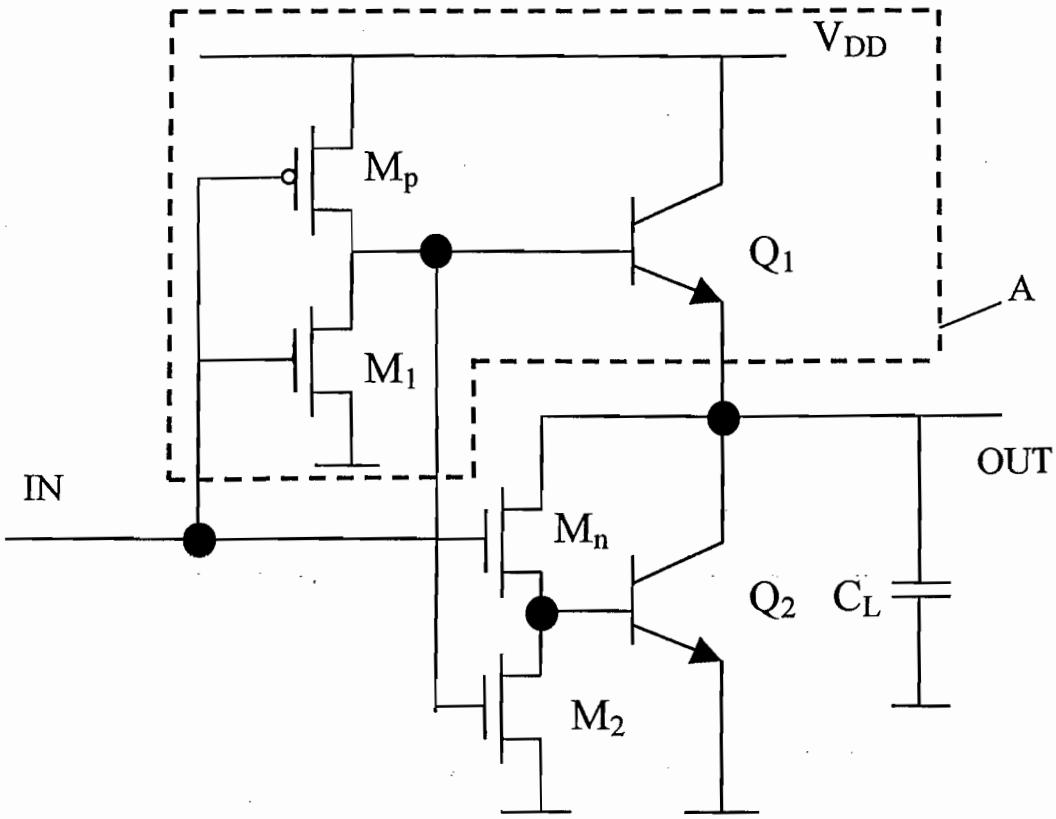

Fig. 1

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2. (a) Give two main advantages and two disadvantages of the SOI technology compared to bulk silicon technology. [20%]

(b) Describe schematically the process steps involved in producing:

(i) wafer bonded and

(ii) Smart-Cut (Unibond) Silicon-On-Insulator (SOI) wafers.

Use drawings to exemplify the steps. What are the advantages and drawbacks of the two technological approaches against each other? [30%]

(c) Describe two main failure mechanisms associated with dielectrics in IC technology. Explain ways to differentiate between them. [20%]

(d) A VLSI integrated circuit has been subjected to an Electromigration (EM) acceleration test by applying high current densities in the metal tracks under high temperature conditions. The average failure rate was 6×10^{-5} per hour at a temperature of 125 °C and a current density of 5×10^{6} A/cm^2. Estimate the average failure rate in the field of use at a temperature of 40 °C and a current density of 10^{6} A/cm^2. Use FIT (Failure In Time) units. The EM failures are described by the equation below, where the activation energy, $Ea = 0.8$ eV and the acceleration factor, n = 2. [30%]

$$t_F = CJ^{-n}e^{(Ea/kT)}$$

where t_F = time to failure in the EM test, C is a constant, Ea is the activation energy, J is the current density, k is the Boltzmann constant (8.6×10^{-5} eV/K) , T is the temperature (in K) and n is the acceleration factor.

3 (a) Explain the meaning of the term scaling as applied to the design of CMOS integrated circuits. Discuss, with reasons, any parameters other than device dimensions that may need to be adjusted as part of the scaling process. [20%]

(b) A designer is considering which of two available CMOS fabrication processes to use for a new mixed-signal design operating at a high frequency. These are:-

(i) an established process with minimum gate width 0.25 μm and 2.7 V rated power supply;

(ii) a new scaled process with minimum gate width 0.18 μm and 1.8 V rated power supply.

Write a brief report detailing the advantages and disadvantages of the two processes. [80%]

Your report should take account of the different structures typically present in a mixed-signal design and should make reference to packing density, cost, yield, capacitance, current, power consumption and delay as well as any other factors you consider important.

4 (a) What is meant by the term *design rule* in CMOS integrated circuit design? Write a short account of the ways in which design rules constrain the form and dimensions of interconnect and contact structures in CMOS technologies. In your account, indicate the origins of the rules you introduce, making it clear whether they arise from physical, electrical or processing constraints. **Note**: details of specific manufacturers' rules are not required. [60%]

(b) An echo cancellation unit for use in a multimedia application implemented as a CMOS integrated circuit uses a large array of 16,000 memory elements organised as a set of eight 2,000-bit shift registers. All stages of the shift register are driven with a 40 MHz clock. Each memory element drives a load which is purely capacitive and equivalent to 30 fF. Binary data sequences are accepted in parallel at eight input pins, and after passing through the shift register, are presented at eight outputs.

By considering the dynamic power dissipated in the array as data is clocked through, estimate the worst-case current consumption of the array, assuming that the supply V_{DD} is 3.3 V. You may ignore power consumed by input/output pads and other parts of the chip. State any other assumptions made. [20%]

Electrical power for the shift register array is supplied by means of aluminium interconnect of layer thickness 0.5 μm. Assuming that significant electromigration may be expected to occur in aluminium interconnect at current densities in excess of 10^9 Am^{-2}, determine a suitable width for the interconnect used to supply the required current, stating any assumptions made. [20%]

5 (a) Describe the circuit and mode of operation of a transmission gate in complementary MOS technology, and explain clearly how this circuit may provide performance superior to that of a simple pass transistor. Give examples of the use of transmission gates in:

(i) digital circuits

(ii) analogue circuits,

briefly indicating any advantages and disadvantages of the circuit in these applications. [50%]

(b) Explain the origin of *body effect*, or *back-gating*, as encountered with MOS transistors. How does this phenomenon affect the measured characteristics of a transistor? By considering the circuits for two-input CMOS NAND and NOR gates, explain qualitatively how body effect influences:

(i) the static transfer function;

(ii) gate delay.

What measures are available to the integrated circuit designer to alleviate these difficulties? [50%]

END OF PAPER