ENGINEERING TRIPOS PART IIB

Monday 30 April 2007 9.00 to 10.30

Module 4B8

ELECTRONIC SYSTEM DESIGN

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Log-log paper is attached. Please detach and submit with your answers if required.

Write your name on every page / log-log paper of your answers, and number your answers on each page.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

Version: 19/3/07

1 (a) A filter is wanted with low and high frequency *–3 dB* points at *10 Hz* and *600 Hz* respectively and with an approximately constant gain between these frequencies. Describe briefly how this may be achieved. What could this circuit be used for?

[15%]

(b) Another filter circuit is to have a peaked gain response between the input voltage v_1 and the output voltage v_2 of the form:-

$$v_2 / v_1 = A\, s\, \omega_0 / (s^2 + \alpha\, \omega_0\, s + \omega_0^2) \quad \text{where } s = j\,\omega .$$

Sketch the main features of the voltage gain against frequency ω characteristic showing particularly the gain at frequency, $\omega = \omega_0$ and the half power bandwidth, $\alpha\omega_0$ on your sketch.

[15%]

(c) The circuit containing 3 Op-Amps shown in Fig. 1 is to be used for this second filter type. Assuming that the Op-Amps are *ideal*, show that it has a similar response for the voltage gain v_2 / v_1, with expressions in terms of the circuit components indicated, given by:

$$A\,\omega_0 = R_3 / (C_2\, R_6\, R_4) \;, \qquad \omega_0^2 = R_3 / (C_1\, C_2\, R_6\, R_7\, R_1) \qquad \text{and}$$

$$\alpha\,\omega_0 = R_3\, R_5\, (1/R_4 + 1/R_1 + 1/R_3) / (C_2\, R_6\, (R_5 + R_2))$$

[45%]

(d) For component values $R_1 = R_2 = 100\ k\Omega$, $R_3 = 10\ k\Omega$, $C_1 = C_2 = 10\ nF$, and given that $R_6 = R_7$, determine the values of R_4, R_5, R_6 and R_7 for a circuit of peak gain of *50* at a frequency of *200 Hz* and with a half power bandwidth of *10 Hz* ?

[25%]

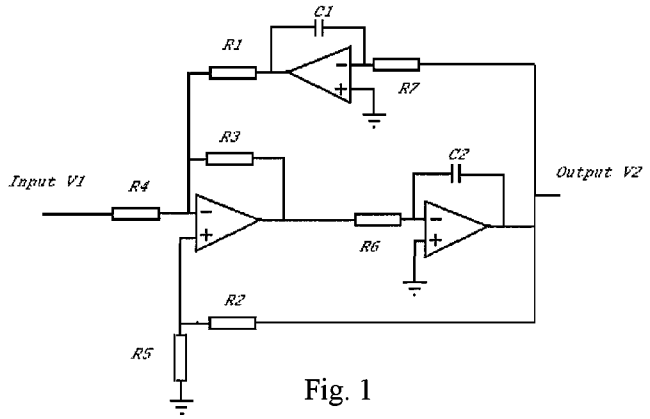


Fig. 1

2 (a) Show the outline diagram, using resistors, diodes and Op-Amps, of how a circuit might be arranged whose output voltage V_0 would be the *product* of its two input voltages V_1 and V_2. Clearly explain the signal polarities for which the circuit is suitable and give the relative resistor values of those needed in your diagram.

[25%]

(b) How would a multiplier package be arranged so that a circuit is given whose output voltage is the *square root* of the input voltage? Briefly explain its action.

[10%]

(c) Using the normal Shockley equation for the current I_D against voltage V_D of a diode junction, and assuming that the circuit temperature is such that $k\ T\ /\ q$ is $26\ mV$, derive equations showing the logarithmic relation of the device voltage to current and explain any limitations clearly.

[25%]

(d) Why and how is a transistor usually used in place of a diode in "logarithmic" circuits? Explain what is done to keep any errors to be three times less than the typical *1 %* tolerance of any resistors in use in the circuit.

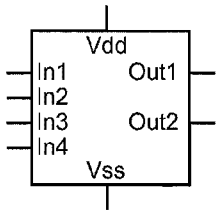
[20%]

(e) What circuits might be added to that given in (d) above to null the reverse saturation current of the transistor junction and to give a circuit having a *2 V* change in output for a <u>*decade*</u> change in input voltage? Show suitable component values where possible which would keep any resistor loads on Op-Amp outputs to be greater than $10\ k\Omega$.

[20%]

3. A digital phase-angle power control heater, running from 230VAC/50Hz mains is to be implemented using a microcontroller and a sensitive gate triac. The heater will have 2 user input buttons, namely "hotter" and "colder", which sets the phase angle for firing the triac. Pressing and holding down the "hotter" button for 2.55s would bring the heater gradually from completely off to completely on. Pressing and holding down the "colder" button for 2.55s would bring the heater from completely on to completely off.

8-bit Microcontroller
Suggested circuit symbol (12C509):



- Supply voltage = 5V
- Supply current = 400μA
- Oscillator = internal/4MHz
- Number of input pins = 4
- Number of output pins = 2
- Output current (max) = 25mA

Triac (2N6071) turn on characteristics
- Gate trigger current = 2mA
- Gate trigger voltage = 2.5V
- Min gate pulse width = 1μs

Heater element
- Load type = purely resistive
- Power @ 230V = 920W

(a) Describe what is meant by "*polling*" and "*interrupt*" implementation of microcontroller programs. Discuss the advantages/disadvantages of "*polling*" and "*interrupt*" implementation.

[20%]

(b) Draw a *complete* circuit diagram for the digital phase-angle power control heater, showing all inputs, components and their values.

[40%]

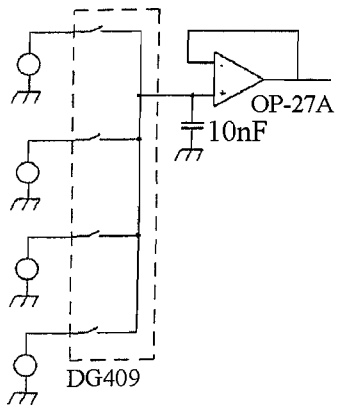
(c) Draw a *flow diagram* for the implementation of the heater, from gathering the user inputs to firing the triac appropriately.

[30%]

(e) Describe the function of a *watchdog timer*. What is the minimum period of the watchdog timer for your program?

[10%]

4. A 4-channel sample and hold circuit is to be made from a DG409 and OP27.



Hold capacitor = 10nF

DG409 4-channel switch
R_{switch} = 40Ω
Total leakage = 1nA
Switching delay = 0.25μs
Charge injection = 20 pC

OP-27A op-amp
Input bias current = 10nA
Assume no slew rate limitations

(a) What is the *acquisition time*, when one input channel is selected, for an accuracy of 0.1%?

[10%]

(b) What is the *hold step voltage* when an input channel is selected? [5%]

(c) The input switch is opened and the sample is held. What is the *droop rate* of this circuit? For a 5V full-scale range, 16-bit dual slope integrating A-D convertor, what is the *maximum conversion time* allowable for ½ LSB error?

[15%]

(d) Draw a block diagram of *a sigma delta modulator* which is used to convert an analog signal into a 1-bit stream. For each block, write down the equation which gives the output of each block in the diagram.

[25%]

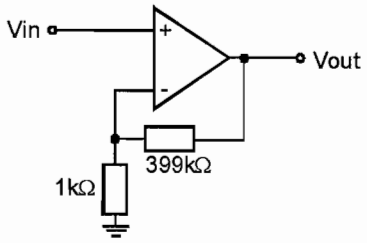
(e) Using a table whose columns are the output of the various blocks of the sigma-delta modulator, generate the first 5 bits (ie. t = 1 to 5) of the output stream for a 2V dc analog input. The '0' level is 0V and '1' level is +5V. At t = 0, assume the outputs at all blocks is 0V. [35%]

(f) Show how the bitstream from (e) can be converted back to the original analog dc level and draw a circuit to do this.

[10%]

(TURN OVER)

5. An op amp with a dc gain of 10^6 and 2 poles, f_1 = 1kHz and f_2 = 1MHz, is used in the following non-inverting amplifier. Assume there are no slew rate limitations.



(a) Draw the open circuit Bode plot (gain and phase) of the op-amp.

[10%]

(b) Determine if the non-inverting amplifier is under-damped, critically damped, or overdamped.

[20%]

(c) Sketch the time response of the non-inverting amplifier to a step function input of 0.01V. Label important features (eg. voltage, time).

[20%]

(d) Sketch the frequency response of the gain of the non-inverting amplifier on your Bode plot. Label important features (eg. gains and frequency).

[20%]

The op-amp is now used in a new circuit with unity gain. Fortunately, the pole f_1 is due to the capacitance across the inputs in the op-amp and can easily be changed by adding more capacitance – ie. f_1 can be moved. f_2 cannot be changed and stays at 1MHz.

(e) Sketch the circuit diagram of the unity gain circuit and determine the frequency of the new dominant pole (f_1) in order for the unity gain circuit to have a phase margin of 45°?

[10%]

(f) Sketch the frequency response of the gain of the compensated op-amp on your Bode plot. Sketch the response of the unity gain circuit on the Bode plot showing the location where the phase margin is 45°. Determine the gain bandwidth product of the compensated op-amp.

[20%]

Second order op-amp with feedback ratio (β):

$$A_f(j\omega) = \frac{A(j\omega)}{(1+\beta A(j\omega))} \quad \text{where} \quad A(j\omega) = \frac{A_O}{\left(1+j\frac{\omega}{\omega_1}\right)\left(1+j\frac{\omega}{\omega_2}\right)} \quad \text{gives:}$$

$$Gain = |A_f| = \frac{|A_{of}|}{\left[\left\{1-\left(\frac{\omega}{\omega_n}\right)^2\right\}+4k^2\left(\frac{\omega}{\omega_n}\right)^2\right]^{1/2}}$$

where $A_{of} = \frac{A_O}{1+\beta A_O}$

$\omega_n = [\omega_1\omega_2(1+\beta A_O)]^{1/2}$

$k = \frac{\omega_1+\omega_2}{2\omega_n}$

Peak occurs at: $\omega = \omega_n(1-2k^2)^{1/2}$

with $|A_{peak}| = \frac{|A_{of}|}{\{2k(1-k^2)^{1/2}\}}$

END OF PAPER