

ENGINEERING TRIPOS PART IIB

Tuesday 8 May 2007 9 to 10.30

Module 4M6

MATERIALS AND PROCESSING FOR MICROSYSTEMS (MEMS)

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

Attachments: 4M6 Data Book (13 pages).

STATIONERY REQUIREMENTS

Single-sided script paper

SPECIAL REQUIREMENTS

Engineering Data Book

CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Describe the process of *thermal oxidation* for the growth of silicon oxide on a crystalline silicon wafer. Your answer should include a diagram of the system used for growth and highlight the key process conditions required. [40%]

(b) Explain why silicon oxide is an important material for the production of free-standing micro-structures made from silicon. To exemplify your answer, describe a process flow for producing free-standing structures of crystalline silicon on an SOI wafer. [35%]

(c) Free-standing cantilever structures of up to 100 μm length are to be formed from a 1 μm thick layer of polycrystalline silicon that has been deposited onto the surface of a silicon oxide coated silicon wafer. Calculate the minimum thickness of the silicon oxide layer that would be required to ensure that stiction cannot permanently occur between the free standing cantilevers and the silicon substrate. You should take the silicon-silicon surface energy to be 0.1 J m^{-2} . State any other assumptions that you make. [25%]

NOTE: $s^*4 = \frac{3Eh^3g^2}{2\gamma}$

2 A thermal actuator, shown in Fig. 1, is to be fabricated in the form of a U-shaped cantilever from a free-standing bilayer of nickel and silicon nitride thin films to produce movement out of the surface plane of the substrate.

(a) Why it is important to minimise thermal and intrinsic stress in the nickel and silicon nitride layers of this structure? [20%]

(b) What physical phenomena might lead to the presence of intrinsic and thermal stresses in this bilayer? [35%]

(c) Construct a process flow for the fabrication of these devices on a silicon wafer, starting from the bare substrate, and using a KOH etch for the release stage of the process. The thickness of the nickel layer is 200 nm and the thickness of the silicon nitride layer is 300 nm. You may assume that nickel is not etched by KOH solution. Justify your choice of processes. [45%]

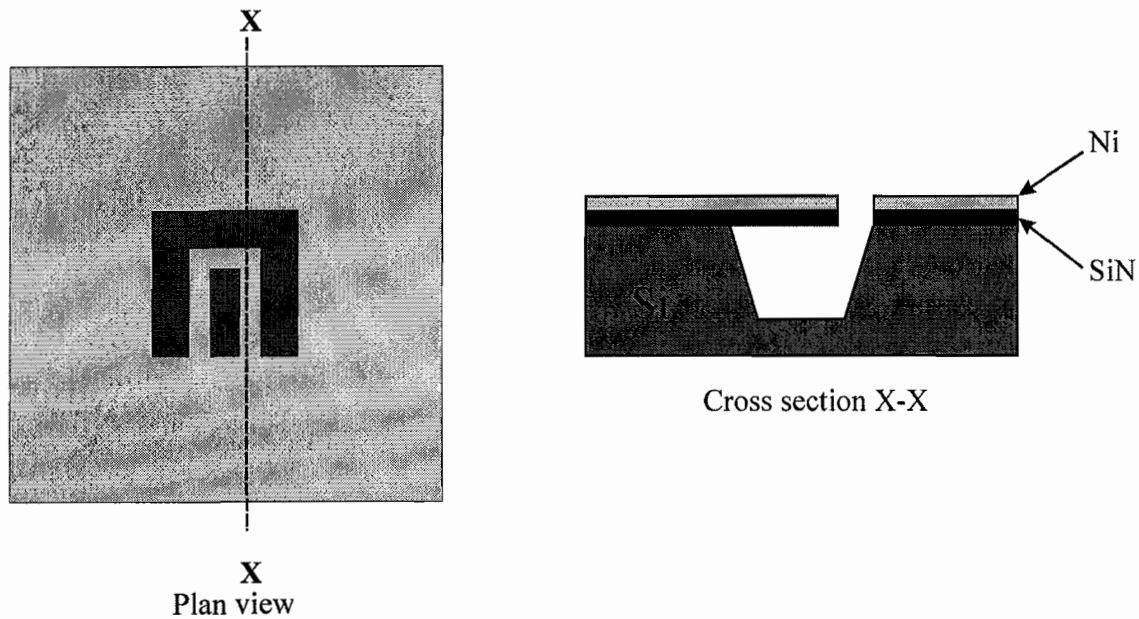


Fig. 1

3 (a) Explain what is meant by the following terms, and how they affect the design of a process flow for microsystem device fabrication:

(i) *process partitioning*;

(ii) *contamination constraints*;

(iii) *wafer architecture*;

(iv) *packaging*.

[40%]

(b) A microscale chemical reactor for catalysing a reaction between two liquids is to be fabricated on a silicon wafer. The reactor cavity consists of a 10×10 array of silicon pillars which are within a well. Each pillar is $200 \mu\text{m}$ tall and $20 \mu\text{m}$ in diameter and at a pitch of $30 \mu\text{m}$ with respect to neighbouring pillars. The interior of the cavity and the surface of the pillars is coated in a thin layer of copper, which is $\sim 10 \text{ nm}$ thick. A schematic diagram of the reactor is shown in Fig. 2.

(i) Construct a process flow for the fabrication of the micro-reactor, starting from a bare silicon wafer. Justify your choice of processes.

[50%]

(ii) Why is it advantageous to construct a chemical reactor on the microscale?

[10%]

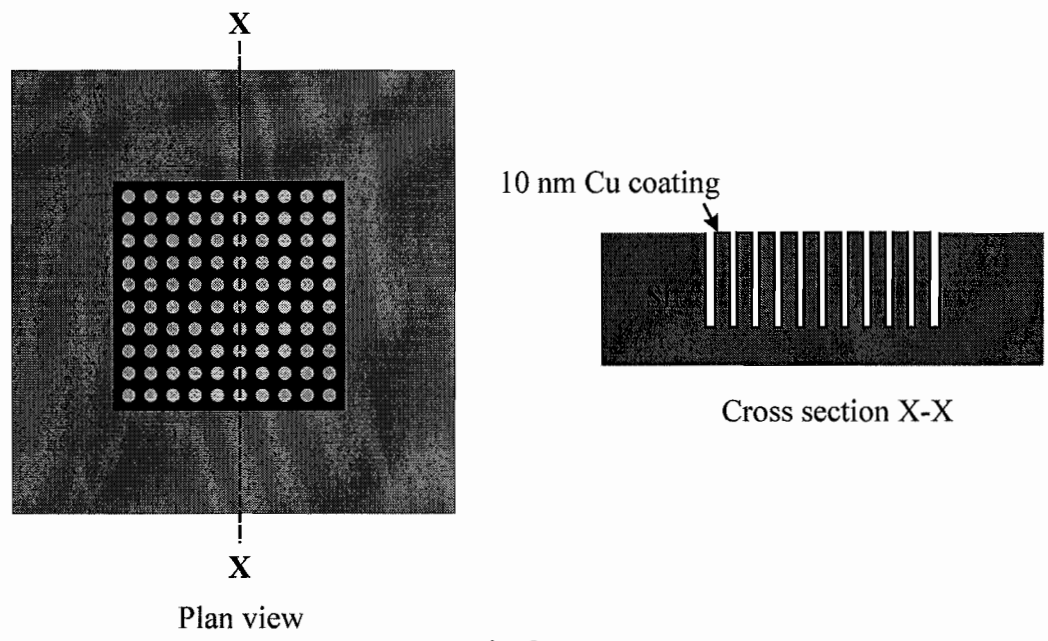


Fig. 2

4 (a) Why is it frequently necessary to planarise the surface of a wafer upon which microsystems devices are being produced during the process flow? [25%]

(b) Describe the following methods for planarising a surface. In each case highlight both the advantages of the method and its limitations. Illustrate your answers with examples of situations in which it would be appropriate to use each technique.

(i) *chemical mechanical polishing*; [25%]

(ii) *polymer planarisation*; [25%]

(iii) *resist etchback*. [25%]

END OF PAPER