ENGINEERING TRIPOS PART IIB

Tuesday 6 May 2008 2.30 to 4.00

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed
Supplementary pages: None.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Draw a diagram of the bath-tub curve that describes the three parts of the failure rate curve of typical VLSI products, and annotate the diagram with

(i) the nature and distribution of the various failures and

(ii) two examples of the various failure mechanisms in each part of the overall failure curve. [40%]

(b) At the device level failures might occur in

(i) the oxide film,

(ii) the metallization,

(iii) the passivation,

(iv) the die or wire bonding.

For any three of these, describe typical failure mechanisms and failure signatures. [30%]

(c) Write notes on the following failure modes as they apply to VLSI products:

(i) Electromigration

(ii) Time-dependent dielectric breakdown

(iii) Hot carrier injection and degradation [30%]

2 Figure 1 shows a current mirror circuit fabricated from n-channel MOS transistors.

(a) Show that, under appropriate conditions, the current I_2 passing through the load resistor R_L depends only on the current I_1 and the dimensions of the active regions of the transistors M1 and M2. State any assumptions made. [30%]

(b) Explain why lithographic tolerances and fabrication process variations may result in I_2 deviating from the design value, and discuss measures that can be taken by the designer to alleviate certain of these difficulties. [20%]

(c) Determine suitable relative dimensions for the active devices if I_2 is required to be 400 μA when I_1 is 100 μA. [30%]

(d) Explain briefly how to extend this circuit so it provides in addition a controlled current of $10I_1$ through a further load resistor which has one of its terminals connected to the negative supply terminal V_{SS}. [20%]

You may assume the following expressions for the drain current I_D in a MOS transistor, where the symbols have their conventional meaning.

$$I_D = \frac{\mu\varepsilon}{t_{OX}}\frac{W}{L}\left((V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right) \qquad 0<V_{DS}<V_{GS}-V_T$$

$$I_D = \frac{1}{2}\frac{\mu\varepsilon}{t_{OX}}\frac{W}{L}(V_{GS}-V_T)^2 \qquad 0<V_{GS}-V_T<V_{DS}$$

(cont.

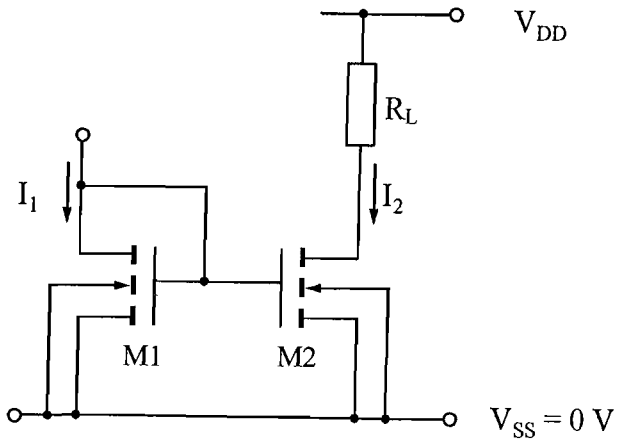

Figure 1

3 A simple form of one-bit dynamic memory cell relying for its storage element on parasitic capacitance is shown in Fig. 2.

(a) Briefly describe how this circuit works for *read* and *write* operations. Discuss the origin of capacitances C_S and C_B, and state how they affect the performance of the memory. [40%].

(b) A square array of cells based on the schematic in Fig. 2 is used as the basis of a memory chip operating from a 3 volt supply. Each cell occupies an area of the silicon wafer 5 μm × 5 μm in dimensions. The capacitance C_S is 30 fF, and each transistor has drain-substrate capacitance of 5 fF. The metal interconnect used to form the bit line has specific capacitance per unit length of 0.6 fF μm^{-1}.

If the sense amplifier used to read out the data is able to discriminate a signal at its input of 10 mV, estimate the largest memory that can be constructed using this cell. State any assumptions made. [30%]

(c) *Flash* memories can provide non-volatile storage with densities and access times comparable to those of dynamic memory, but require no storage capacitor. Discuss this statement and describe how these benefits are accomplished. [30%]

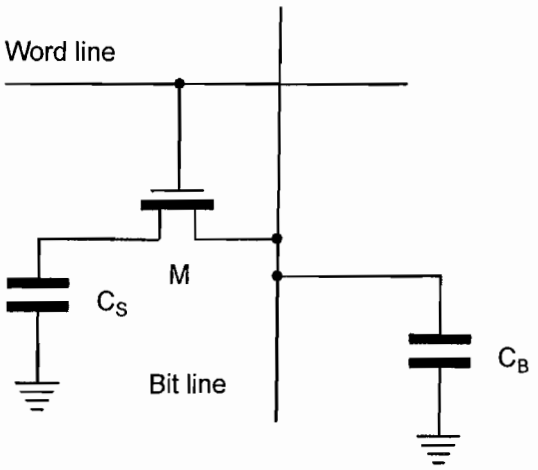

Fig. 2

4 (a) Describe with a diagram the operation of an n-channel MOS transistor. If the gate length is 0.1 μm, indicate on the diagram the thicknesses of the various layers and the lateral feature sizes. [30%]

(b) With a series of diagrams, show the process route by which such an MOS transistor is made, including brief notes on the individual process steps. [30%]

(c) If this transistor was a part of a CMOS circuit, what other process steps would be involved? [30%]

(d) Given that the dielectric constant of SiO_2 is $\varepsilon_{SiO2} = 4 \times 10^{-11}$ F/m, and the charge of an electron is 1.6×10^{-19} C, approximately how many electrons are stored in a 0.05 μm gate-length, square-channel, transistor with a 2 nm gate oxide, biased to 3V? Comment on this value in the context of circuit operations. What if the transistor is scaled to 0.01 μm gate length? [10%]

5 (a) Explain the meaning of the term *sheet resistance*. Show how this concept can be used during the design of an integrated circuit to predict the resistance of electrical interconnects containing a number of right-angle bends. [30%]

(b) Describe briefly how *ring oscillator* circuits can be used to measure nanosecond gate delays despite the comparatively large time delays associated with getting signals on and off chip. What are the limitations of this approach to characterisation of logic gate performance? Discuss whether or not a simple ring oscillator design can give a realistic measurement of practical circuit delays. [40%]

(c) In recent years, silicon on insulator (SOI) technology is replacing bulk silicon technology for CMOS applications. Describe the relative merits and weaknesses of the competing technologies

(i) silicon-on-sapphire

(ii) SIMOX (separation by implantation of oxygen) and

(iii) BESOI (bonded and etched back SOI). [30%]

END OF PAPER