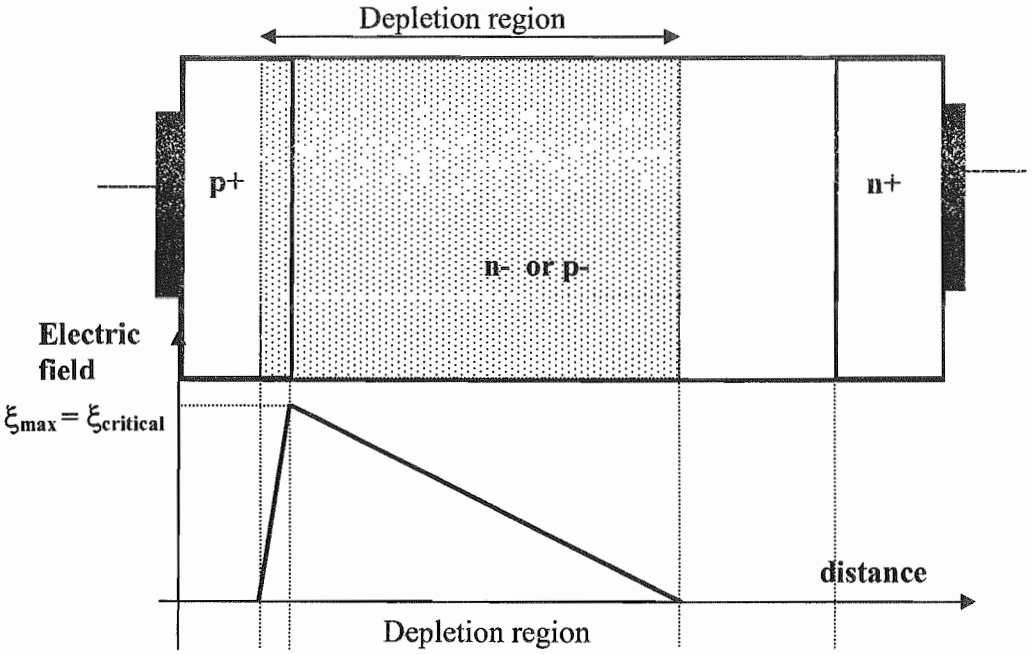
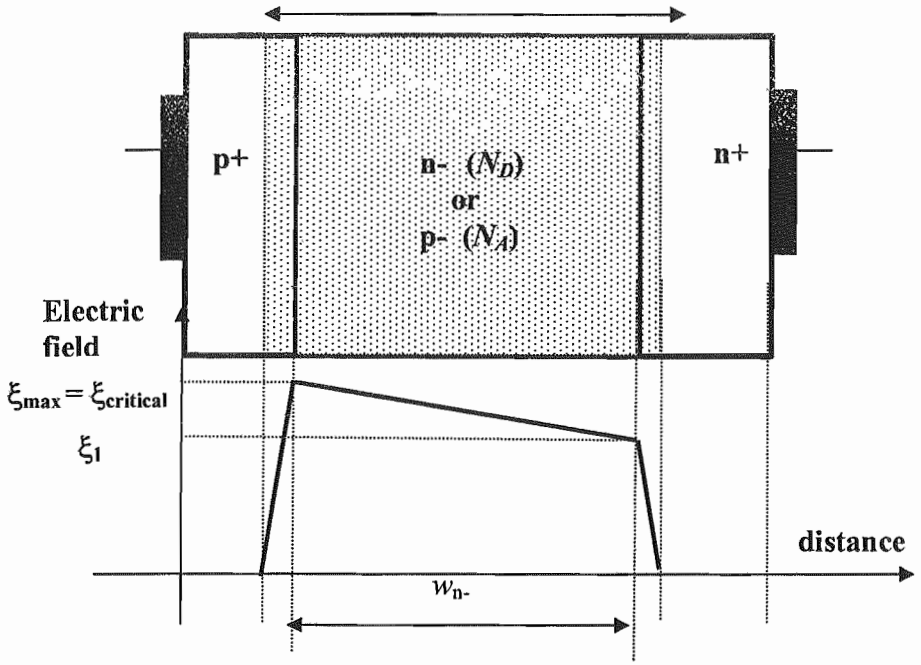
1. (a) The Non punch-through (NPT) high voltage diode is a based on a PIN diode where the thickness (width) of the lowly doped layer (n- or p-) is larger than the depletion region thickness (width) at breakdown. Thus the depletion region never reaches the n+ cathode region.



The Punch-through (PT) high voltage diode is a based on a PIN diode where the thickness (length) of the lowly doped layer (n- or p-) is smaller than the depletion region thickness (length) at breakdown. Thus the depletion region reaches the n+ cathode region before avalanche breakdown takes place.



For the BJT the PT design is more appropriate. The drift length is shorter in the PT design,and since the BJT operates in hard saturation, the charge in the drift region (collector) is much greater than the doping, so a PT design will ensure minimum drop across this region. [40%]

(b) $f = \frac{1}{T} = 10\text{kHz}$ *to*...100kHz, $D = 50\%$, $t_{on} = DT = \frac{D}{f}$

$$P_{ON} = \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON} dt = V_{ON} I_{ON} D, \qquad P_{ON\_MOS} = 3 \times 5 \times 1/2 = 7.5W$$

$$P_{ON\_IGBT} = 3 \times 2 \times 1/2 = 3W$$

TURN – OFF

Delay time: $P = V_{ON} I_{ON} t_s f$

$P_d = 3 \times 5 \times 0.1 \times 10^{-6} f = 1.5 \times 10^{-6} f$ (for both IGBT and MOS)

Growth time:

$$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_{dc} - V_{ON}}{t_g} t\right) = t_g f I_{ON}\left[\frac{V_{dc} + V_{ON}}{2}\right]$$

$$P_g\_MOS = 0.3 \times 10^{-6} \times 3 \times 202.5 \times f = 182.25 \times f \times 10^{-6}$$

$$P_g\_IGBT = 0.3 \times 10^{-6} \times 3 \times 201 \times f = 180.9 \times f \times 10^{-6}$$

Fall time :

$$P_f = tf \times f \frac{V_{dc} \times I_{ON}}{2}$$

$$P_f\_MOS = 0.1 \times 600 \times 10^{-6} f = 60 \times 10^{-6} f$$

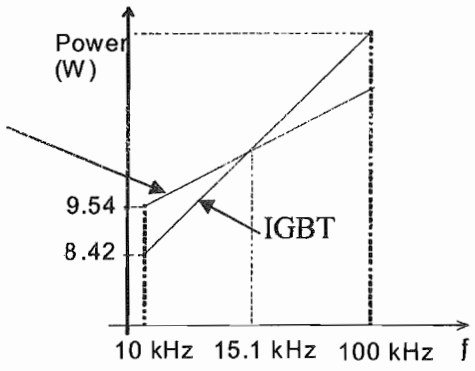
$$P_f\_IGBT = 0.6 \times 600 \times 10^{-6} f = 360 \times 10^{-6} f$$

Total losses (on-state + turn-off):

$MOS : 7.5 + 243.75 \times 10^{-6} f$

$IGBT : 3 + 542.4 \times 10^{-6} f$

Power MOSFET



The power MOSFET is more efficient at high frequencies (due to lower switching losses) > 15 kHz. IGBT is more efficient at low frequencies (due to lower on-state losses) <15kHz [40%]

(c) In the MOSFET the on-state resistance (on-state voltage) is expected to increase by 2-3 times from 25 to 150 °C. The turn-off losses in MOSFET are generally unaffected. In the IGBT, it depends if a positive temperature coefficient (NPT) or negative temperature coefficient (PT) design is employed. In any case the voltage drop can decrease or increase by a very small amount (say 0.1 V – 1V). The turn-off losses are expected to increase slightly in the IGBT as the tail current gets larger and longer at higher temperatures. Overall, the IGBT will perform better at higher

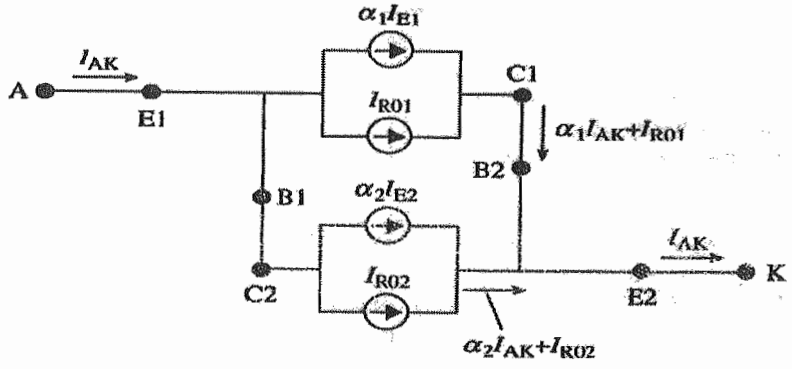
temperatures and therefore it will increase slightly the maximum operating frequency beyond which the MOSFET will be more efficient. [20%]

2. . (a) The dI_F/dt condition appears during the turn-on of the thyrsitor. If the rise time is too short (dI_F/dt is too high), the plasma cannot spread fast enough from the edge of the cathode (in the proximity of the gates) to the middle of the cathode. Therefore during the risetime the device conduction is limited to a small area around the edge (compared to the cross-sectional area of the device) and the voltage cannot fall quickly enough. Hence, large instantaneous power dissipation occurs during this period of time which leads to hot spot formation followed by thermal runaway and eventually permanent failure.

Two ways to improve this:

- increase the density of gates per total area – that is to say that we increase the density of gate-cathode inderdigitation. This also has the advantage of shortening the turn-off time (as well as the turn-on time). This is simple but requires advanced layout and photolithography.
- use a smaller auxiliary or pilot thyristor integrated on the same silicon chip with the main thyristor. The current injected into the gate of the pilot thyristor is relatively small but this is amplified by the pilot thyristor so that the gate current delivered to the main thyristor is relatively high. This is however expensive as it needs another component (or larger chip area). [30%]

(b) (i) The Ebers-Moll equivalent circuit of the thyristor based on the two equivalent circuits for the bipolar transistors is shown below. The gate current was considered to be zero as the thyristor is in the off-state.



From the equivalent circuit above (Fig. 6.5 c) one can obtain the following expression:

$$I_{AK} = \alpha_1 I_{AK} + I_{R01} + \alpha_2 I_{AK} + I_{R02}$$

where I_{AK} is the anode current (same as cathode current) and I_{R01} and I_{R01} are saturation currents (leakage currents) associated with the two transistors.

$$I_{AK} = \frac{I_{R01} + I_{R02}}{1-(\alpha_1 + \alpha_2)}$$

If $\alpha_1 + \alpha_2 < 1$ the thyristor blocks the voltage and the anode-cathode current I_{AK} (i.e. leakage current) is small; of the same order of magnitude as the saturation currents of the bipolar transistors. However when $\alpha_1 + \alpha_2$ approaches one, the leakage current increases and when $\alpha_1 + \alpha_2 = 1$ the device no longer can block the voltage and the device turns on. [30%]

(ii) Breakover occurs when

$\alpha_1 + \alpha_2 = 1$ or $\alpha_{npn} + \alpha_{pnp} = 1$

$\alpha_{npn} = 0.5 \quad \alpha_{pnp} = 1 - \frac{w_{eff}^2}{2L_p^2}$

$w_{eff} = w_{drift} - w$ (The effective base of the pnp transistor is the undepleted region of the n –difrift region – n-base).

$$\Rightarrow \alpha_{pnp} = 1 - \frac{(w_{drift} - w)^2}{2L_p^2} = 0.5$$

$$\Rightarrow (w_{drift} - w) = L_p$$

$$\Rightarrow w = w_{drift} - L_p \Rightarrow \frac{2\varepsilon_0\varepsilon_r V}{q}\frac{1}{N_D} = (w_{drift} - L_p)^2$$

$$\Rightarrow V = \text{BREAKOVER VOLTAGE} = \frac{qN_D(w_{drift} - L_p)^2}{2\varepsilon_0\varepsilon_r}$$

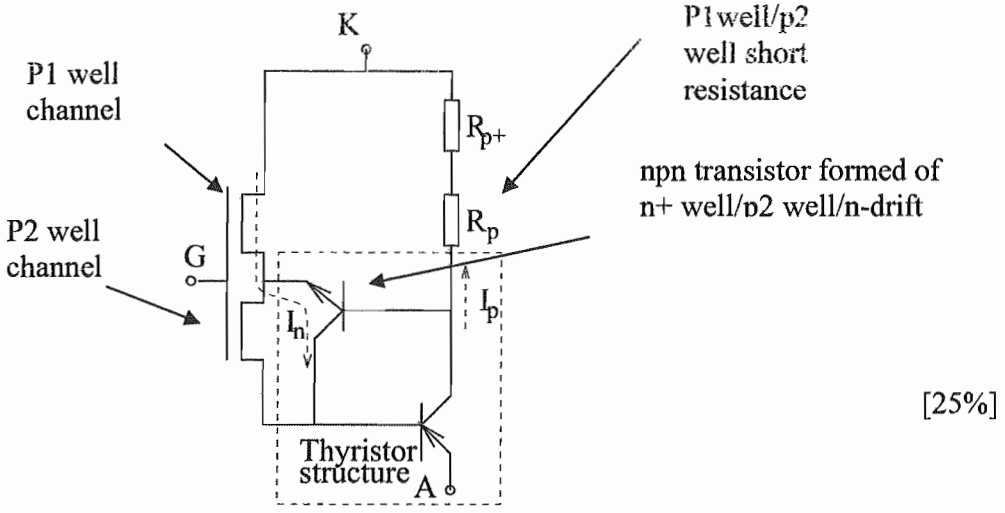
$$V = \frac{1.6\times10^{-19}\times10^{13}\times10^{6}\times150^2\times10^{-12}}{2\times11.9\times8.854\times10^{-12}} = 170.83V \Rightarrow BREAKOVER$$

For 10^{13} cm^{-3}, the avalanche breakdown voltage ~10^3 V, much higher than the breakover voltage. [30%]

(iii) The break-over voltage is based on the positive feedback of the two bipolar transitors, while the avalanche breakdown refers strictly to the abrupt multiplication of carriers when the electrical field at one location reaches a critical limit. The break-over voltage is in general smaller (and in some cases significantly smaller) and tends to limit the breakdown before avalanche sets in. Nevertheless if the gains of the npn and pnp transistors are very small (by for example applying heavy lifetime killing), it is possible, in theory that avalanche sets in before break-over. In diodes, only avalanche is possible as there is no positive feedback (no bipolar transistors present) [10%]

3. (i) This device has a built-in thyristor formed between the n+ well/p2well /n-drift/p+anode. The thyristor is in series with a MOSFET channel formed in the p1-well. There is also a path for extraction of holes during the turn-off via the p2well and p1well. The built-in thyristor will offer an increased electron injection at the upper side of the drift region which will result in higher carrier plasma formed locally at the cathode side of the drift region. This will offer a lower on-state voltage drop without penalty in the switching speed.

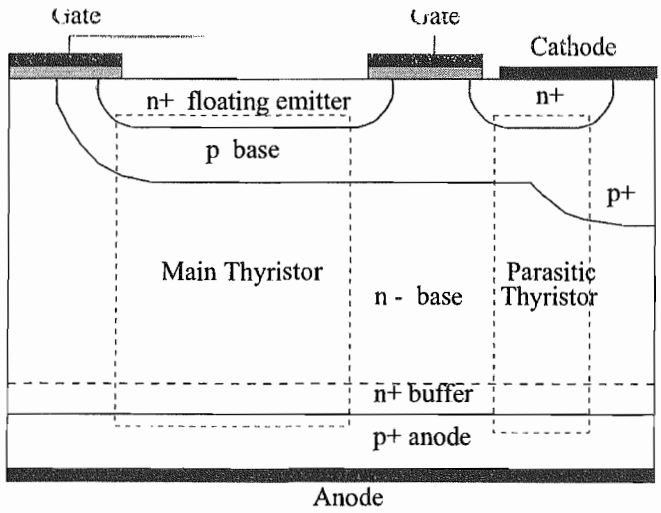
- In the off-state the device behaves similarly to an IGBT with most of the voltage supported across the n- drift region. The reverse biased junction is that formed between the p2-well and the n-drift region.
- The device is turned on by applying a positive voltage onto the gate, thus forming a channel in the p1-well and p-2 well and an accumulation layer in the n+ well. This allows injection of electrons into the n- base.
-In the on-state, as the n+well/p2 well junction becomes forward-biased, then the current will largely bypass the channel formed in the p2 well and will prefer to flow via the built-in thyristor path. The channel formed in the p1-well still controls the flow of the current. A small fraction of hole current will flow via the p1-well/p2-well window to the cathode short terminal. The thyristor will ensure high conductivity modulation and as such the n- drift region resistance is reduced significantly.
- The turn-off of the device is achieved by reducing the gate voltage under the threshold voltage. As the thyristor is in series with the MOS channel formed in the p1-well, its turn-off is well controlled without encountering classical thyristor problems such as filamentation. Holes are extracted during turn-off via the p1well/p2 well path. The depletion region extends into the n-drift region, clearing out plasma. [40%]



[25%]

(iii) Advantage: The structure has a reduced on-state voltage drop (on-state resistance or resistance of the drift region) as the thyristor increases the electron injection at the top side of the drift region (via the npn transistor). Disadvantage: The technology is complex (and therefore the cost is high). The insertion of the n+ well between the two p-wells is very difficult from a process point of view. [10%]

(iv) The alternative planar structure is shown below. The in-built thyristor is shown as the main thyristor here. The n+ well is now replaced with a surface layer called n+ floating emitter. The p base is now continuous (no need for two separate p wells).

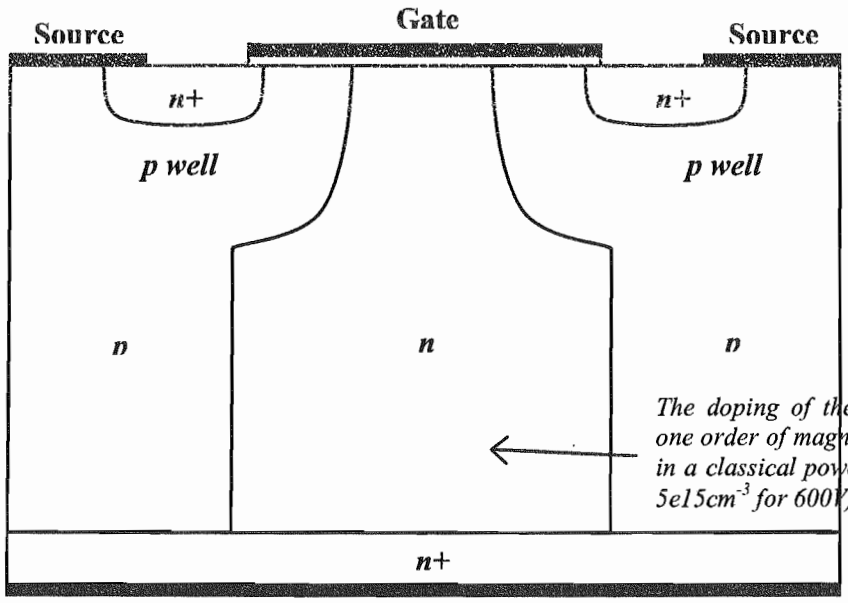


Advantages of the trench technology:
(1) higher channel density – reduced channel resistance
(2) more natural, 1D current distribution
(3) No parasitic JFET effect
(4) More robust against the latch-up (reduced influence of the parasitic thyristor)

Disadvantage : trench fabrication (by dry etch) is more difficult Filling the trench and etching back the poly is another difficult step. The technology is therefore slightly more costly than the planar alternative. [25%]

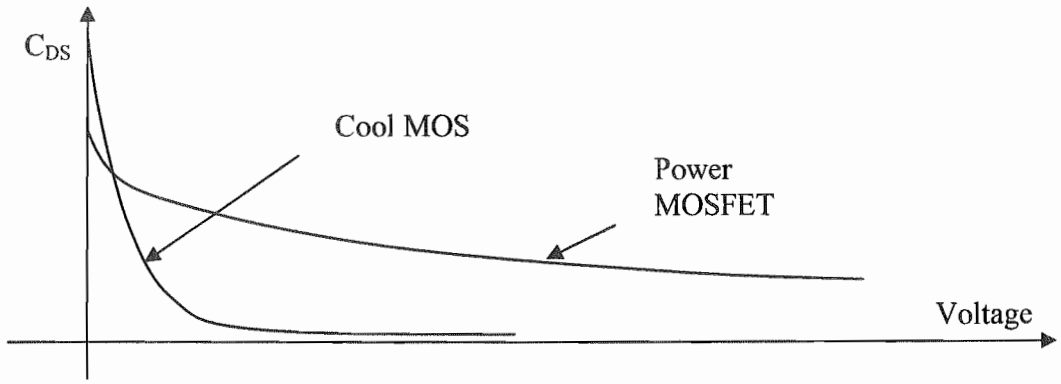
4. (a) (i) The Cool MOS is based the superjunction effect. The superjunction comprises multiple junctions disposed in the drift region with alternate layers of relatively highly doped n and p layers. The drift region is therefore made of thin and highly doped n/p stripes rather than a single n- layer. The depletion of the drift region is in this case dictated by these n/p multiple junctions rather than by the classical p+/n- junction. Since the stripes are very thin (compared to their length), they deplete at much lower voltage (due to the extension of the depletion region across the n/p junctions). The net advantage is a major reduction in the on-state resistance for the same breakdown capability. The electric field distribution is square rather than triangular, and the doping of the n pillars is considerably higher than that of the classical power MOSFET. For the same breakdown a reduction of 5-10 times in the on-resistance is possible.

The Cool MOS is shown below:



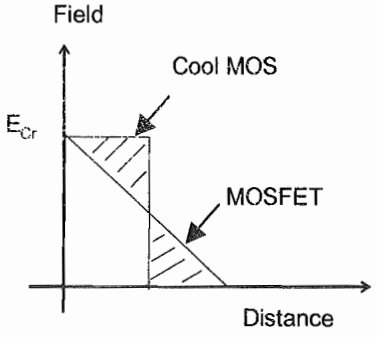
[25%]

(ii) The C_{DS} capacitance for the Cool MOS is high to start with, as the multiple junctions have a large (folded) area. At the same time the doping of the n and p pillars are very high limiting the extension of the depletion region at low voltages. These 2 effects lead to very high C_{DS} in Cool MOS at low voltages. At high voltages, in Cool MOS, the whole n-p pillar stack depletes, thus reducing sharply the capacitance. In contrast in Power MOSFET, the capacitance at low voltages is quite low (reduced area and reduced doping), while decreasing with $1/V^2$ at high voltages.



[25%]

(b) (i) For MOSFET $w = w_{drift}$ (the depletion region at breakdown just reaches the n+ drain region)



$$V_{BQ} = \frac{E_{cr}}{2} W$$

$$V_{BR} = \frac{\varepsilon_0 \varepsilon_r E_{cr}^2}{2qN_D} \Rightarrow N_D = \frac{\varepsilon_0 \varepsilon_r E_{CR}^2}{2qV_{BR}}$$

drift length $w = \frac{2V_{BR}}{E_{CR}} \Rightarrow w_{drift} = w = \frac{\varepsilon_0 \varepsilon_r E_{CR}}{qN_D}$ - MOSFET

$w_{drift-CoolMOS} = \frac{w_{drift-MOSFET}}{2}$ (the drift width of CoolMOS is only half of that of MOSFET, as the field distribution for Cool MOS is rectangular rather than triangular – see picture above) [30%]

(ii) specific resistance for Cool MOS $= \frac{w_{drift-CoolMOS}}{q\mu_n N_{D_{CoolMOS}}} \frac{X_n}{X_n + X_p}$

$N_{D\,Cool\,MOS} = 10\times N_{D\,MOSFET}$ and $w_{drift-CoolMOS} = \frac{w_{drift-MOSFET}}{2}$

$X_n = 1/2 X_p$ (to allow charge balance in the drift region of the Cool MOS)

$$\frac{R_{spcoolMOS}}{R_{spMOSFET}} = \frac{1}{10} \times 3 \times \frac{1}{2} = \frac{3}{20} = 0.15$$ [20%]