4B6 2009 Crib

Q1

a) For a negligible V_{DS}, the threshold voltage V_T is the voltage between gate and source, V_{GS}, such that the concentration of minority carriers at the surface equals the concentration of majority carriers in the bulk.

20%

b) In these conditions:

$$|E_F - E_i|surface = |E_F - E_i|bulk = q\psi_B$$

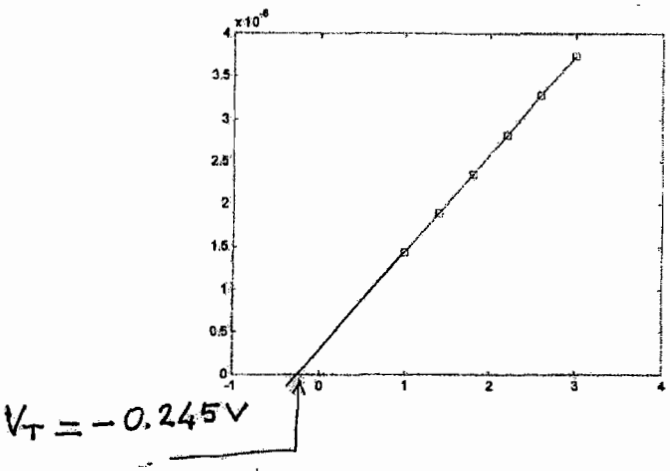
$$N_A \approx p = n_i \exp\frac{q\psi_B}{kT}$$

$$\psi_S = 2\psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i} = 0.618$$

$$Q_B = (2\,\varepsilon_S\, qN_A\psi_S)^{\frac{1}{2}} = -1.44x\ 10^{-8}\ C\,cm^{-2}$$

$$V_T = \psi_S + \frac{d}{\varepsilon_i}Q_B = 0.659V$$

40%



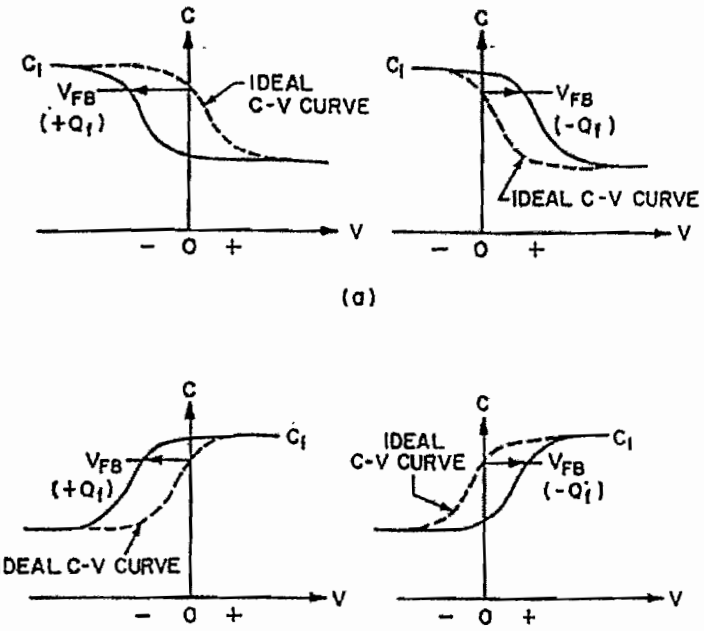
$V_T = -0.245V$

$$Q_F = \frac{\varepsilon_i}{d}\Delta V_T = 3.12\ x\ 10^{-7}\ C\ cm^{-2}$$

40%

Q2

a)



C–V curve shift along the voltage axis due to positive or negative fixed oxide charge. (a) For *p*-type semiconductor. (*b*) For *n*-type semiconductor. (After Nicollian and Brews, Ref. 7.)

35%

b)

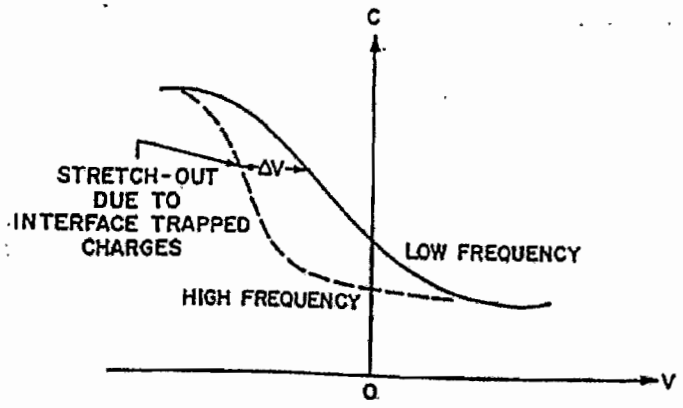
The interatomic bond lengths in SiO_2 and Si are quite different, so at the interface some bonds are not coupled into covalent bonds and remain single, or as one say 'dangling'. A dangling bond (D.B.) has only one electron . It can loose it becoming positively charged and acting therefore as a donor, or it can acquire a second electron, becoming negatively charged and acting as an acceptor. In addition dangling bond can reconstruct between them resulting in 'long' or stretched bonds. These bonds also produce energy levels in the bandgap, which can act as traps.

When a voltage is applied, the interface trap levels move up or down with the valence and conduction bands, while the Fermi Level remains fixed. A change of charge in the interface trap occurs when it crosses the Fermi level, i.e. Q_{it} is a function of ψ_S.

This means that in our MOS equations we have to add the charge term Q_{it}

$$V_G = \frac{d}{\varepsilon_i}(2\varepsilon_s q N_A \psi_s)^{\frac{1}{2}} - \frac{d}{\varepsilon_i} Q_{it}(\psi_s) + \psi_S$$

At sufficiently high frequency Q_{it} cannot follow the variation of the AC voltage swing, so the capacitance is free of contribution from the interface traps. Not so at low frequency. The presence of the additional term in the above equation results in a 'stretch-out' of the low frequency C-V curve as compared to the high frequency one. This strech-out can indeed be used to deduce the distribution of interface traps in the bandgap.



35%

Capacitance stretch-out due to interface trapped charges.

c)

1) Dangling bonds; 2) reconstructed or weak bonds; 3)disorder induced localised states.

1) They are a consequence of the presence of Si atoms with coordination lower than 4,which leaves one bond uncoordinated. Coordinated bonds are directional, uncoordinated ones are not, hence the adjective 'dangling'. These defects are believed to give rise to energy levels near midgap.

2) Some dangling bonds can reconstruct resulting in 'weak' bonds (they are called weak because they stretch over more than a perfect Si-Si tetrahedral bond distance). The energy levels associated with these are believed to span the entire energy gap.

3) These are due to a quantum mechanical effect: when the disorder-induced fluctuations of the crystal potential exceed a critical value (dependent on the atomic species involved) localized states form. These are located near the conduction and valence band edges.

These states act as electron traps . This means that for increasing density of states in the bandgap increasing gate to source voltages are needed to achieve the same free electron density in the channel, resulting in a higher threshold voltage and lower field effect mobilities (and on-currents).

4B6 Answer for Question 3 on FRAM:

(a) WRITE : WL set to High (i.e. the transistor to ON state); [20%]
Apply a positive(negative) voltage pulse between the BL and the CP, which is sufficiently high to switch the ferroelectric material of the ferroelectric capacitor to a positive(negative) polarisation direction, corresponding to the "1"("0") state;
WL set to Low (i.e. the transistor to OFF state).

READ : WL set to High (i.e. the transistor to ON state); [30%]
Apply a voltage pulse of a fixed polarity (either positive or negative) between the BL and the CP;
Use sense amplifier connected to the BL to detect its potential change and determine the value of the ; (The fixed voltage pulse will switch or not switch the polarisation in the ferroelectric capacitor, depending the information state stored in it and resulting a difference in the amount of electric charge dumped from the capacitor to the BL. Because the BL has a finite parasitic capacitance, the difference in the amount of charge translates to the different in the BL potential, which is picked up by the sense amplifier attached to it.)
If the voltage pulse has switched the ferroelectric material, applying a voltage pulse of opposite polarity to switch the polarisation back and restore the originally state of stored information;
WL set to Low (i.e. the transistor to OFF state).

(b) (i) Remnant polarisation: $Pr = 23\ \mu C\ cm^{-2}$ [10%]
Coercive field: $Ec = 150\ kV\ cm^{-1}$

(ii) The corresponding electric field for +5V is +500 kV cm^{-2} (= +5V / 100nm). [20%]

Resulting charge is:

$$\Delta Q = \Delta P * Area = (0.25\mu m * 0.25\mu m)\ \Delta P = 6.25 \times 10^{-10}\ cm^2 * \Delta P$$

For State "1" (positively polarised) with CP=+5V and BL=0V,

$$\Delta Q_{"1"} = 6.25 \times 10^{-10}\ cm^2 * \Delta P_{"1"} = 6.25 \times 10^{-10}\ cm^2 * (38+23)\ \mu C\ cm^{-2}$$
$$= 38 \times 10^{-15}\ C = 38\ fC$$

For State "0" (negatively polarised) with CP=+5V and BL=0V,

$$\Delta Q_{"0"} = 6.25 \times 10^{-10}\ cm^2 * \Delta P_{"0"} = 6.25 \times 10^{-10}\ cm^2 * (38-23)\ \mu C\ cm^{-2}$$
$$= 9.4 \times 10^{-15}\ C = 9.4\ fC$$

(iii) Energy consumed due to switching of polarisation from negative to positive direction can be approximated in the order of: [20%]

$$\Delta E \sim 2 * Pr * Ec * Volume = 2 * Pr * Ec * Area * Thickness$$
$$= 2 * 23\ \mu C\ cm^{-2} * 150\ kV\ cm^{-1} * 6.25 \times 10^{-10}\ cm^2 * 100 \times 10^{-7}\ cm$$
$$= 4 \times 10^{-14}\ J = 40\ fJ$$

4B6 Answer for Question 4 on MRAM:

(a) (i) A magnetic tunnel junction (MTJ) consists of two conductive magnetic layers (Co layers here) with a non-conductive non-magnetic tunnel layer (Al_2O_3 layer here) in between. The magnetisation is usually switchable only in one layer. [10%]

CPP configuration: Apply voltage across the two magnetic layers and measure the resulting current which tunnels through the non-conductive layer;.

CIP configuration: Apply voltage on the same magnetic layer and measure the resulting tunnelling current.

(ii) The lower Co layer in the CIP configuration can have effect on the measured current. This is because the non-conductive tunnel layer is thin, in comparison to the electron coherence length. The spin polarisation state of the electrons flow from one electrode to the other can be altered when they are scattered of from the lower Co layer during transportation, resulting a change in scattering coefficient (depending on the magnetisation direction in the lower Co layer) when they return to the upper Co layer, hence the change in the magnitude of the measured current. Note that this is a pure quantum effect without classical correspondence. [20%]

(iii) A bit of information is physically stored in terms of the direction of magnetisations in the upper and lower Co layers. For example, the parallel (anti-parallel) configuration can be referred as State "1" (State "0"). [20%]

The magneto-resistance in a MTJ (in either the CPP or the CIP configuration) is low (high) when the magnetisation directions in the two magnetic layers are parallel (anti-parallel). Therefore, the stored bit of information can be represented by the two levels of MTJ resistance.

(b) (i) To write a bit of information is to switch the magnetisation in one of the magnetic layers (the upper one here) to the desired direction. [30%]

To avoid switching the half-selected cells, switching is performed by using a combined magnetic field induced by the electric current in the corresponding D-Line and B-Line (neither of them can do the switching on its own as shown on the right in Figure 4).

In the case of writing into B2-W2, using D2 to induce a magnetic field and switching the magnetisation half way and followed by using B2 to induce a separated magnetic field in the desired direction to complete the switching.

(ii) Select W2 to High (i.e. the transistor to ON state), apply a voltage on B2 and measure the current through it. The current level corresponds to the resistance of the MTJ at B2-W2, hence the bit of information stored in it. [10%]

(iii) A MTJ should be rectangle in shape, so that the magnetisation in the switchable layer only has two easy directions, representing the state of stored binary information. [10%]