Crib:

Q1:
(a) Assume parallel plate capacitor with doped GaAs as the metal layers and undoped AlAs as the dielectric layer.
Then with $C=\varepsilon A/d$, the side of square capacitor must be 10nm from the data given.

Use e-beam lithography to lay down 10nm square pads, and use dry etching to below the depth of the AlAs layer.
Probably need to contact to pad before dry etching, as probe measurements are impractical.
Legitimate question: Might there be electronic damage from the etching in from the dry etching?

(b) The ultimate test is by measuring the capacitance by C-V profiling, but one could check that the physical shape was correct in a high resolution SEM.

(c) The square shape of 10nm is only 30 atoms side by side. This is advanced routine in advanced silicon transistor technology, but even here an error of +/- 2-3 layers at each edge translates to a 30% error in the total area. Uniformity and reproducibility would be a major problem.

(d) $Q=CV$ so for $Q=ne$, we have $V=n\,(e/C)$, and for $n=1, 2, 3$ we need $V= n0.625$ volts. A large voltage for each extra electron.

(e) We consider the possibility of getting an electron from one contact into the central quantum well. The kinetic energy of quantum confinement in one dimension, normal to the multilayers, for a well of 10nm is 50meV. [Note for a first: multiply by 3 for the confinement in the other two dimensions, as we really have a quantum dot.]
Since $kT < KE$ of quantum confinement, a significant bias will be needed to put one electron on what is now a quantum dot. This electron will have to tunnel out the other side before another electron would be able to enter the dot.

Q2:
(a)
1st: $V_M f_T = E_B v_s / 2\pi$,
2nd: $PZ(f_T)^2 = (E_B v_s)^2 / 32\pi^2$.

V_M= maximum voltage applied across device.
f_T the maximum frequency to which the device can respond.
P=power into an impedance Z.
E_B = dielectric breakdown strength of semiconductor
v_s=saturated drift velocity of semiconductor

Assume a piece of material of length L. The maximum voltage we can apply to this material is $V_M = E_B L$, and the time that is characteristic of the carriers crossing this material is $\tau = L/v_s$, for which the associated frequency is $f_T = 1/(2\pi\tau)$.

For a device made of this material, there is a limitation on the maximum voltage applied at the device speed: $V_M f_T = E_B v_s / 2\pi$, the first Johnson criterion.
If V_M is considered the peak-to-peak voltage swing in an ac device, the rms voltage is $V_M(2\sqrt{2})$. The maximum power delivered to an output impedance Z is given by $P = (V_M)^2/8Z$. Substituting for V_M we arrive at the second Johnson criterion: $PZ(f_T)^2 = (E_B v_s)^2 / 32\pi^2$.
The product of maximum drive voltage and operating frequency of any transit time device is limited by strictly materials properties. Similarly, there is not unlimited power available from high-speed devices, indeed there is a hard trade-off.
The only way to move is to change materials, and hence the interest in SiC and GaN where the $E_B v_s$ figure of merit can be 15 times higher than in Si or five times higher than GaAs.

(b) From the ratio square, one should get 12.5W of energy from the device.
Problems of making good ohmic contacts capable of withstanding the very high currents and the power densities implicit in a GaN Gunn diode have not be overcome to date.

(c) A GaAs Gunn diode relies of a high field to accelerate electrons into the satellite valley as 0.3eV above the minimum central valley at the bottom of the conduction band. For very high frequency devices, the distance needed to heat the electrons can be a fraction of the entire transit length (1.2μm for 100GHz second harmonic devices). By using a 50nm layer of $Al_xGa_{1-x}As$ with x graded from 0 to 0.3 over that length, followed by a heterojunction reverting sharply to x=0, one can inject electrons hot, with energy 0.3eV into the transit region and get effective transfer into the satellite valley.
In practice, limit on fundamental mode operation rises from 60Hz to 90GHz.
The hot electrons are at 3000K after the heterojunction and the lattice temperature does not matter – the devices are much less sensitive to the ambient temperature.
The fact that the electrons are cold up to the heterojunction a nd then suddenly heated, prevents the emission of optic phonons the principal source of sideband noise in GaAs Gunn diodes. This is reduced by a factor of three in the heterojunction devices.

Q3:

(a) Detector or mixer needs curvature in the I-V characteristics, i.e. non-linearity, and preferably near V=0, so that zero bias operation is possible.
Sources need negative differential resistance so that the normal exp(-t/RC) damping of a signal can be converted into a growing signal.

(b)
From my lecture notes:.
Single AlAs barrier with GaAs on either side, asymmetrically doped, produces curvature near the origin – demonstrated as an effective detector with wide dynamic range, low noise, low temperature sensitivity etc, but unmanufacturable.
Double barrier AlAs resonant tunnelling diode with GaAs as the well material between the AlAs barriers and as the contact layer on either side, shown to work as a microwave source up to 500GHz.

(c) For device design, TEM, and X-ray techniques are sued to produce layer thicknesses, while X-ray techniques are rapid enough, and non-destructive to be used in an in-line analysis mode.
For doping, SIMS is fine off-line and simply C-V profiling in-line, or some form of infrared spectroscopy for the contact layer doping.

(d) The layers are too thin to control adequately. Tunnelling itself is extremely sensitive to local layer thickness, with X3 variation of current density per monolayer. The uniformity has top be on the scale of 10nm across the wafer, as that is the coherence diameter of tunnelling electrons. The finite control over epitaxy at this level reduces the yield, uniformity and reproducibility of device within wafer and from wafer-to-wafer.

(e) Schottky barriers and planar-doped-barriers rely on thermionic emission a=over a barrier and are more temperature sensitive that tunnel diodes. The (Esaki) germanium backward diode is exceptionally temperature independent and relies on tunnelling between the conduction and valence bands in a reversed biassed p+/n+ junction.

Q4: Moore's law
Nearly every quarter, most electronics magazines run a feature on this topic. There are an enormous number of www pages to which one can refer.
Here are just three, got by Googling 'After Moore's law'.
http://www.processor.com/editorial/article.asp?article=articles%2Fp2713%2F39p13%2F39p13.asp
http://www.cl.cam.ac.uk/~mvw1/lect-Moores-law-and-the-future.pdf (by the father of CXambridge Computing, Prof Maurice Wilkes)
http://lowendmac.com/musings/moore.shtml

Q5

(a)

Much lower power consumption for FET based devices.
High speeds possible with FETs.
Very high speeds from BT.

(b)

Field effect:
Higher currents in the channel are possible
Higher biases in the channel before hot electron effects occur.
Lower mass semiconductor possible in channel without compromising hot electron and other effects.

Bipolar:
Better emitter efficiency without back injection from base
Higher doping in base allowed
Less perimeter effect from sideways voltages in the base
Higher speed of response
Higher and lower temperature of operation compared with homojunction transistor.

(c)

GaAs FETs faster by factor 3 for same commitment to lithography.
Lower power consumption when signal processing at high speeds.
Lower noise at high frequency.
Optically active for all optoelectronic applications and GaAs and related materials directly compatible with optical devices for on-chip modulation and signal processing for the optical element drives.

(d) Standard diagram of ft versus gate length showing improvement in mobility of InGaAs over GaAs, and the higher heterojunction barrier for AlInAs than AlGaAs allowing for greater channel density and higher source-drain drive voltages.