ENGINEERING TRIPOS PART IIB

Monday 20 April 2009 9 to 10.30

Module 4B2

POWER MICROELECTRONICS

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS
Single-sided script paper

SPECIAL REQUIREMENTS
Engineering Data Book
CUED approved calculator allowed

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) Discuss briefly the differences between a punch-through (PT) high voltage junction and a non-punch-through (NPT) high voltage junction. Which of the two is preferred in the design of a Bipolar Junction Transistor (BJT) and why? [40%]

(b) Either a power MOSFET or an Insulated Gate Bipolar Transistor (IGBT) are to be used in an inductive application with the current and voltage turn-off waveforms shown schematically in Figure 1. The rail voltage V_{dc} = 400V and the on-state current required for the application is I_{ON} = 3A. The static and dynamic parameters of the two transistors are summarised in table 1. Consider that the turn-on and the off-state losses are negligible for both transistors. The switching frequency is variable from 10 kHz to 100 kHz with a constant duty cycle of D = 50%.

Table1

Parameter	On-state voltage drop V_{ON} [V]	Turn-off delay time t_s [μs]	Turn-off voltage growth time t_g [μs]	Turn-off current fall time t_f [μs]
Power MOSFET	5	0.1	0.3	0.1
IGBT	2	0.1	0.3	0.6

(i) Estimate the total power losses in the Power MOSFET and the IGBT and sketch a graph of these as a function of frequency. Comment on the efficiency at these transistors and the preferred use of one or the other for the given range of frequency. [40%]

(ii) The parameters in Table 1 are given at room temperature. How would you expect the on-state and the turn-off power losses to change at higher junction temperatures for the two transistors? Will the junction temperature influence the choice of the transistor? [20%]

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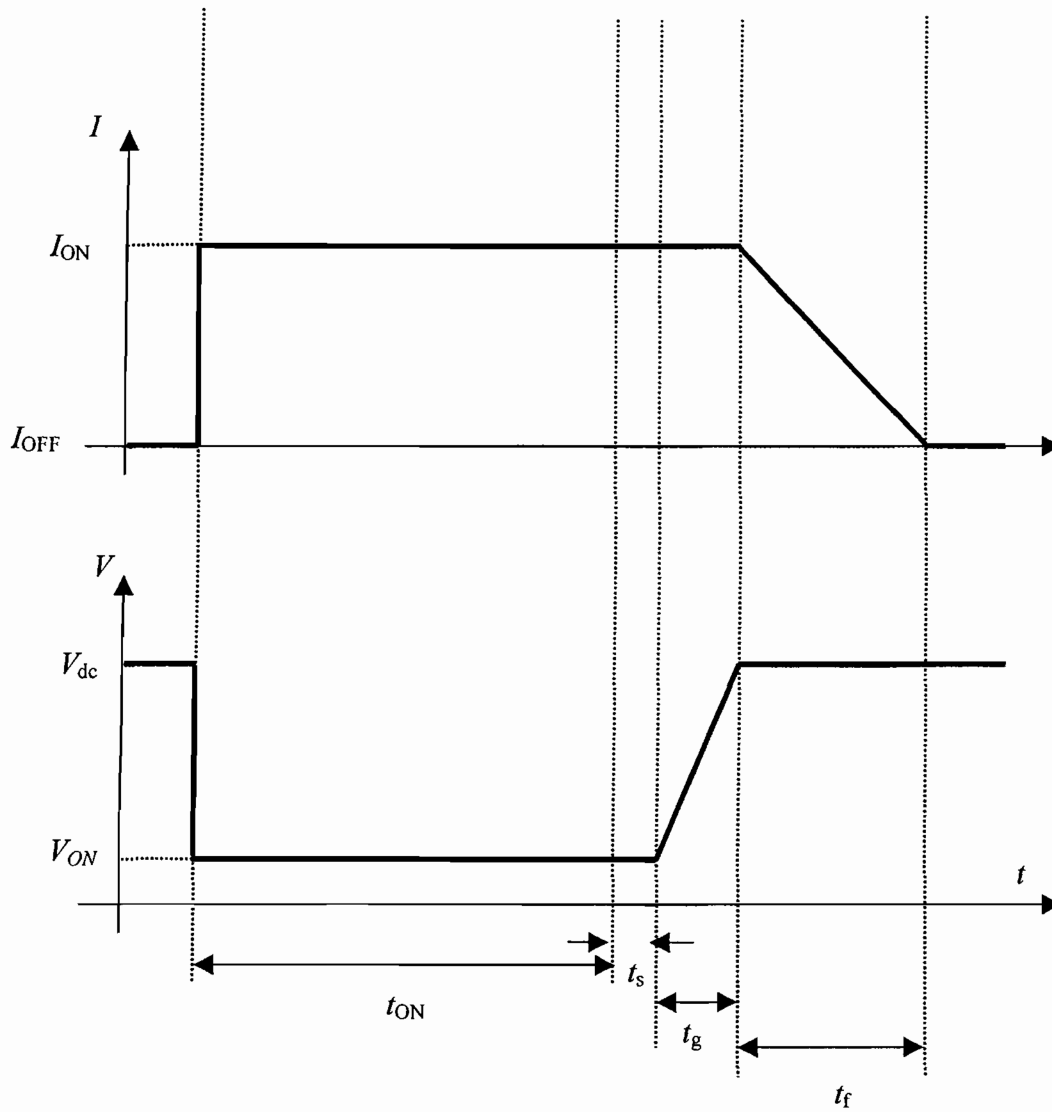


Figure 1

(TURN OVER

2 (a) Explain the dI/dt effect in thyristors. Give two solutions to improve the dI/dt ratings and discuss their advantages and disadvantages. [30%]

(b) (i) Using the simplified Ebbers-Moll equivalent models for the two bipolar transistor components of the thyristor, find an expression for the anode current in the voltage blocking mode as a function of the leakage currents of the bipolar transistors and their current gains α_{npn} and α_{pnp}. [30%]

(ii) Calculate the break-over voltage, V_{BO}, of the thyristor, assuming that α_{npn}= 0.5 remains constant. The width of the n- drift region is w_{drift} = 200 μm, the hole diffusion length Lp = 50 μm and the doping concentration of the drift region, N_D= 10^{13} cm^{-3}. [30%]

(iii) Discuss briefly the occurrence of break-over and avalanche breakdowns in the drift region of a thyristor and that of a PIN diode. [10%]

You may assume the following equations in the calculations of breakdown and current gain of a pnp transistor

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

$$\alpha_{pnp} \approx 1 - \frac{w_{eff}^{\ 2}}{2L_p^{\ 2}}$$

where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, α_{pnp} is the current gain of the pnp transistor, w_{eff} is the effective base width of the pnp transistor, L_p is the hole diffusion length, q is the electronic charge and the other symbols have their usual meaning. ε_0 = 8.854 x 10^{-12}F/m, ε_r=11.9 for Silicon.

3 The structure in Figure 2 is a MOS controllable power device with a trench gate.

(i) Explain briefly its operation during on-state, off-state, turn-on and turn-off. [40%]

(ii) Draw an equivalent circuit for the device. [25%]

(iii) Give one advantage and one disadvantage of this device compared to a conventional Trench Insulated Gate Bipolar Transistor (IGBT). [10%]

(iv) The device in Figure 2 is based on trench gate technology. Draw an equivalent device using a planar gate technology. Give three advantages and one disadvantage of the trench gate structure compared to a planar (DMOS) gate structure. [25%]

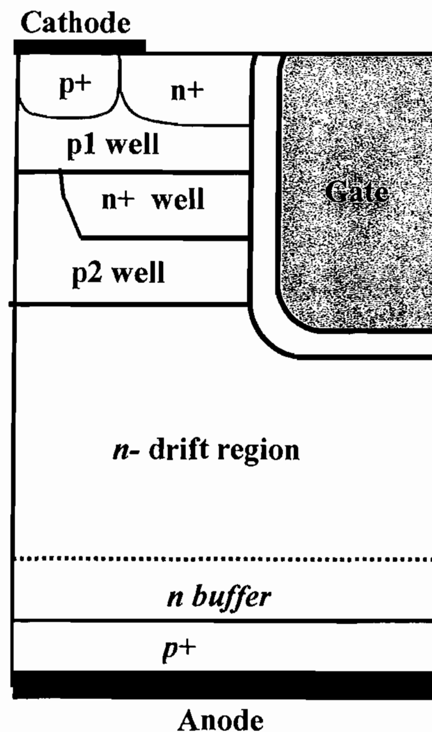


Figure 2

4 (a) (i) Draw the structure of the Cool MOS and explain its advantage in terms of the trade-off between the specific on-state resistance and the breakdown voltage. [25%]

(ii) Draw schematically a graph of the drain-source capacitances as a function of the blocking voltage for both the Cool MOS and a conventional Power MOSFET. Explain briefly the different behaviour of the two capacitances at low voltages and high voltages. [25%]

(b) (i) A power MOSFET and a Cool MOS are to be designed to have the same breakdown voltage V_{BR}. Assuming that the critical electric field, E_{cr} remains constant, independent of the doping level, find the optimal doping level and the optimum width of the drift region for the power MOSFET. What is the optimum width of the drift region for the Cool MOS to deliver the same V_{BR}? [30%]

(ii) Assume that the doping levels of the Cool MOS n-pillar and p-pillar are ten and five times higher than the doping level of the drift region in the power MOSFET respectively. Find the relative decrease in the specific drift on-state resistance of the Cool MOS with respect to that of the Power MOSFET. [20%]

You may assume the following equation in the calculation of the breakdown voltage

$$w = \left[\frac{2\varepsilon_r \varepsilon_0 V}{q} \frac{1}{N_D} \right]^{\frac{1}{2}}$$

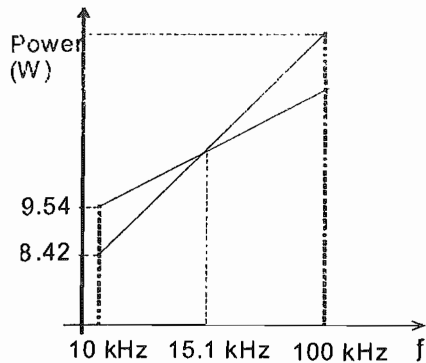
where w is the depletion region width; N_D is the doping concentration of the drift region, V is the blocking voltage, q is the electronic charge and the other symbols have their usual meaning.

END OF PAPER

List of Numerical answers

Question 1

b) $MOS: 7.5 + 243.75\times10^{-6} f$
$IGBT: 3 + 542.4\times10^{-6} f$



Question 2

b) $V_{Breakover} = 170.83$ V

Question 4

b) (i) $N_D = \dfrac{\varepsilon_0\varepsilon_r E_{CR}^2}{2qV_{BR}}$ and $w = \dfrac{2V_{BR}}{E_{CR}} \Rightarrow w_{drift} = w = \dfrac{\varepsilon_0\varepsilon_r E_{CR}}{qN_D}$ for the Power MOSFET

$$w_{drift-CoolMOS} = \frac{w_{drift-MOSFET}}{2}$$

b) (ii) $\dfrac{R_{spcoolMOS}}{R_{spMOSFET}} = \dfrac{1}{10}\times 3 \times \dfrac{1}{2} = \dfrac{3}{20} = 0.15$