ENGINEERING TRIPOS PART IIB

Monday 4 May 2009 9 to 10.30

Module 4B7

VLSI DESIGN, TECHNOLOGY AND CAD

*Answer not more than **three** questions.*

All questions carry the same number of marks.

*The **approximate** percentage of marks allocated to each part of a question is indicated in the right margin.*

There are no attachments.

STATIONERY REQUIREMENTS	SPECIAL REQUIREMENTS
Single-sided script paper	Engineering Data Book CUED approved calculator allowed Supplementary pages: None.

You may not start to read the questions printed on the subsequent pages of this question paper until instructed that you may do so by the Invigilator

1 (a) With a series of diagrams, show the process route by which an MOS transistor is made, including brief notes on the individual process steps. [30%]

(b) If this transistor were part of a CMOS circuit, what other process steps would be involved? [20%]

(c) Discuss the factors that must be considered in determining the order in which the various steps in (a) and (b) above are performed. [20%]

(d) Viewed from the year 2009, what factor is most likely to bring to an end the continued miniaturisation of MOS transistors? What is likely to happen in electronics once a minimum gate-length is reached? [30%]

2 (a) Describe the critical success factors in achieving customer satisfaction at a wafer fabrication plant. [20%]

(b) Describe the considerations that go into determining the layout of equipment in a wafer fabrication facility. [20%]

(c) Discuss the role of metrology and analysis, both in-line and off line. [40%]

(d) Describe the processes of calibration and recalibration of equipment in both the start-up phase, and when restarting after planned maintenance. [20%]

3 (a) What is meant by the term *design rule* in CMOS integrated circuit layout? Write a short account of the ways in which design rules constrain the general form and dimensions of interconnect and contact structures in CMOS technologies. [60%]

(b) Show how the following structures and phenomena give rise to specific design rules:

(i) well and substrate taps;

(ii) process-induced gate-oxide damage;

(iii) contact cut;

(iv) power pad. [40%]

In your account indicate the origins of the rules you introduce, making it clear how they arise from physical, electrical or processing constraints. **Note**: details of specific manufacturers' rules are not required.

4 (a) Write notes on the following failure modes as they apply to VLSI products:

(i) EM (Electromigration)

(ii) Corrosion

(iii) HCI (Hot Carrier Injection)

(iv) TDDB (Time dependent Dielectric Breakdown)

(v) ESD (Electrostatic discharge) [50%]

(b) The circuit in Fig. 1 shows a simple Class A amplifier to be used as a low power output stage in an integrated operational amplifier. V_{GG} is a fixed bias supply of +2 volts. The output stage drives a purely capacitive load C_L of 200 pF, and is required to deliver an output voltage swing of ± 2 volts with a maximum slew rate of 3×10^6 V s^{-1} under these conditions.

Determine a suitable quiescent operating current I_D for the circuit, assuming that the minimum acceptable current is to be used consistent with achieving the required slew rate. If transistors M1 and M2 each have channel lengths of 10 μm, deduce appropriate channel widths W_1 and W_2. State any other assumptions made. [30%]

Estimate the a.c. gain and the small-signal output resistance of the amplifier. [20%]

The following device parameters apply to devices M1 and M2.

M1: $V_T = +1$ V, $\lambda = 0.01$ V^{-1}, and $\mu_N \varepsilon / t_{OX} = 15 \times 10^{-6}$ AV^{-2}.
M2: $V_T = -1$ V, $\lambda = 0.02$ V^{-1}, and $\mu_P \varepsilon / t_{OX} = 6 \times 10^{-6}$ AV^{-2}.

You may assume the following expressions for the drain current I_D in a MOS transistor.

$$I_D = \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right) (1 + \lambda V_{DS}) \qquad 0 < V_{DS} < V_{GS} - V_T$$

$$I_D = \frac{1}{2} \frac{\mu\varepsilon}{t_{OX}} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \qquad 0 < V_{GS} - V_T < V_{DS}$$

(cont.

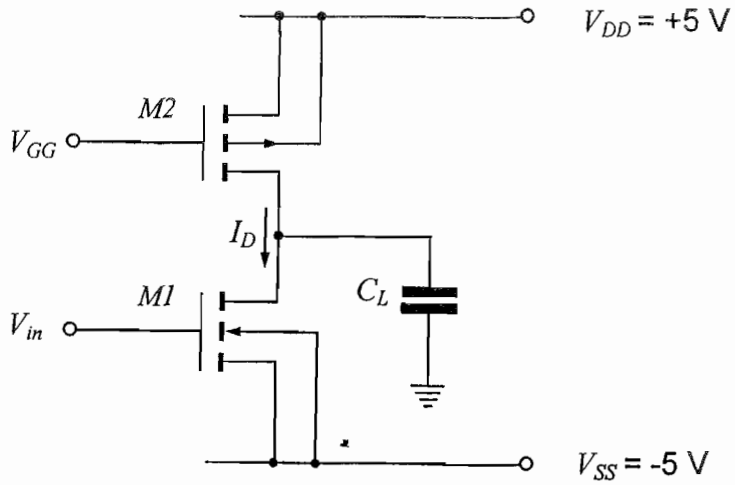

Fig. 1

5 (a) Show that the conductance G of a MOS transistor of aspect ratio W/L in the ON state can be approximated by the expression:

$$G = \mu C_{OX} V_{DD} (W / L)$$

where μ is the electron mobility, C_{OX} is the capacitance per unit area of the gate and V_{DD} is the power supply voltage. [30%]

(b) A multi-stage CMOS output pad driver consists of a number of appropriately designed inverters connected in cascade. It is to transmit the signal from the output of an inverting gate consisting of minimum geometry transistors to a pad, which, together with external circuitry, imposes a purely capacitive load of 75 pF. The capacitance to substrate at the input to the inverting gate is 0.2 pF, and the channel dimensions W and L of the n-channel transistor used in its construction are 1 μm and 0.5 μm respectively.

(i) Estimate the delay that would be observed if the output of the minimum geometry inverter were connected directly to the output pad. [20%]

(ii) Stating any assumptions made, show how to find the number of stages required in the driver to minimise the delay, and estimate the minimum delay achieved. [50%]

You may assume that circuit capacitances are dominated by the pad and transistor gate electrode capacitances, and that the delay imposed on a signal by a CMOS inverter driving a capacitive load C is given by $3C/G$, where G represents the conductance of the MOS devices involved. Take $\mu_N / \mu_P = 2$, $\mu_N C_{OX} = 10^{-4}$ AV^{-2} and $V_{DD} = 3$ V.

END OF PAPER

4B7 VLSI Design, Technology and CAD - 2009 Numerical Answers

1.

2.

3.

4. (b) M2=472 x 10 μm; M1=95 x 10 μm. S-S gain – 7.15; Rout = 55.5 kΩ

5. (i) 375 ns. (ii) 6 stages, 16.2 ns (including the min geom. stage)