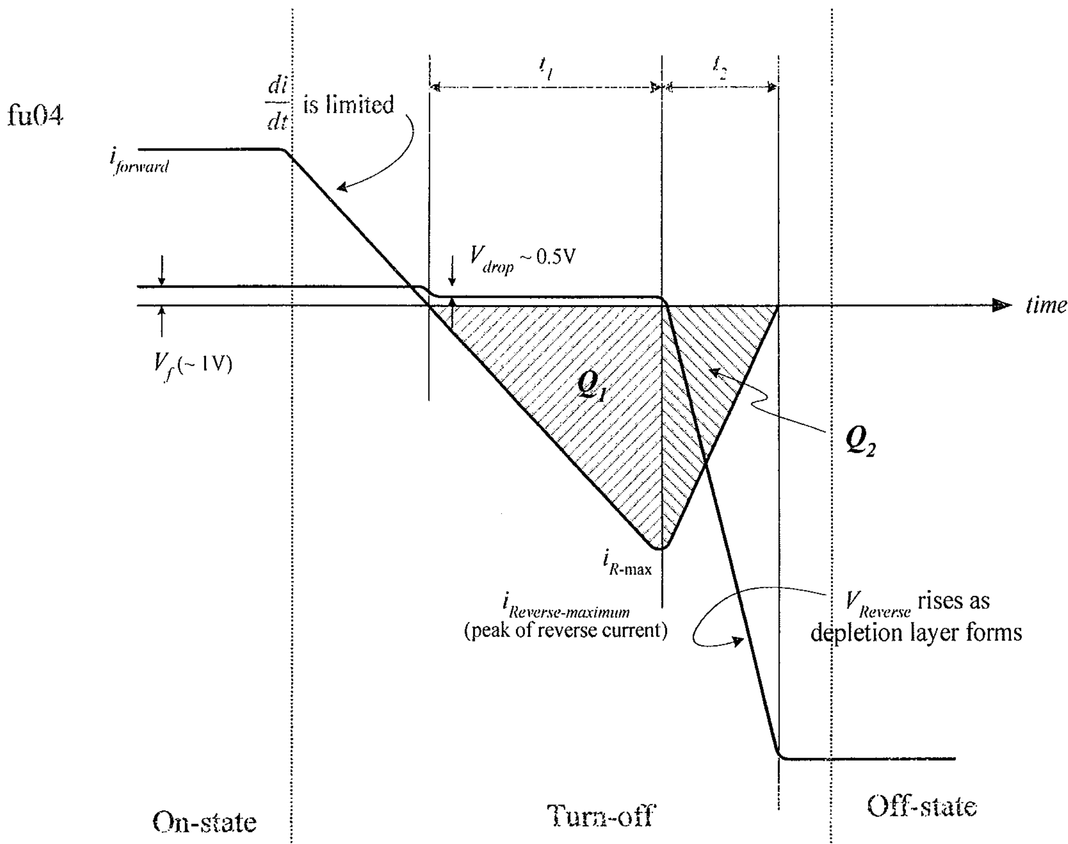
PART IIB 2010 4B2 POWER MICROELECTRONICS

PROF F UDREA

1.

(a)

fu04



Turn-off

- di/dt is limited by the external circuit. As an attempt is made to reverse-bias the diode, the current starts decreasing and flows in the opposite direction as plasma is still present.
- Q1 is associated with the plasma in the drift region and t1 is the time taken to remove it.
- Once plasma is removed at the end of t1, a depletion region starts to grow and the reverse voltage across the diode can increase. At the end of this region the device can block the voltage and the current decreases to a leackage level. [30%]

(b) $f = \frac{1}{T} = 10\text{kHz} \Rightarrow \text{T} = 100\,\mu s$, $D = 50\%$,

$DT = t_{on} + t_r + t_d = 50\mu s \Rightarrow t_{on} = 50 - 0.1 - 0.1 = 49.8\mu s$

$(1-D)T = t_{off} + t_s + t_g + t_f = 50\mu s \Rightarrow t_{off} = 50 - 0.1 - 0.2 - 0.1 = 49.6\mu s$

<u>ON -STATE</u>

$$P_{ON} = \frac{1}{T}\int_0^{t_{ON}} V_{ON} I_{ON}\, dt = V_{ON} I_{ON} \frac{t_{on}}{T} = 5\times 1\times 0.498 = 2.49W \ ,$$

<u>TURN – ON</u>

$$P_r = \frac{1}{T}\int_0^{t_r} V_{dc} \frac{I_{ON}t}{t_r} dt = t_r f I_{ON} \frac{V_{dc}}{2} = 0.15W$$

$$P_d = \frac{1}{T}\int_0^{t_d} I_{ON} [V_{dc} + (V_{ON} - V_{dc})\frac{t}{t_d}] dt = t_d f I_{ON} \frac{V_{dc} + V_{ON}}{2} = 0.1525W$$

<u>TURN – OFF</u>

Delay time: $P_s = V_{ON} I_{ON} t_s f = 0.005W$ (negligible)

Growth time:

$$P_g = \frac{1}{T}\int_0^{t_g} I_{ON}\left(V_{ON} + \frac{V_{dc} - V_{ON}}{t_g} t\right) = t_g f I_{ON}\left[\frac{V_{dc}}{2} + V_{ON}\right]$$

$$P_g = 0.2\times 10^{-6} \times 1\times 155\times 10\times 10^3 = 0.31W$$

Fall time :

$$P_f = tf \times f \frac{V_{dc}\times I_{ON}}{2}$$

$$P_f = 0.1\times 10^{-6} \times 10\times 10^3 \times 150\times 1 = 0.15W$$

<u>Total losses (on-state + turn-on + turn-off)</u>:

P total= 2.49+ 0.15+ 0.153+0.31+0.15 = 3.253W [40%]

(i) On-state losses are much higher than the switching losses –this means that the switching frequency is too low. Balancing the losses will lead to a better design.

(ii) <u>Advantage:</u> (1) Increasing the frequency will shrink the size of the transformer and capacitors. This will lead to potentially lower cost, lower volume and weight. <u>Disadvantages:</u> However over increasing the frequency will lead to too high switching losses and therefore poorer efficiency. Overheating will also result, and as a result, better heat sink will be needed. In addition overheating could result in reliability problems. Furthermore increasing the switching frequency could also lead to EMI issues. [30%]

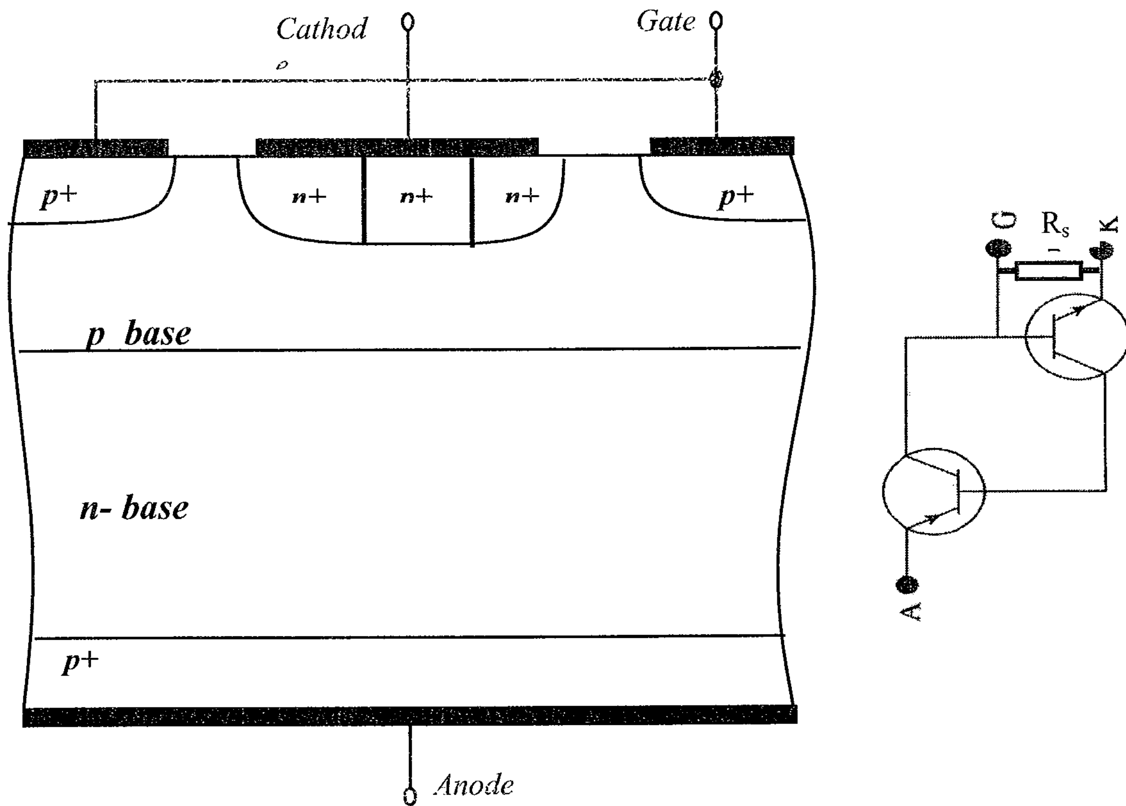
Examiner's comment:

This question was answered by all the candidates to a very high standard. It was pleasing to see that the candidates had good knowledge of calculation of losses in inductive switching applications.

2. (a)

This effect appears during turn-off when a high forward voltage is re-applied to the structure. There is a maximum *dV/dt* rating above which the displacement current of the form CdV/dt created through the junction capacitance will be greater than the breakover current, thus resulting in a parasitic re-turn-on (the device refuses to turn-off).

(1) One solution to minimize the effect of the *dV/dt* is to use cathode shorts as shown below:



The shorts can collect some of the displacement current which could otherwise turn-on the npn transistor. The smaller the short resistance R_s, the more effective the cathode short is, and the higher the maximum dV_F/dt rating.
There are two more advantages resulting from the use of cathode shorts:

(i) the increase in the breakover point – this gets closer to the maximum breakdown

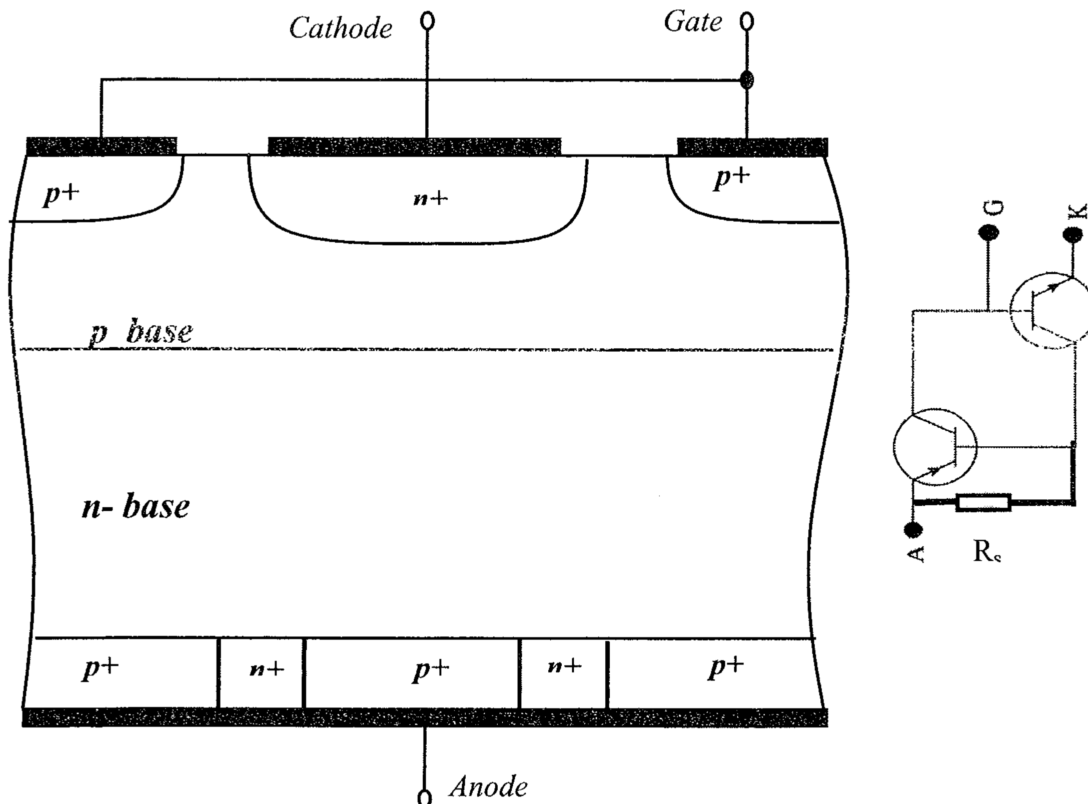
(ii) a faster turn-off. This is due to lower plasma injection

There are however two major drawbacks:

(i) the turn-on is slightly slower.

(ii) The on-state losses are slightly higher as the npn transistor has lower gain.

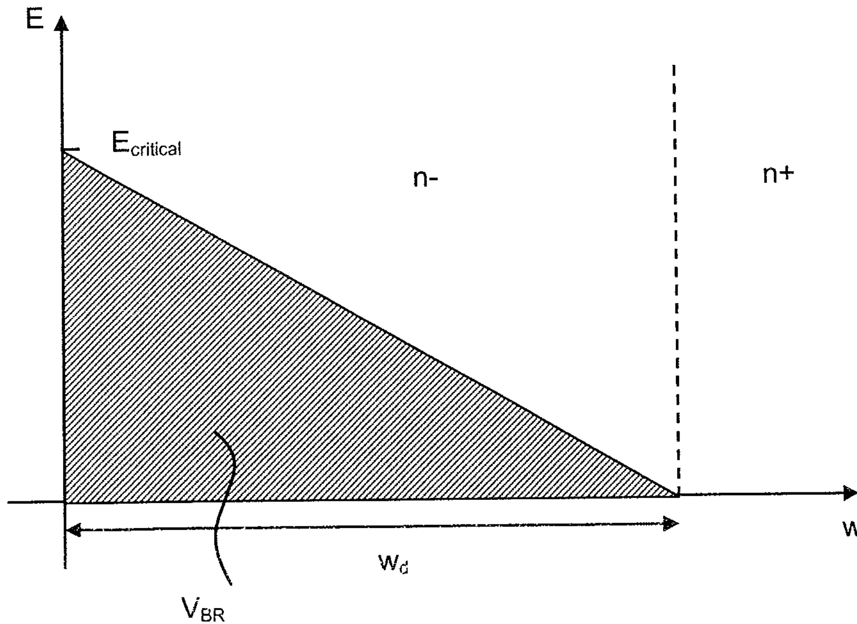
Similarly to the cathode-shorted thyristors, the anode-shorted devices are used to increase *dV/dt* rating as well as the turn-off speed and the breakover voltage. This time the gain of the pnp transitor is lowered:



The anode shorts allow higher level of cathode-gate interdigitation as no top surface area is wasted to form the cathode shorts.

Anode shorts are slightly more difficult to fabricate as they require a photolithographic process on the back side of the wafer, but they offer good overall trade-off between robustness & turn-off speed on one hand and turn-on and on-state losses on the other hand. This is certainly one of the preferred solutions for GTOs. [40%]

(b To minimize the on-state resistance, an NPT design should be used with the electric field at breakdown just "touching" the n+ drain contact region. Therefore, the drift width w_d should equate $w_{critical}$.



$w_d = w_{critical}$

$$V_{BR} = \frac{E_{critical} w_d}{2} \quad (1)$$

But $w_d = \sqrt{\frac{2\varepsilon_0 \varepsilon_r V_{BR}}{qN_D}}$

replace w_d in (1) and calculate V_{BR}^2

$$\Rightarrow V_{BR} = \frac{E_{critical}^2}{2} \frac{\varepsilon_0 \varepsilon_r}{qN_D} \quad (2)$$

but $R_{specific} = \frac{w_d}{q\mu_n N_D} = \frac{2V_{BR}}{E_{critical} q\mu_n N_D}$

$\Rightarrow q N_D = \frac{2V_{BR}}{E_{critical}\mu_n R_{specific}}$ replace in (2)

$$V_{BR} = \sqrt{\frac{E_{critical}^3}{4} \varepsilon_0 \varepsilon_r \mu_r R_{specific}}$$

$$\frac{V_{BRDiamond}}{V_{BRSilicon}} = \sqrt{\frac{E_{crdiamond}^3}{E_{Si}^3} \frac{\varepsilon_{rdiamond}}{\varepsilon_{rSilicon}} \frac{\mu_{diamond}}{\mu_{Silicon}}} = \sqrt{\left(\frac{20}{3}\right)^3 \frac{9}{12} \frac{800}{1200}} = 12.17$$

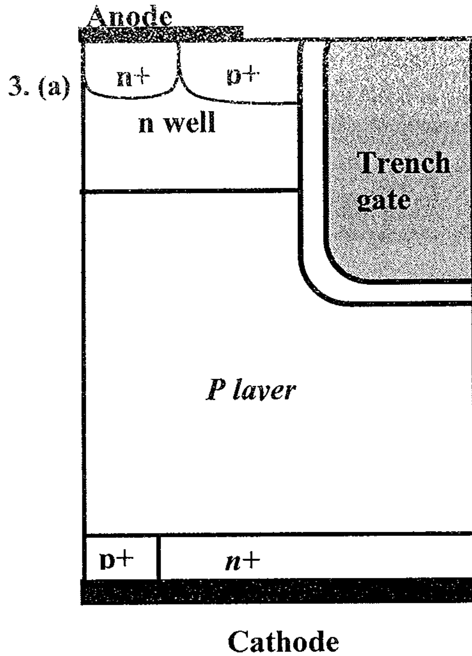
[40%]

c) Diamond is (i) very expansive (ii) very difficult to process –etch, implant, diffuse (iii) very difficult to make an Ohmic contact to (iv) very difficult to find an oxide to match (v) high threshold voltages (due to wide bandgap) [20%]

Examiner's comment:

The general answers showed a good understanding of dV/dt effect but still a lot of candidates had problems to express the breakdown voltage function of the specific on resistance.

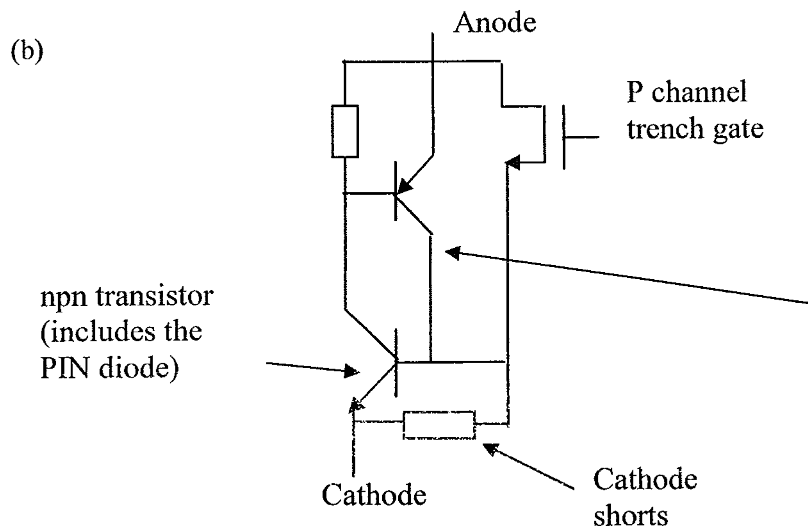
3. (a)



The device is a p-channel IGBT with cathode shorts. The Anode sits at the highest potential and the gate is referred to the anode potential. The cathode sits at lower potential than the anode. When the absolute value of the gate voltage is greater than the threshold voltage of the channel formed in the n well, alongside the trench walls, a hole inversion layer is established which connects the p+ source with the p layers. Holes are thus injected from the p+ source (connected to the anode) into the p layer which acts as drift region. Initially the holes are collected by the p+ short, but when the n+ cathode/p drift layer junction becomes forward biased, the n+ layer starts injecting electrons into the p layer modulating its resistance.

- In the off-state the device behaves similarly to an n-channel IGBT. Most of the voltage is supported across the p layer region (the n well/p layer junction is reverse biased).
- The device is turned on by applying a negative voltage onto the gate, with respect to the anode, thus forming a channel in the n well and an accumulation layer in the p well around the trench gate. This allows injection of holes into the p layer.
-In the on-state, initially the device behaves as a p-channel Power MOSFET, with the holes collected by the p+ short. The device turn into an IGBT mode, following a snap-back, when the n+ cathode/p layer junction becomes forward biased and electrons are injected into the p layer via the action of an npn transistor and n+/p layer/jole accumulation layer PIN diode. As a result heavy conductivity modulation occurs in the p layer resulting in formation of plasma.
- The turn-off of the device is achieved by bringing the gate voltage to the anode potential. Electrons are extracted during turn-off via the n+ short and the depletion starts building into the p layer clearing out the plasma. [40%]

(b)



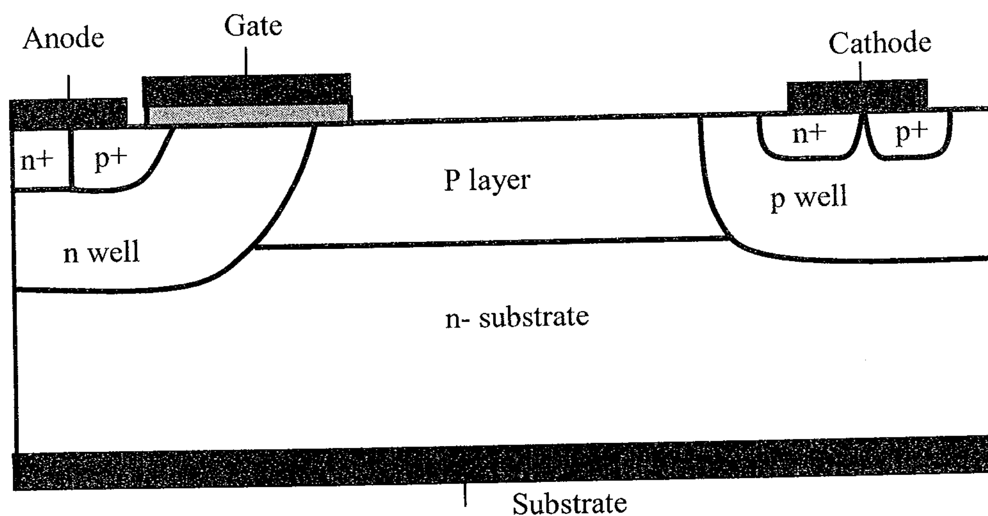
Parasitic pnp transistor. Its action is inhibited by the n+ short resistance (between its base and emitter).

[25%]

(c) Advantage: The structure can be used as a high side device without the need for a level shifter. Thus the gate of the device can be referred to the anode – which in high side is the rail voltage.

Disadvantage: The structure has a p-channel instead of the n- channel. Since the mobility of the holes is much smaller than that of the electrons (approximately by 1/3), the channel resistance and thus the voltage drop on the p-channel IGBT will be larger than that of the Trench IGBT.

The alternative lateral structure with planar technology is shown below. [10%]



Advantages of the lateral technology:

(1) Possibility of integrating CMOS circuits for drive, control, protection and processing of the signals. The power device could be turned into a power IC.
(2) Possibility of running much lower gate voltages (5 V) than those typical for the vertical devices (15V)
(3) Better tolerances and control due to the CMOS process.

Disadvantages of lateral technology

(1) Poorer on-state performance (because of larger area consumption)
(2) Presence of a second parasitic npn with the substrate – slower speed
(3) The substrate terminal needs to be connected to the highest potential to reverse the n-substrate/p layer junction.
(4) Lower on-state channel resistance due to lower gate density – this would be vene more visible in the p –channel lateral device as the mobility of the holes is lower than that of the electrons. [25%]

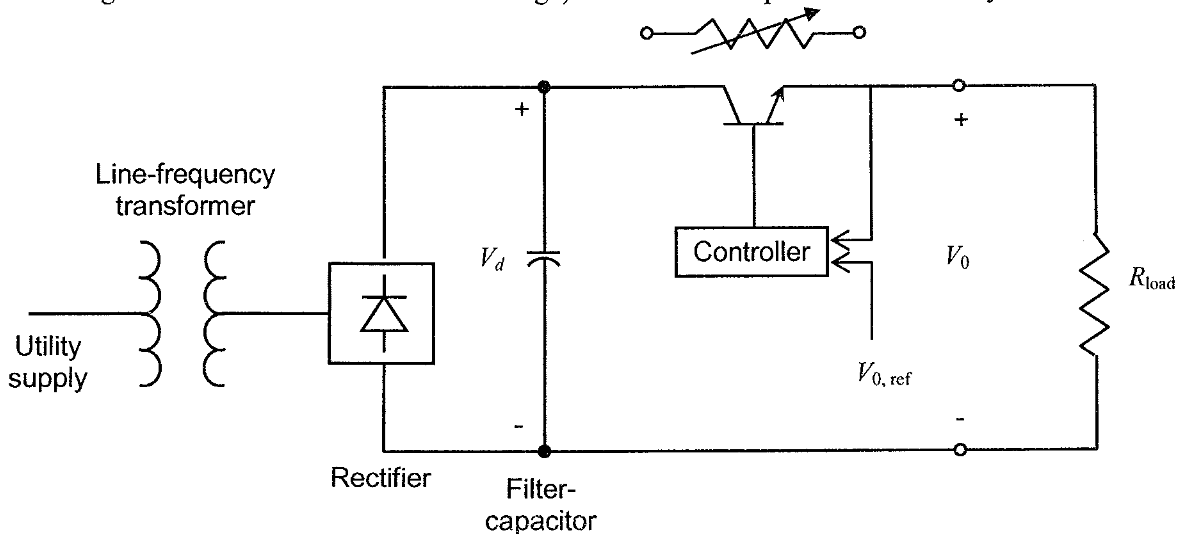
Examiner's comment:

The question proved to be very difficult. In spite of this there were some good attempts and some candidates were able to draw the equivalent circuit of the structure correctly.

4.

Linear electronics

The figure below shows a typical linear AC-DC converter and some voltage waveforms (at the transformer secondary and output). . In the linear power supply a line- is used to for stepping down the line voltage to an appropriate level (close to the level of the desired DC output). The voltage at the secondary is then rectified and filtered so that the resultant voltage V_d (which depends on the utility supply magnitude and its variations, typically 10%) is slightly higher than the output voltage V_o. The transistor, used in common base configuration absorbs the voltage difference between V_o and V_d and behaves like a controlled resistor. In this configuration the transistor dissipates a lot of power as the current flowing from collector to emitter is very high (the voltage at the secondary winding is low and therefore the current is high) and the device operates continuously



Disadvantages

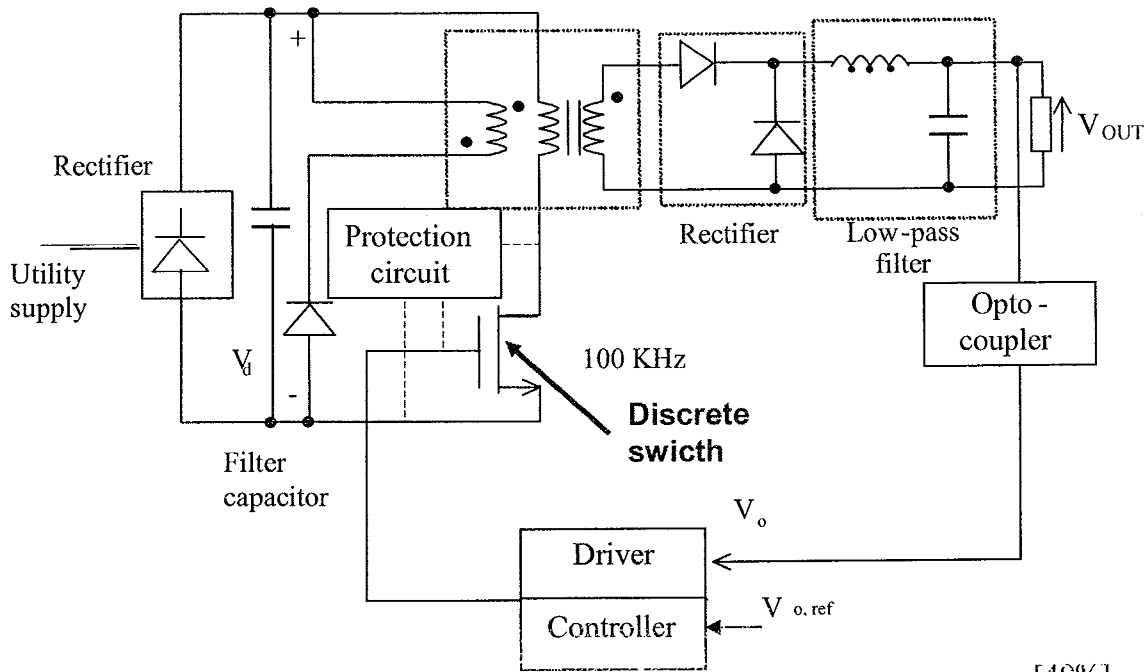
- very low efficiency (typically 30-50% !) (losses are high in the transistor as this operates as an 'adjustable resistor')
- the low frequency line transformer is very heavy and large - remember low $\omega \Rightarrow$ large L (to achieve the same reactance ωL) $\Rightarrow$ large size and weight
- heating problems (due to excessive power losses) which lead to reliability problems

Advantages

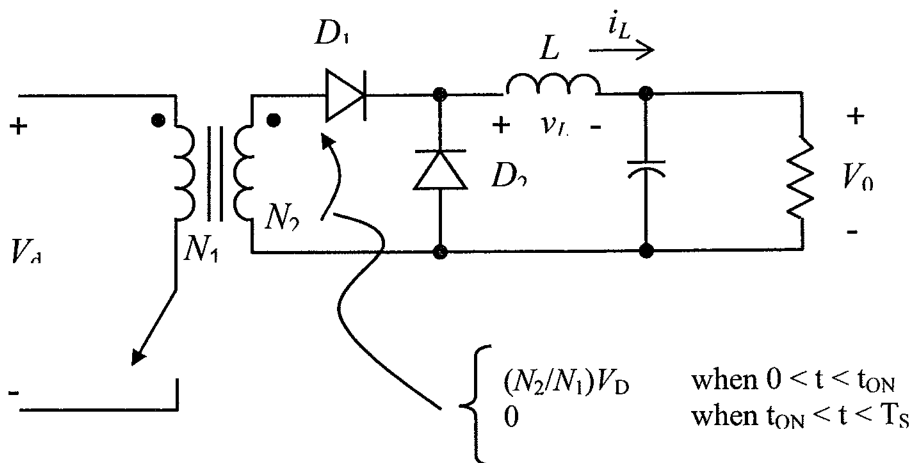
- presently cheaper than switching mode electronics, although the prices in power electronics are decreasing rapidly
- operation at low frequency means the EMI (electro-magnetic interference) is less severe.

Switching mode power electronics

The AC-DC converter is shown below. The signal provided by the utility supply is first rectified and filtered to obtain a high DC voltage V_d. The DC voltage is then converted back into an AC form by switching the transistor ON/OFF at high frequencies (e.g. 100 KHz). The transistor is placed on the primary side of the transformer and therefore sees a high voltage (in the OFF state) and a lower current in the ON state (when compared to the output current).. Since the transistor operates ON/OFF with relatively low losses, the efficiency of the system can be dramatically improved! The ac voltage at the secondary is then rectified by the output diodes and a low-pass filter is used to extract its average DC component so that the load sees a constant DC voltage. A feedback is provided from the output voltage to the gate of the transistors via a controller. This ensures that no matter what the load is, the output voltage remains unchanged. This can be done by finely adjusting the ON to OFF time ratio of the transistor.



[40%]

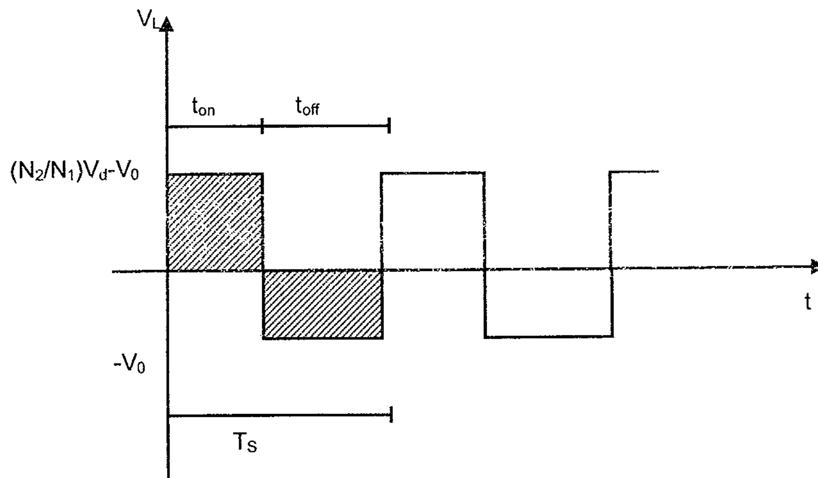


Initially when the switch is ON, D1 is forward biased and D2 is reverse biased. Therefore:

$V_L = \frac{N_2}{N_1} V_d - V_0$ when switch is ON

(ii) When the switch is OFF the inductor current i_L circulates through D2:

$V_L = -V_0$ when switch is OFF



Since the average power dissipated in the inductor is zero, we can equate the integral of the inductor voltage over one period to zero. The result is a DC voltage V_0 across the load:

$V_0 = \frac{N_2}{N_1} V_d \frac{t_{on}}{T_S}$ where $\frac{t_{on}}{T_S}$ is the duty cycle D and $\frac{N_2}{N_1}$ is the transformer turns ratios.

$$t_{ON}\left(\frac{N_2}{N_1} V_d - V_0\right) = V_0\left(T_S - t_{ON}\right) \Rightarrow V_0 = \frac{N_2}{N_1} V_d \frac{t_{ON}}{T_S}$$ [30%]

The feedback helps to maintain a constant DC level at the output with minimum ripple. The feedback provides a negative feedback that can adjust in small steps the duty cycle (via PWM) or the switching frequency (FM) to make sure that the output remains at a constant level. [10%]

The MOSFET will perform better at higher switching frequency than the IGBTs as there is no plasma in drift region (unipolar conduction). Thus at frequencies beyond 100kHZ, the Power MOSFET often is a more efficient solution than the IGBT. The IGBT is better at high temperatures, as its mixed MOS- bipolar conduction tends to suffer less in temperature compared to that of the MOSFET.The on-state resistance in a Power MOSFET can increase by as much as 2X to 3X, when operated at elevated temperature (125 C). In power the IGBT tends to operate better due to its bipolar conduction, high current density and less temperature sensitivity [20%]